A 15.5 dB, Wide Signal Swing, Dynamic Amplifier Using a Common-Mode Voltage Detection Technique

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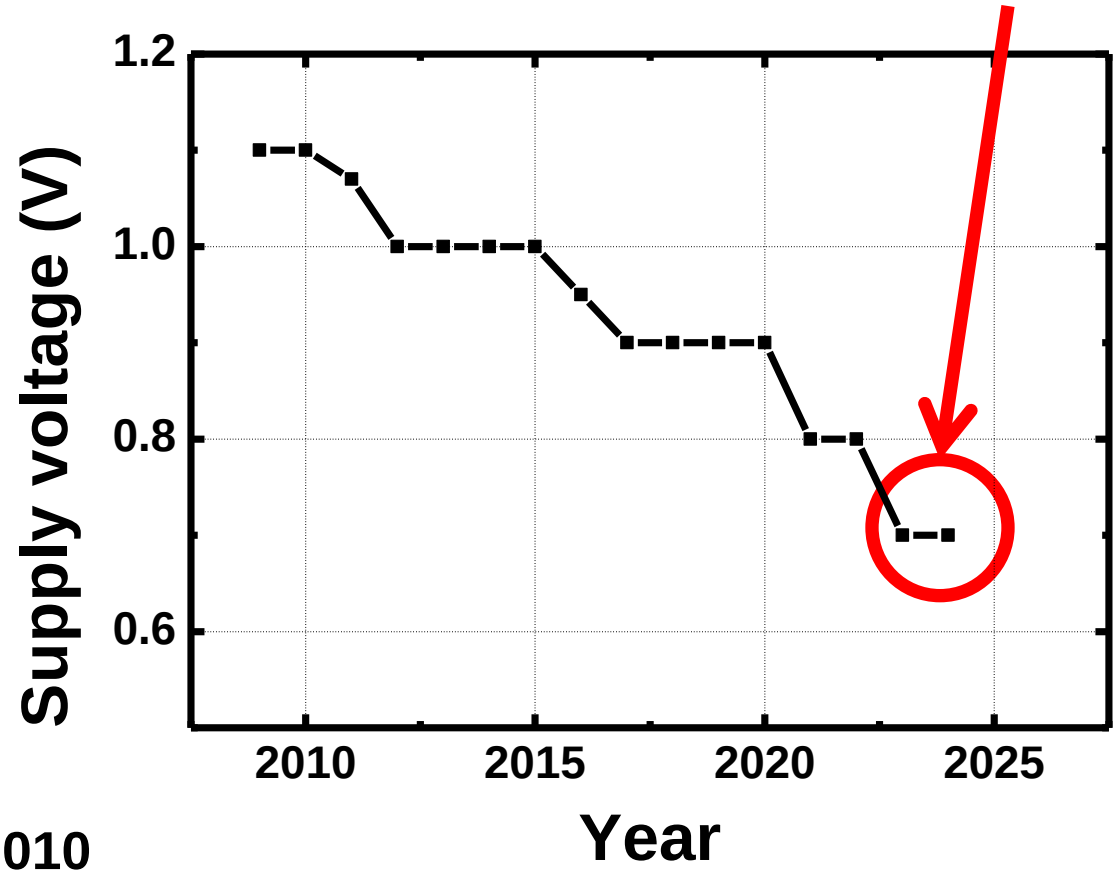
Outline

- **Motivation**
- **Background**
- **Design Concept**
- **Circuit Implementation**
- **Conclusion**

Roadmap

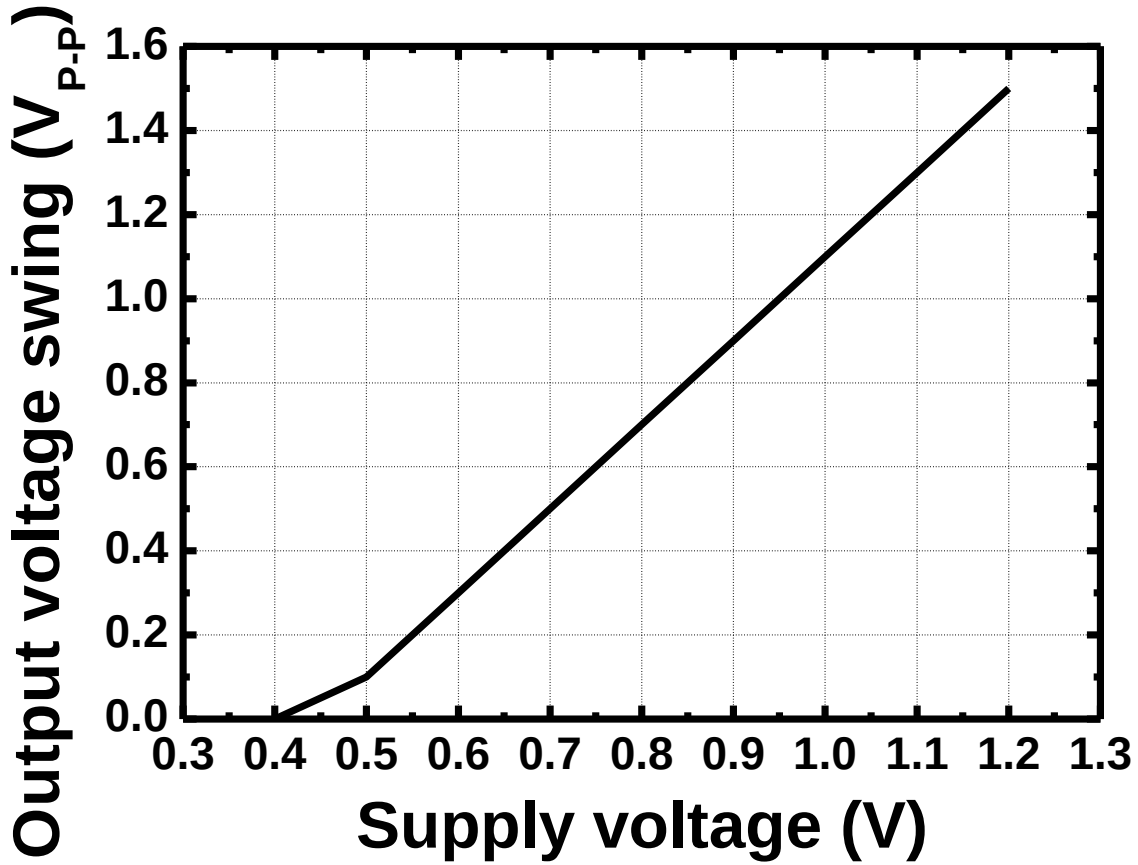
- ITRS's roadmap for future supply voltage [1]
- What are some foreseeable difficulties? [2]



[1] ITRS, 2010
[2] A. Matsuzawa, ISSCC 2011 Forum

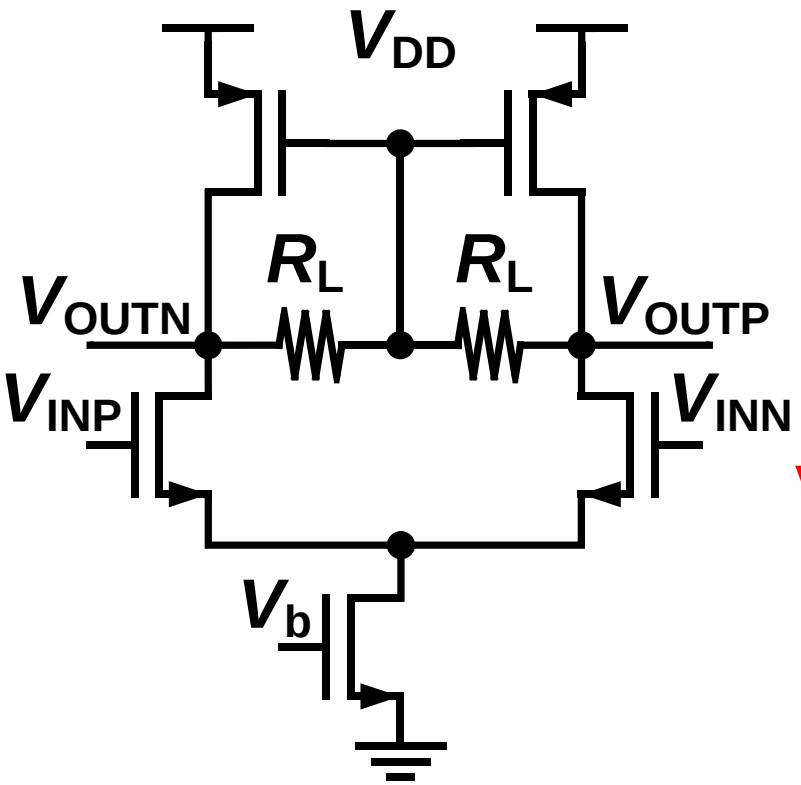
Conventional Amplifier

- **Amplifier design becomes increasingly difficult with supply voltage lowering**

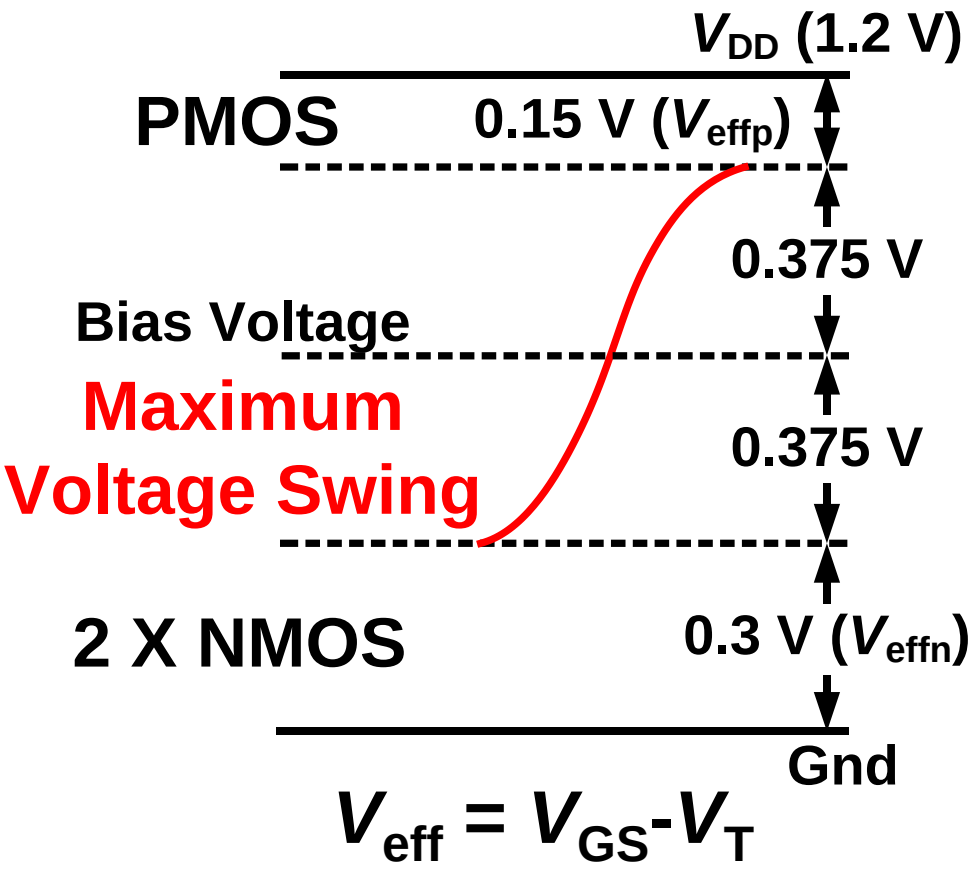


Conventional Signal Swing and Linearity

- **Stacked architecture limits signal swing**



[3] B. Razavi, McGraw-Hill



$V_{eff} = V_{GS} - V_T$

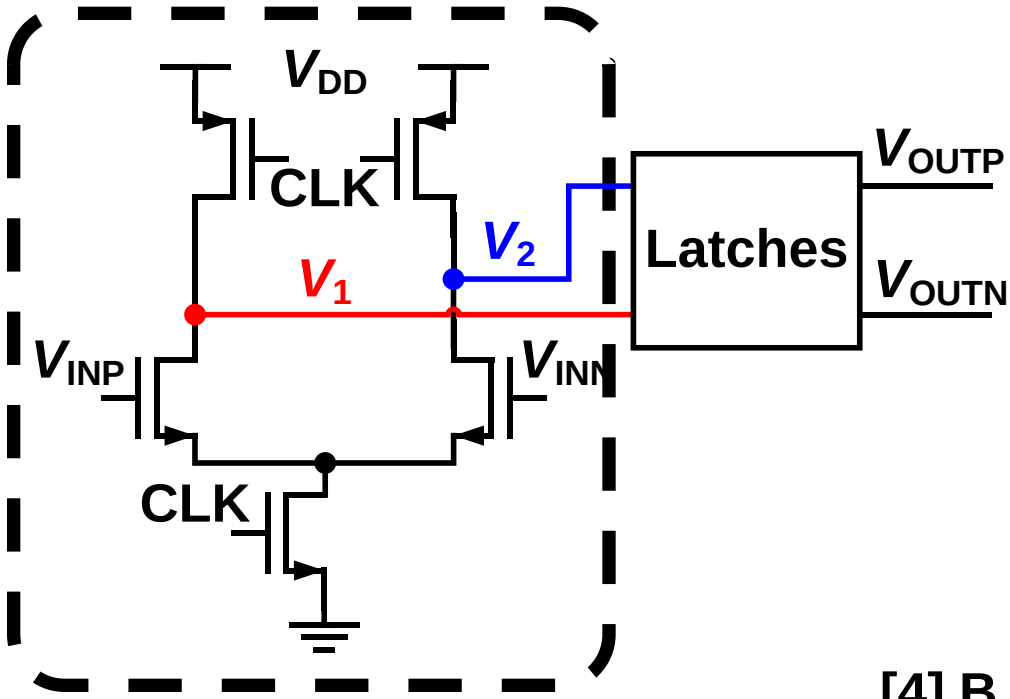
Motivation

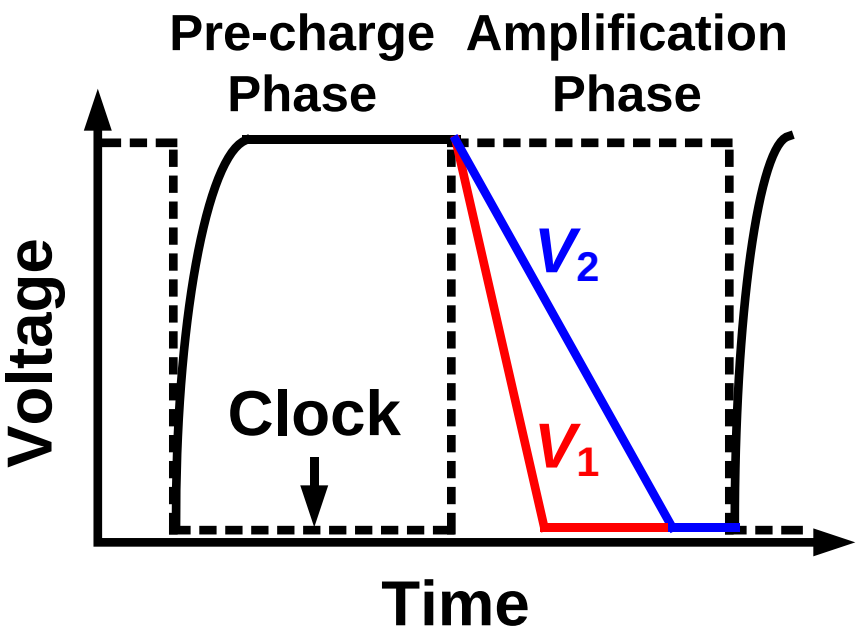
- **Ultra low voltage operation (0.5 V)**
  - **Minimally stacked architecture**
- **Scalable power dissipation with speed**
  - **Dynamic operation for mixed-signal applications**

- **Dynamic amplifier → A minimally stacked amplifier with variable power consumption is proposed**

Conventional Applications

- **Conventional applications:**
  - **Pre-amplifiers for dynamic comparators [4]**
  - **Receiver amplifiers for DRAM circuits [5]**





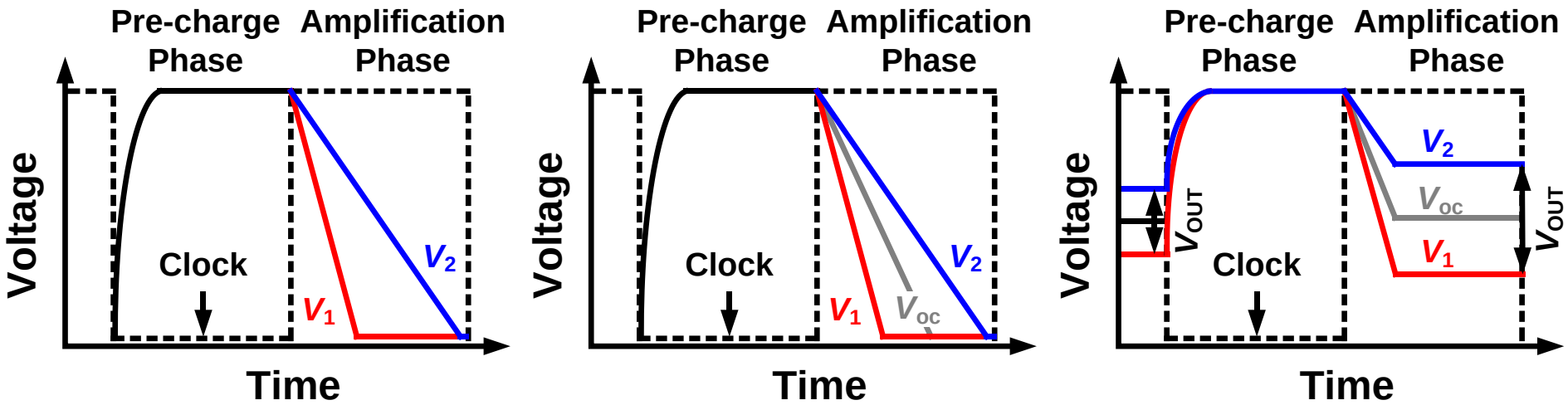
[4] B. Razavi, IEEE Press

[5] H. Fujisawa *et al.*, ESSCIRC 2000

Proposed Waveform

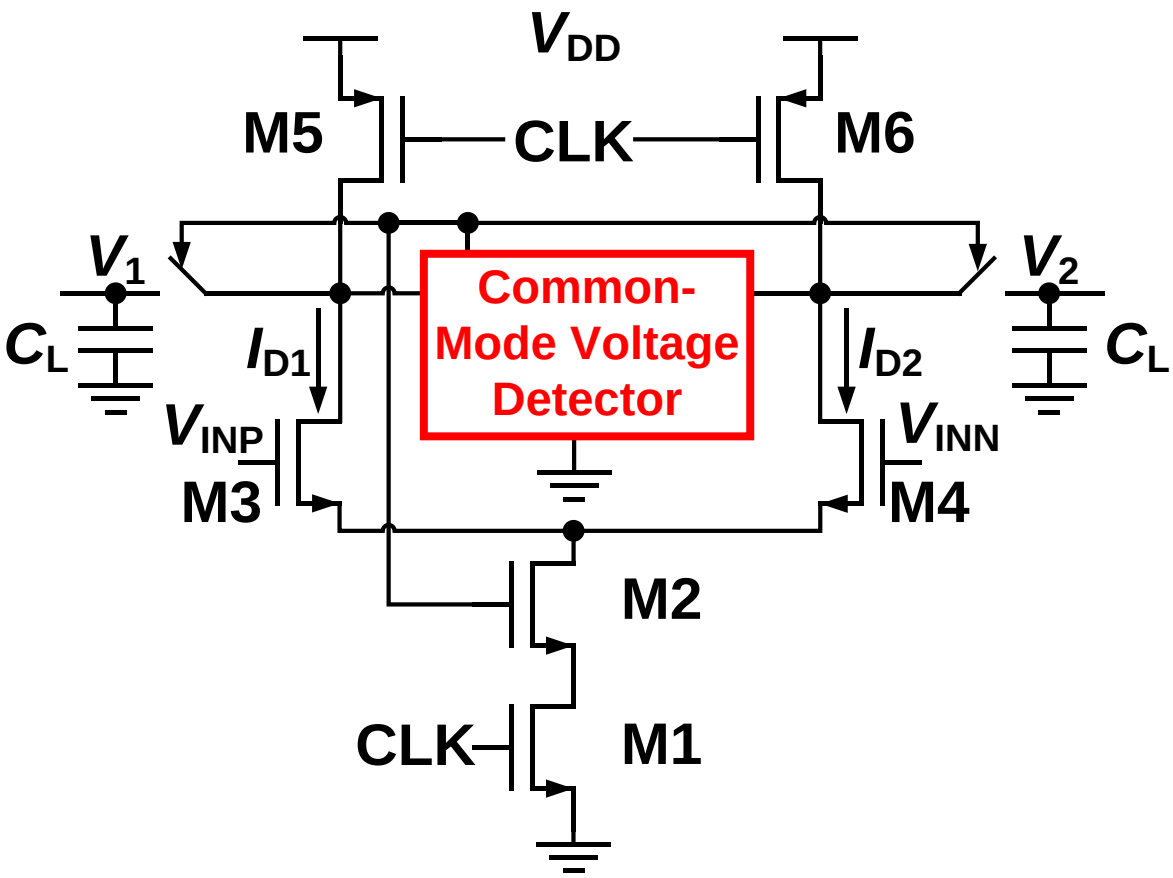
- **If discharging can be terminated**

  → A single stage amplifier can be realized



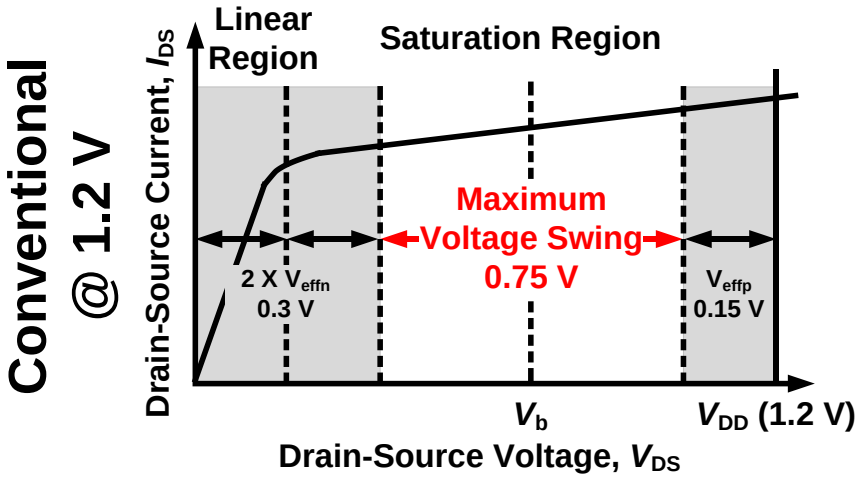
Proposed Architecture

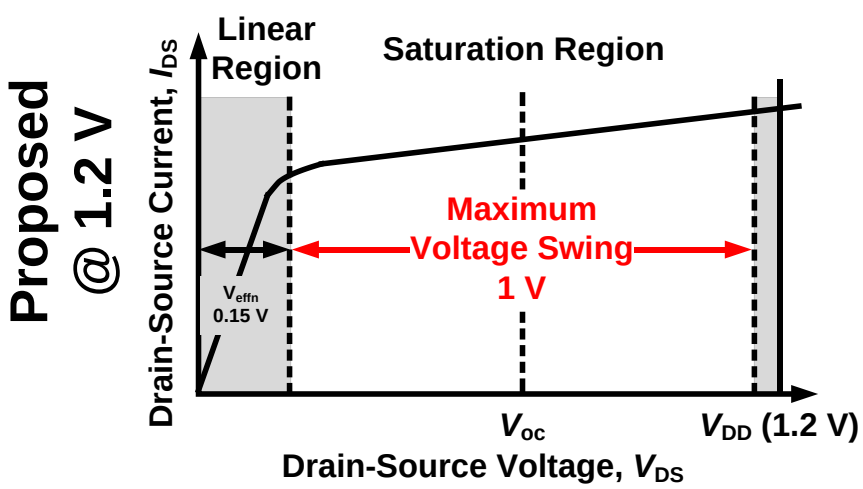
- **A common-mode voltage detector with sampling switches realize dynamic amplification**

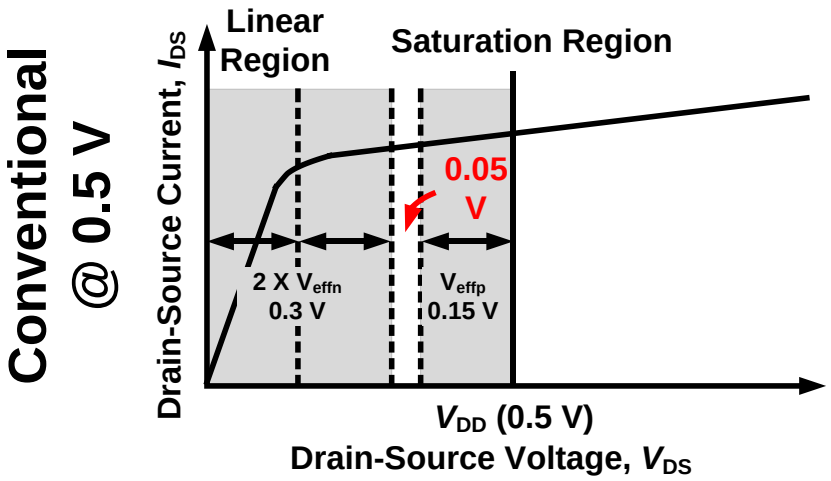


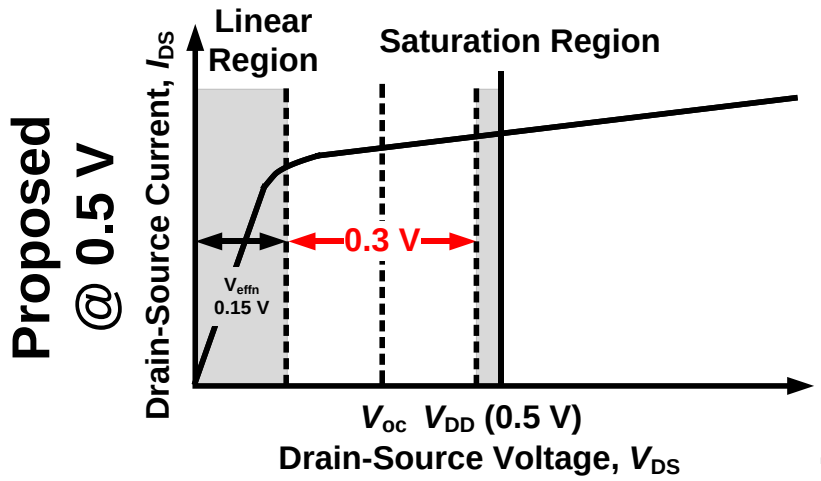
Signal Swing and Linearity

- **Minimally stacked architecture gives extra margin for signal swing**





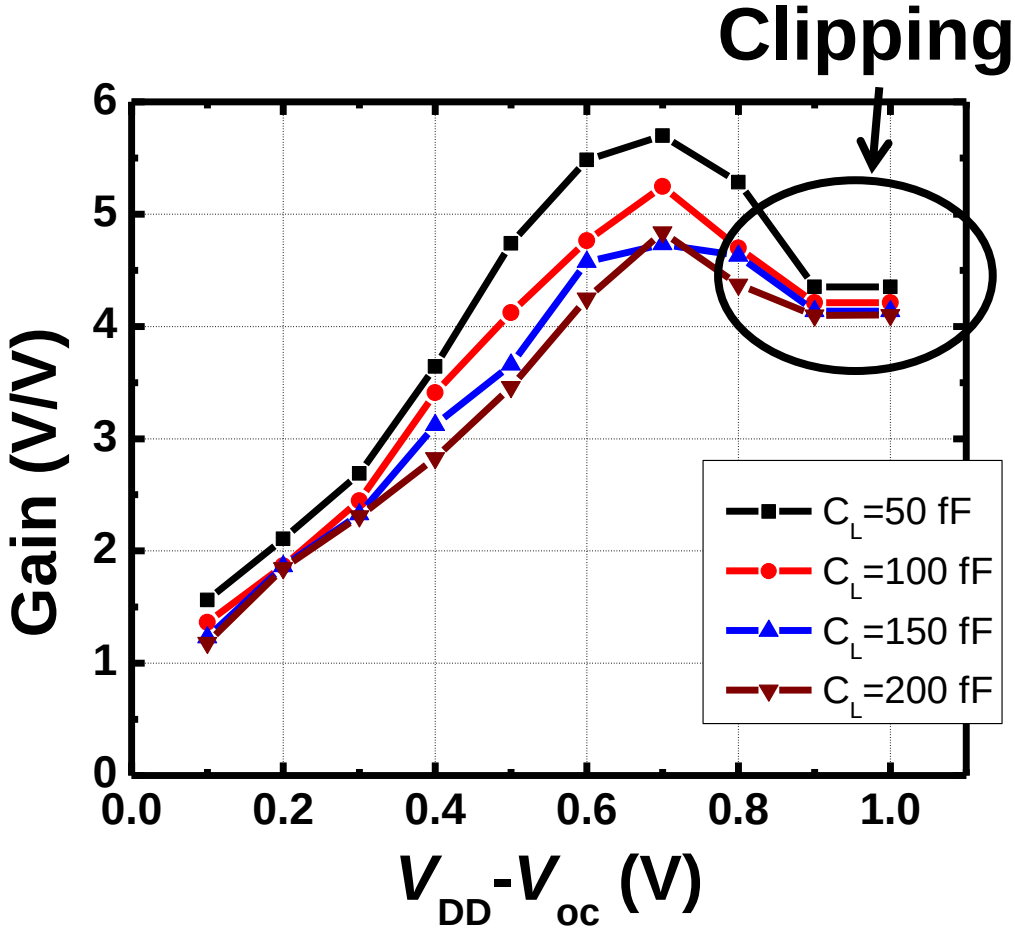




Gain

$$G_{diff} = \frac{2\left(V_{DD} - V_{oc}\right)}{V_{eff}}$$

G_{diff}: differential gain
V_{DD}: supply voltage
V_{oc}: common-mode (CM) output voltage
V_{eff}: effective gate voltage, which is gate-source voltage minus threshold voltage

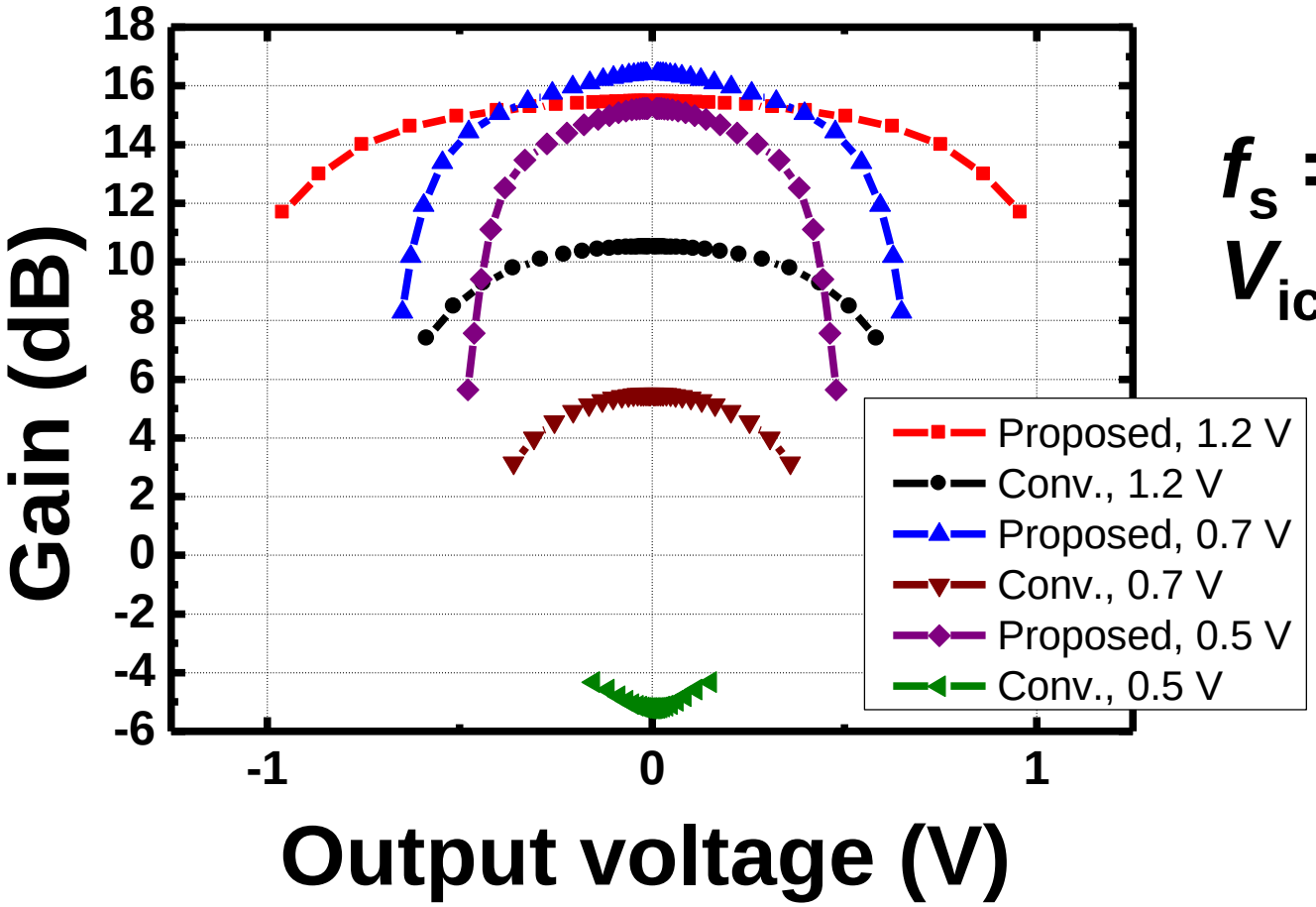


V_{DD} = 1.2 V

$V_{eff} = V_{DD}/2 - V_{thn}$

Signal Swing and Linearity

- **Wider signal swing, especially in low voltage operation**

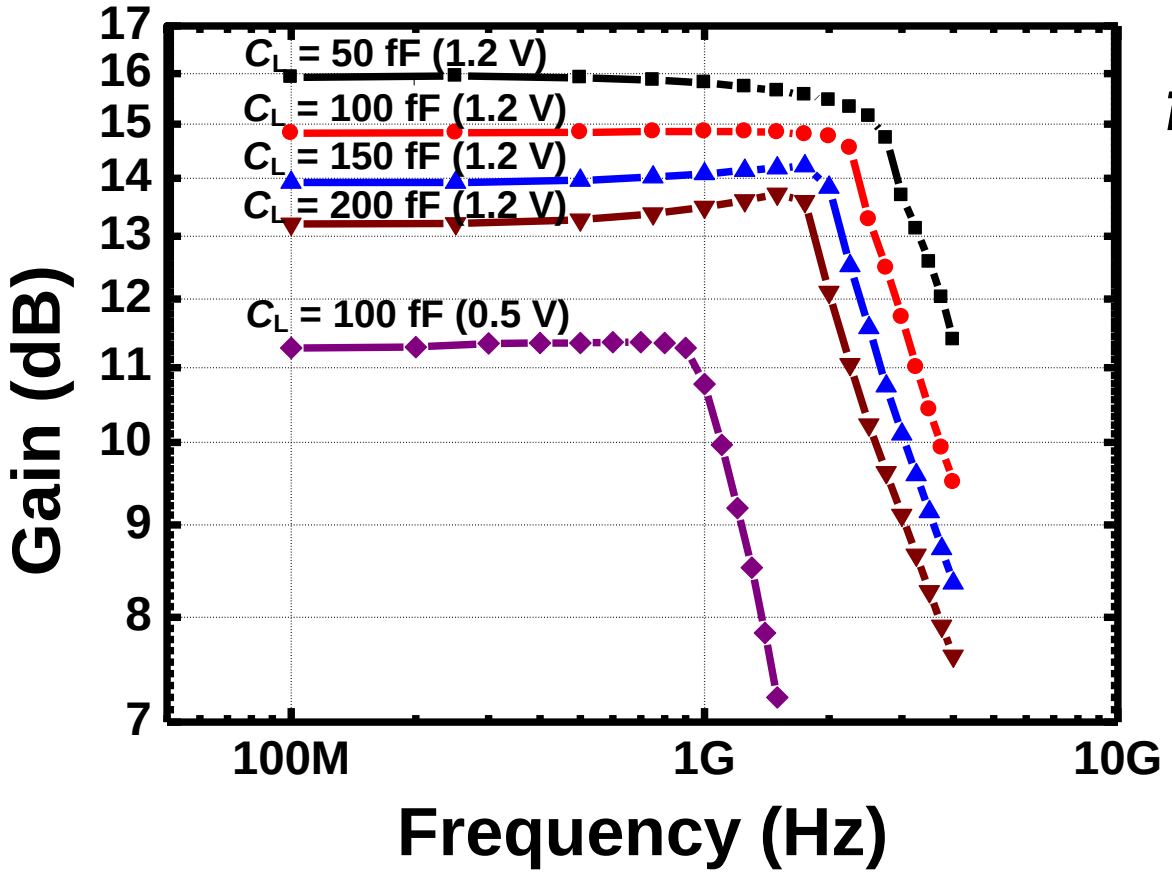


f_s = 50 MHz

$V_{ic} = V_{DD}/2$

Speed

- **Key applications: Mixed-signal circuits**



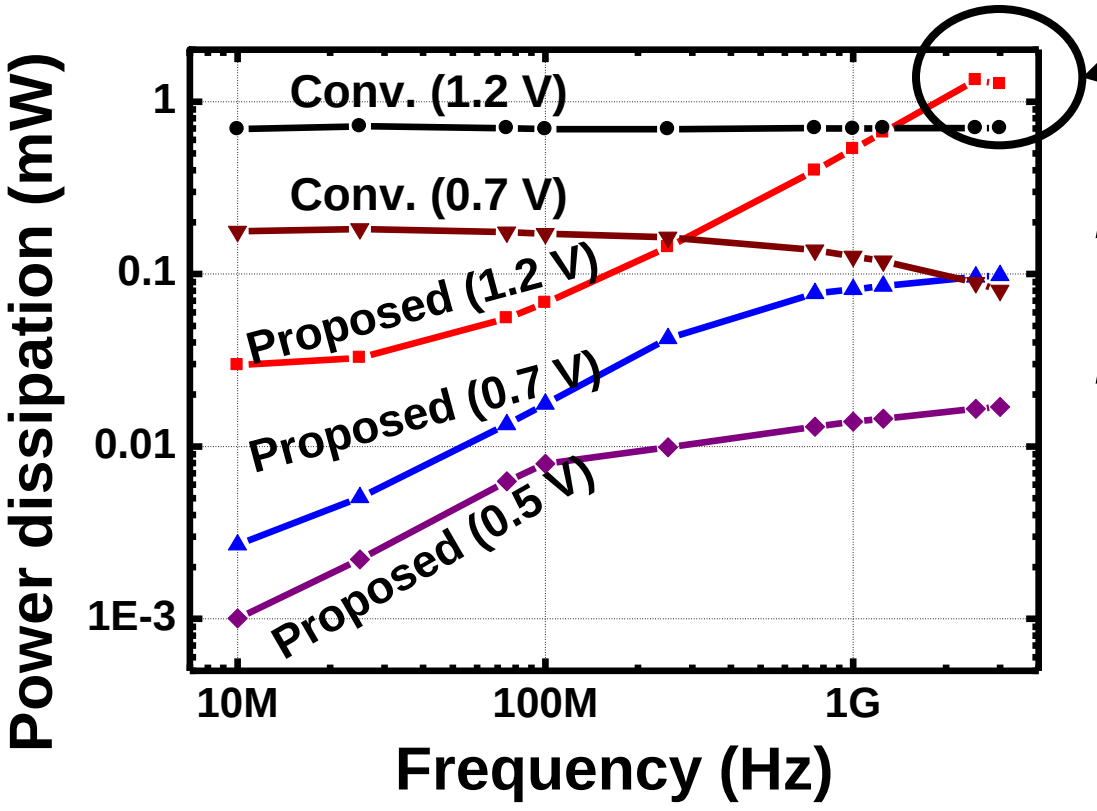
$$f_S = \frac{I_{DCM}}{2(V_{DD} - V_{oc})(C_L + C_P)}$$

- f_S: operating/clock frequency
- I_{DCM}: CM drain current
- C_L: load capacitance
- C_P: parasitic capacitance
- V_{id}: diff.-mode (DM) input voltage
- V_{ic}: CM input voltage

$V_{ic} = V_{DD}/2$ $V_{id} = 0.1$ V

Power Dissipation

- **Scalable power dissipation due to dynamic operation**



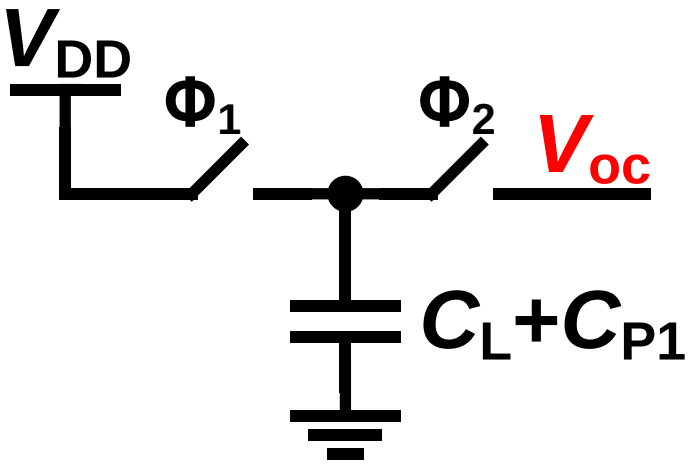
$$P_T(f_S) = P_{Amp}(f_S) + P_{CMD}(f_S)$$

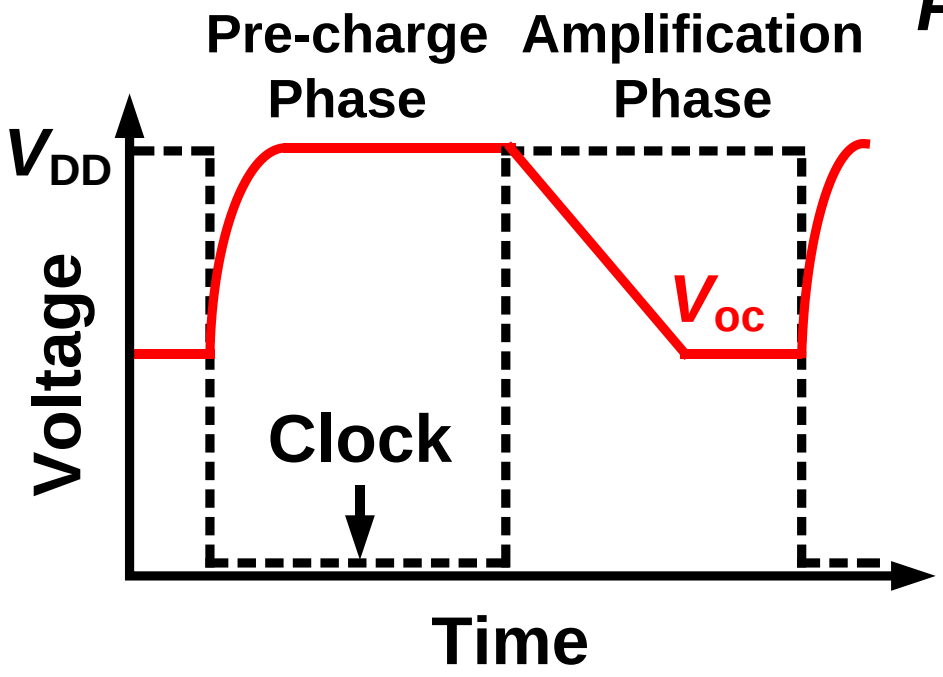
P_T: total power dissipation

P_{Amp}: power dissipation in amplifier circuit

P_{CMD}: power dissipation in logic circuit

Power Dissipation, cont'd





- A dynamic amplifier can save energy

$$P_{CMD} = f_S C_{L2} V_{DD}^{\ 2}$$

$$P_{Amp} = 2\left(C_L + C_{P1}\right) f_S \Delta V \left(V_{DD} - \frac{\Delta V}{2}\right)$$

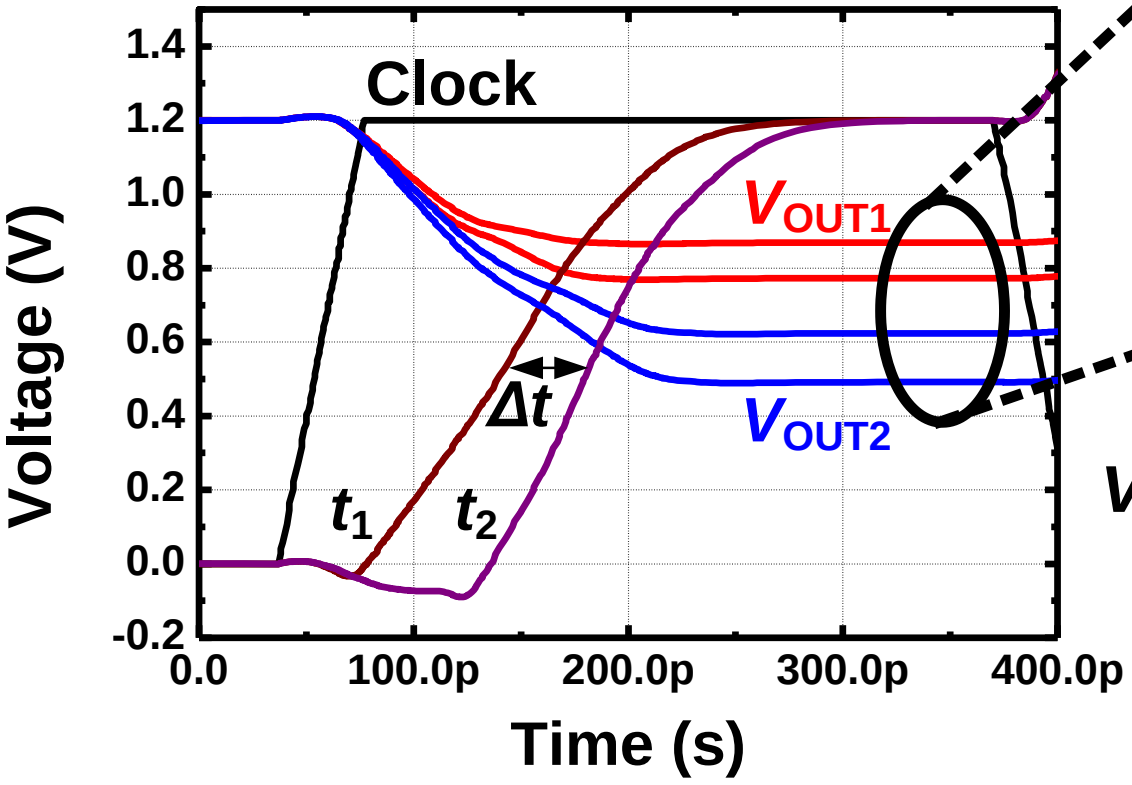
C_{P1}: parasitic capacitance

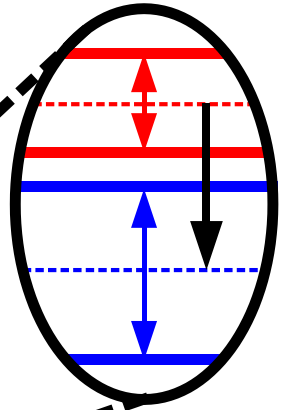
C_{L2}: common-mode detector's load capacitance

ΔV: V_{DD}-V_{oc}

Effects of Delay

- **Delay causes a gain error and a CM output voltage shiftc**





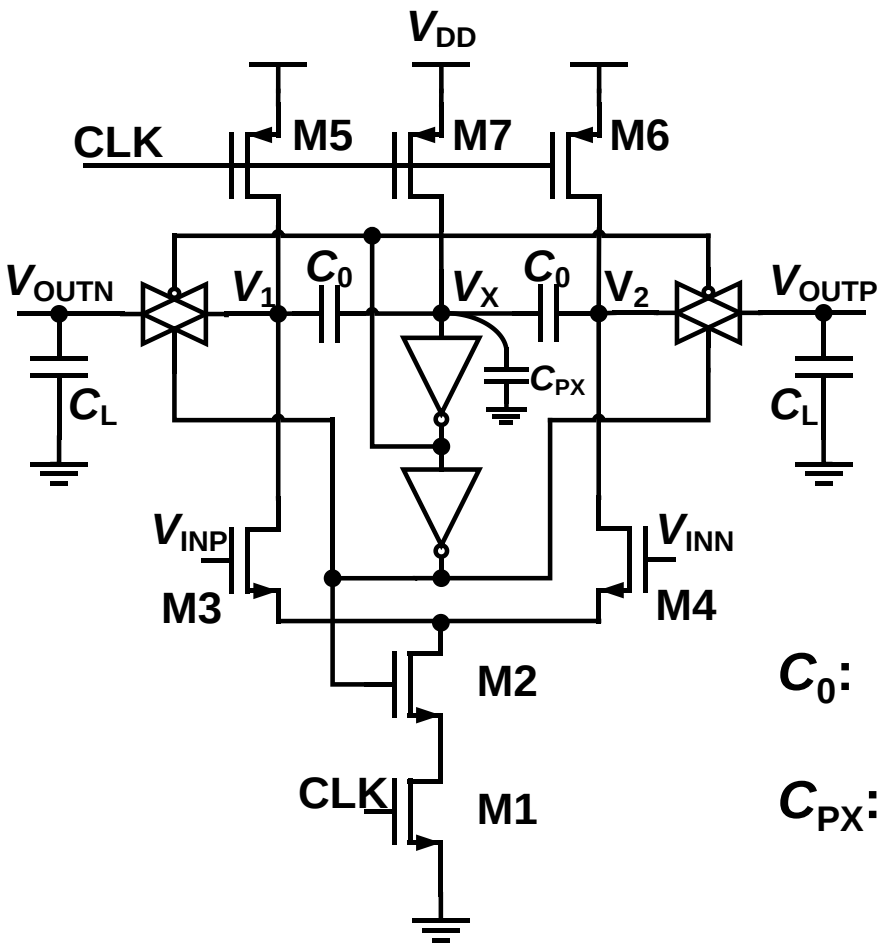
V_{oc} shift

$$V_{OUT} = \left(\frac{I_{D1} - I_{D2}}{I_{DCM}} \right) \left(V_{DD} - V_{oc} \right)$$

$$+ \left(\frac{I_{D1} - I_{D2}}{C_L} \right) t_d$$

Circuit Implementation

- **Parasitic capacitance causes a common-voltage error**



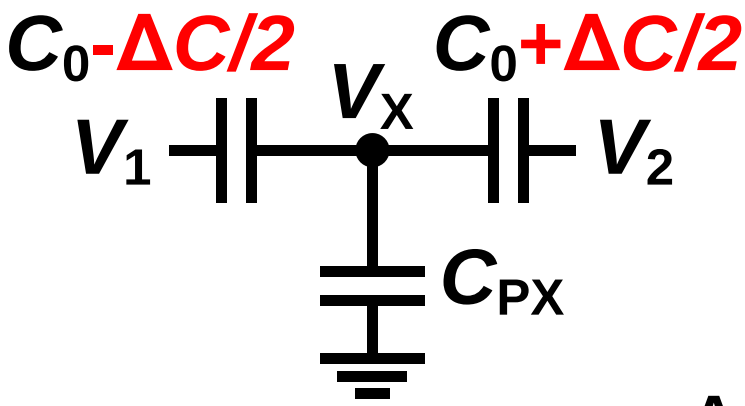
$$V_X = \frac{1}{1+\frac{C_{PX}}{2C_0}}\left(\frac{V_1+V_2}{2}\right) + \frac{C_{PX}}{2C_0+C_{PX}}V_{DD}$$

C_0: common-mode detector's sampling capacitor

C_{PX}: parasitic capacitance at node X

Sampling Capacitor Mismatch

- **Capacitor mismatch causes a gain error**



Pre-charge phase:

$$V_1 = V_2 = V_X = V_{DD}$$

$$Q_X = C_{PX} V_{DD}$$

$$Q_X' = Q_X$$

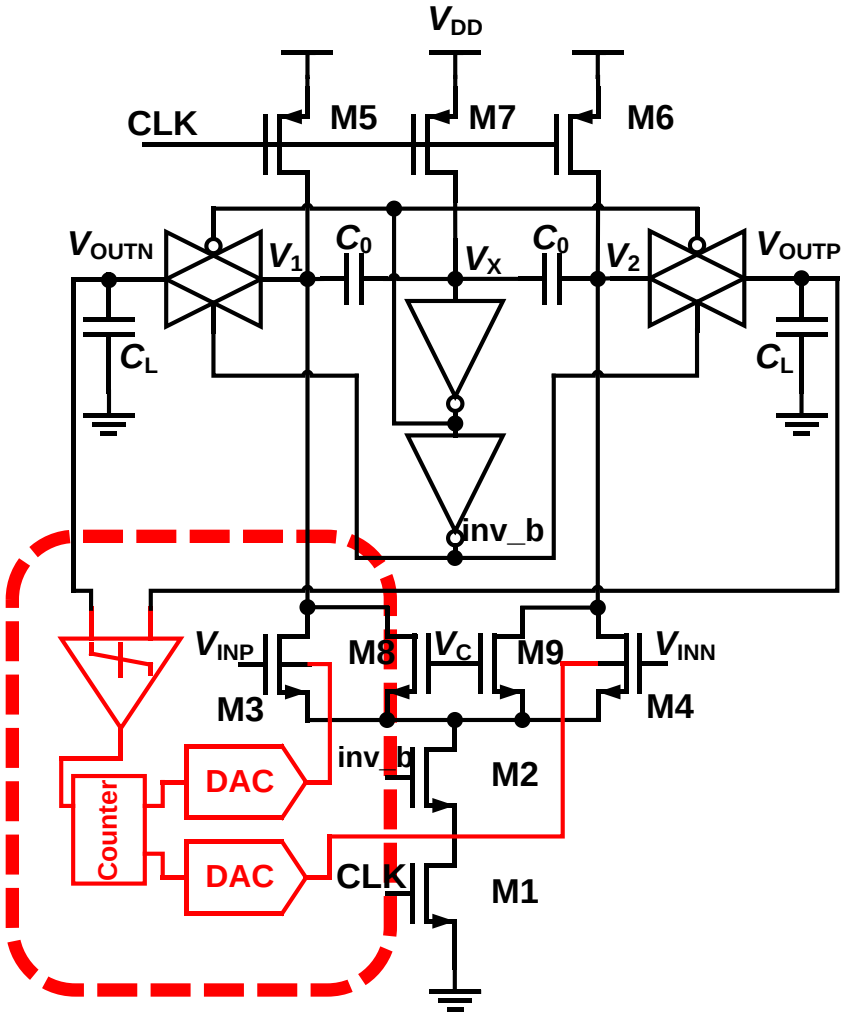
Amplification phase:

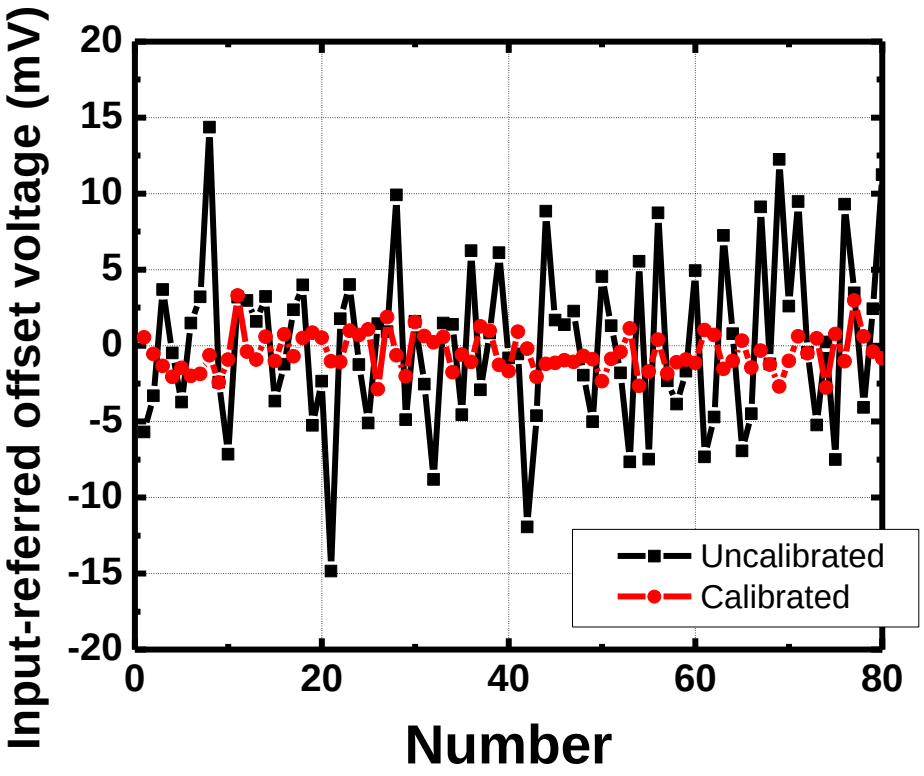
$$V_X = \frac{C_{PX} V_{DD} + C_0 (V_1 + V_2) - \frac{\Delta C}{2}(V_1 - V_2)}{2C_0 + C_{PX}}$$

$$V_X = \frac{1}{1 + \frac{C_{PX}}{2C_0}} \left(\frac{V_1 + V_2}{2} \right) + \frac{C_{PX}}{2C_0 + C_{PX}} V_{DD} - \frac{\Delta C}{2C_0 + C_{PX}} \left(\frac{V_1 - V_2}{2} \right)$$

Mismatch Calibration

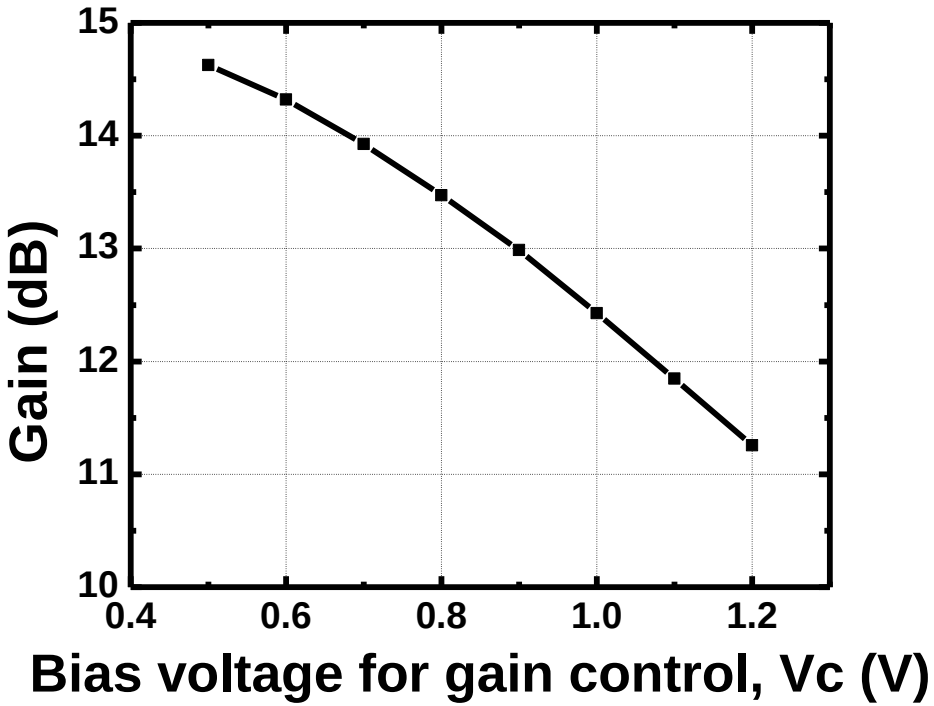
- **5.59 mV (σ) →1.27 mV (σ)**

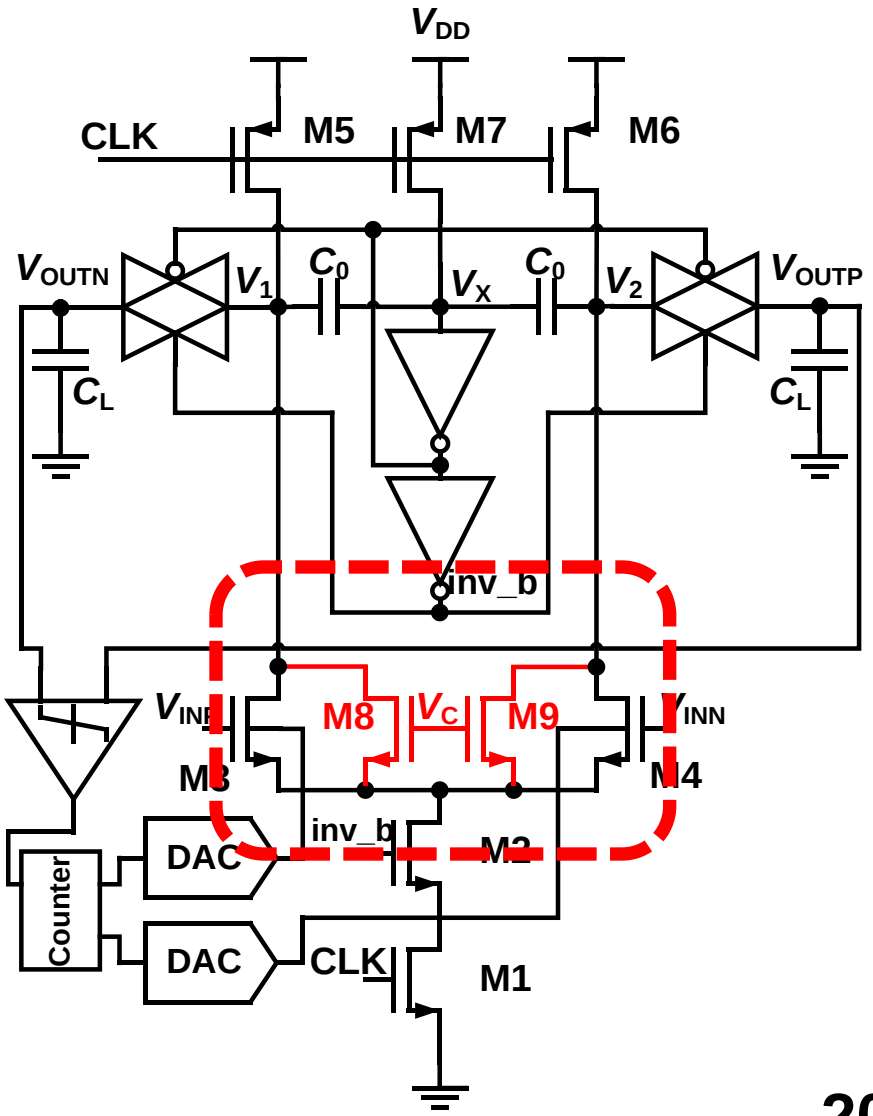




Gain Control

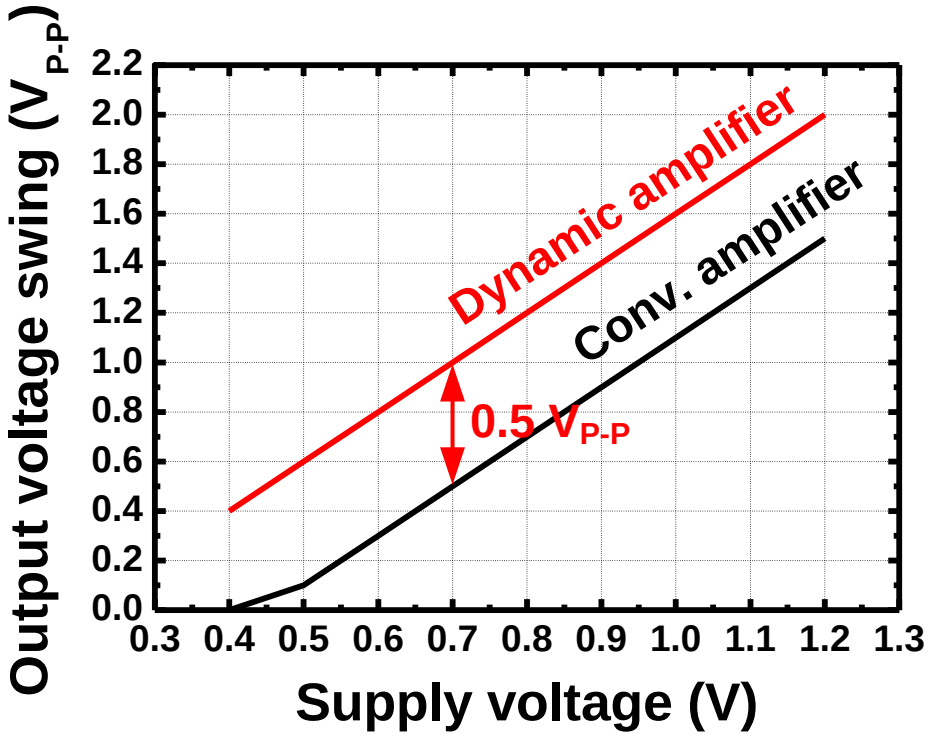
- **3 dB gain control**





Conclusion

- **A dynamic amplifier realizes**
  - **0.5 V ultra low voltage operation**
  - **Wider signal swing**
  - **Variable power dissipation for clock scalable circuits**



Future Work

- **Low-voltage ADC using dynamic amplifiers**
- **Other RF applications such as sampling mixers**

References

[1] International Technology Roadmap for Semiconductors, "2010 update – RF and analog mixed-signal CMOS technology requirements," Dec. 2009.

[2] A. Matsuzawa, "An ultra low power analog and ADC design," ISSCC Forum, Feb. 2011.

[3] B. Razavi, "Design of analog CMOS integrated circuits," McGraw-Hill, 2001.

[4] B. Razavi, "Principle of data conversion system design," IEEE Press, 1994.

[5] H. Fujisawa, T. Takahashi, M. Nakamura, and K. Kajigaya, "A dual phase-controlled dynamic latched (DDL) amplifier for high-speed and low-power DRAMs," Proc. 26th Eur. Solid-State Circuits Conf., pp. 184-187, Sept. 2000.

Thank you for your interest!

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