A High-Speed Clock-Scalable Dynamic Amplifier for Mixed-Signal Applications

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Outline

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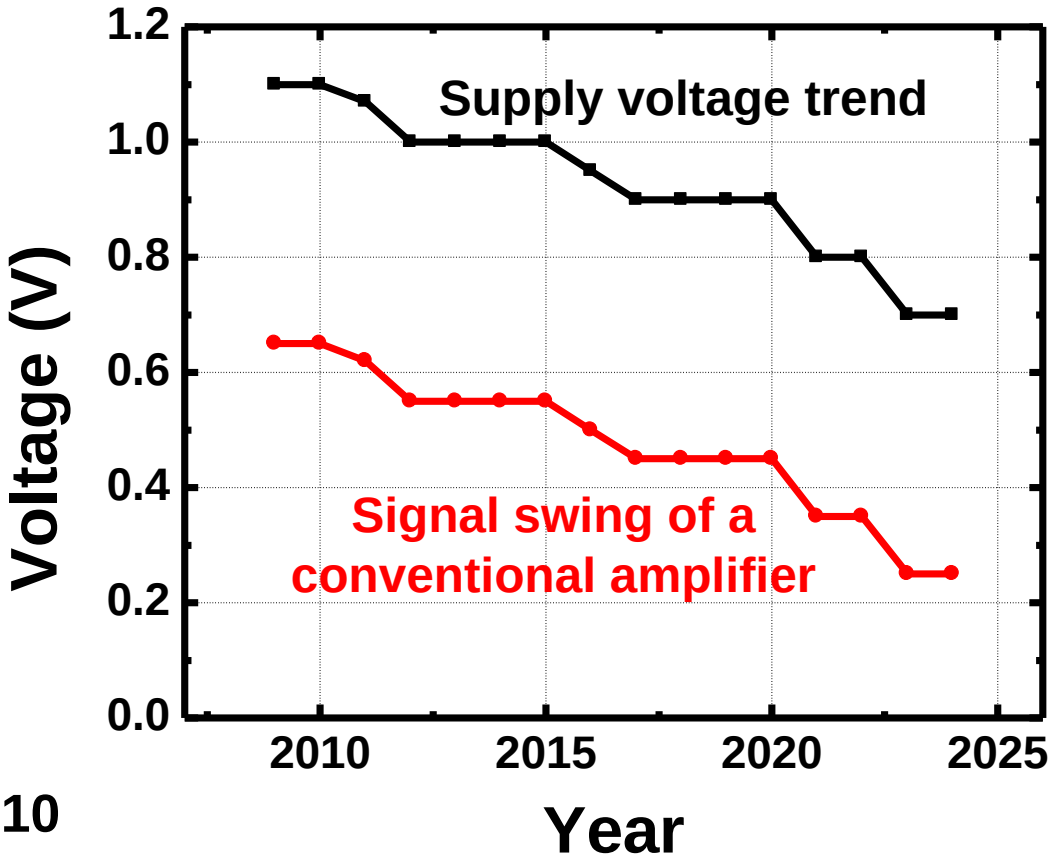
1. Background
2. Motivations
3. Circuit Design
4. Conclusion
5. Future Work

Technology Roadmap

- ITRS's roadmap for future supply voltage [1]
- What are some foreseeable difficulties? [2]

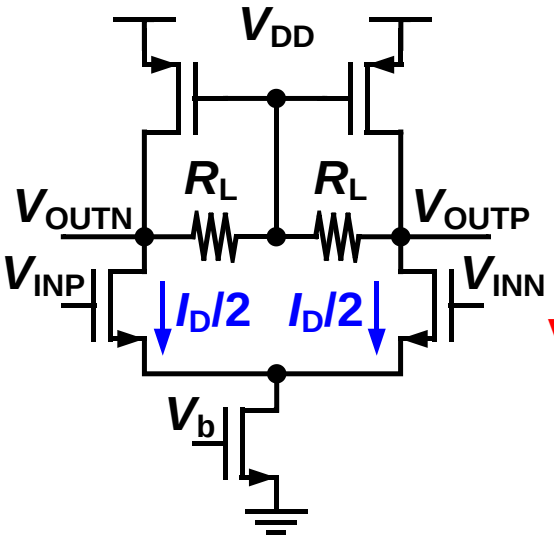


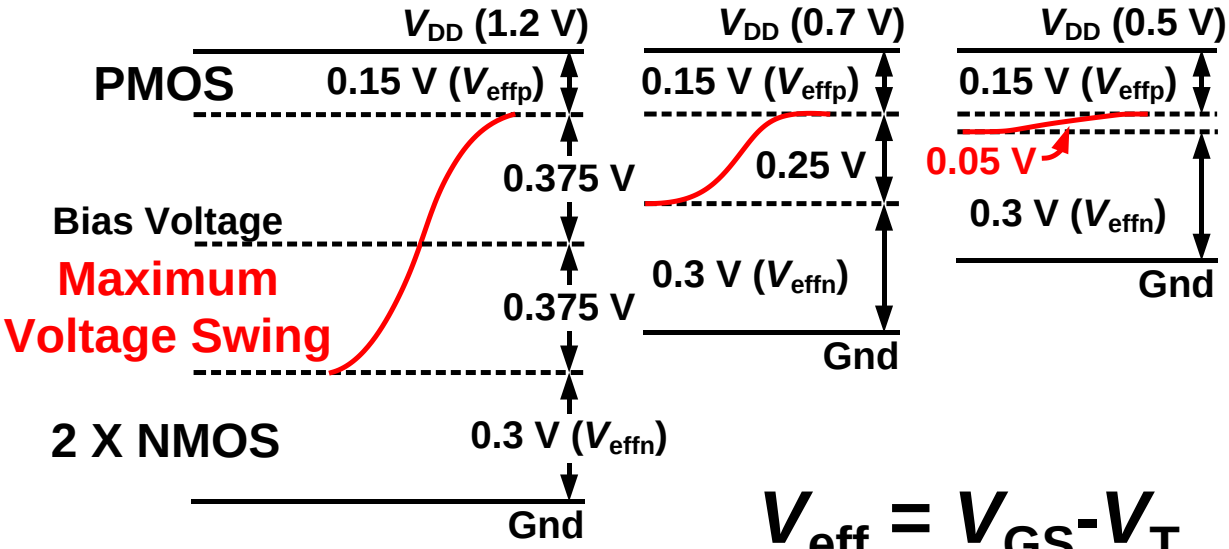
[1] ITRS, 2010

[2] A. Matsuzawa, ISSCC 2011 Forum

Conventional Signal Swing and Linearity

- **Stacked architecture limits signal swing**
- **Conventional analog amplifier consumes static current**





$$V_{eff} = V_{GS} - V_T$$

[3] B. Razavi, McGraw-Hill

Motivation

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- **A wide output swing amplifier (up to 0.5 V)**
  - **Minimally stacked architecture**
- **Clock scalable power consumption**
  - **Dynamic operation for mixed-signal applications**

- **Dynamic amplifier → A minimally stacked amplifier with variable power consumption is proposed**

Proposed Dynamic Amplifier

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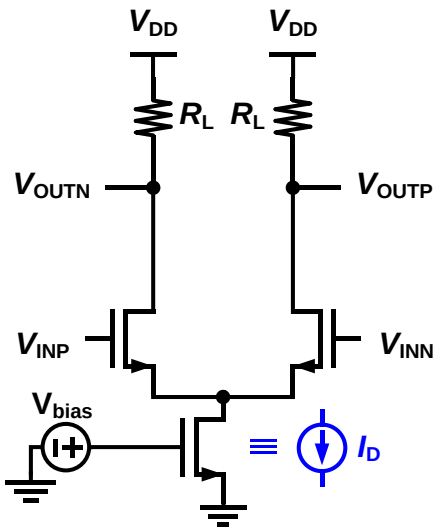

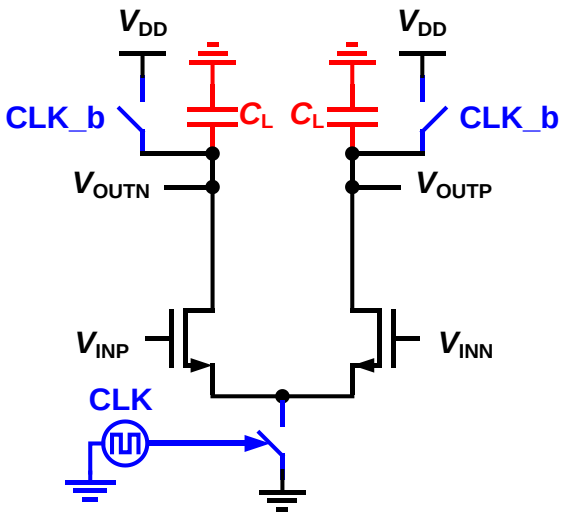

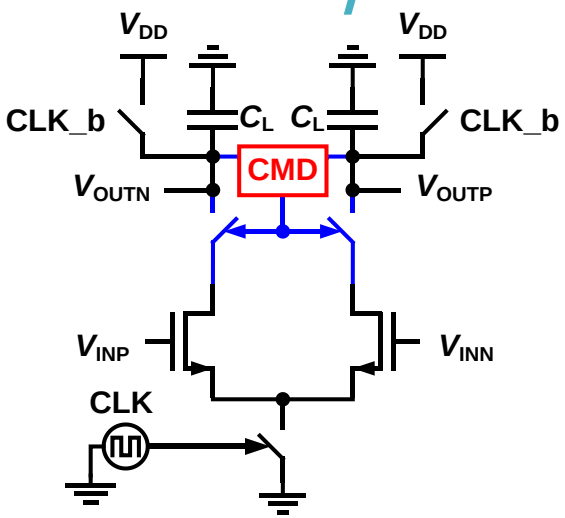

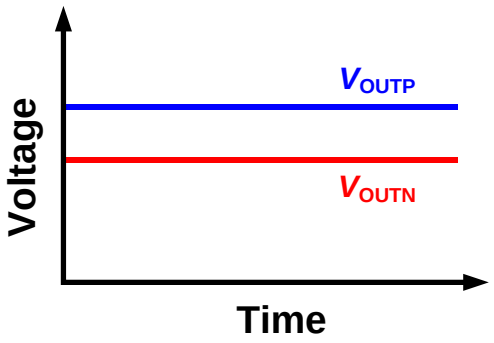

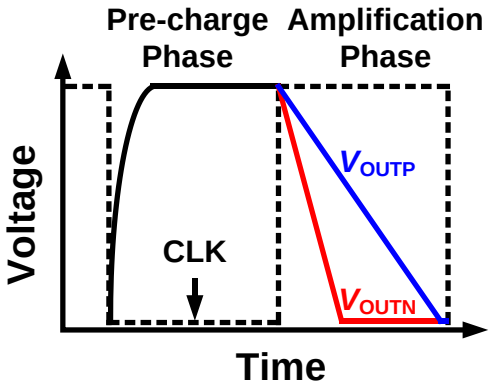

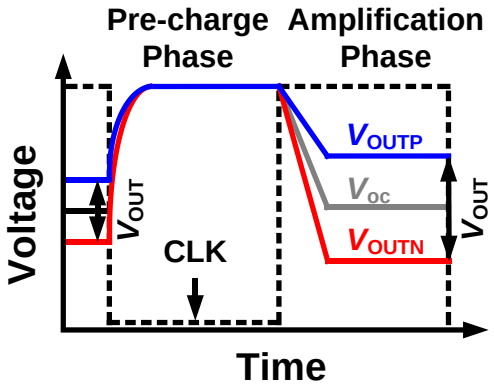

$G = g_m R_L$
$P_d = I_D V_{DD}$

Conventional Continuous-Time Amplifier

$P_d = fC_T V_{DD}^2$
C_T: Total capacitance

Conventional Dynamic Amplifier

$G = V_{DD}/V_{eff}$
$P_d = fC_T V_{DD}^2$

Proposed Dynamic Amplifier

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Signal Swing and Linearity

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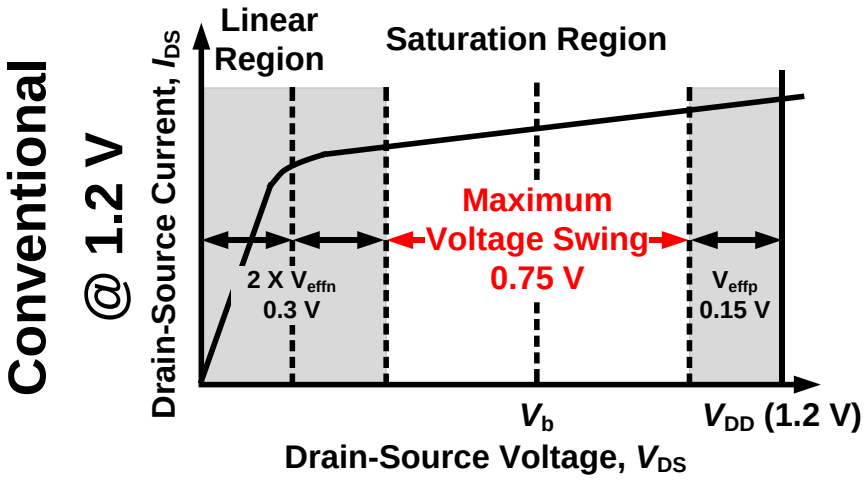
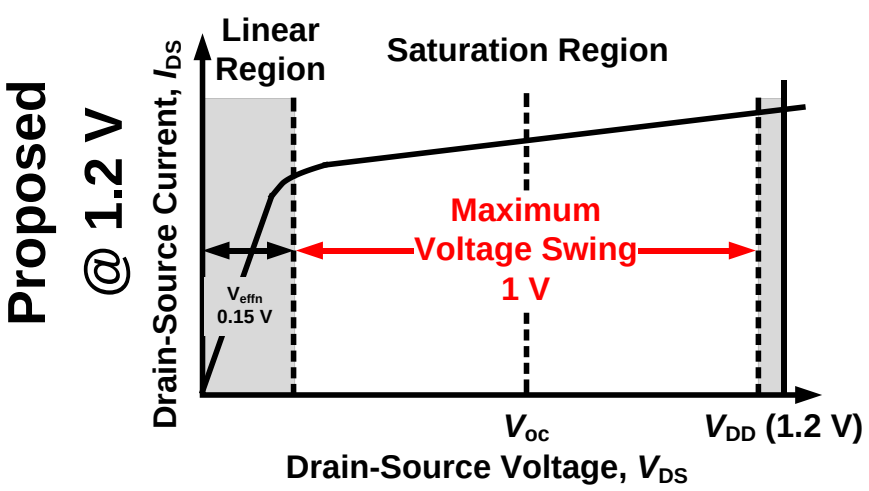
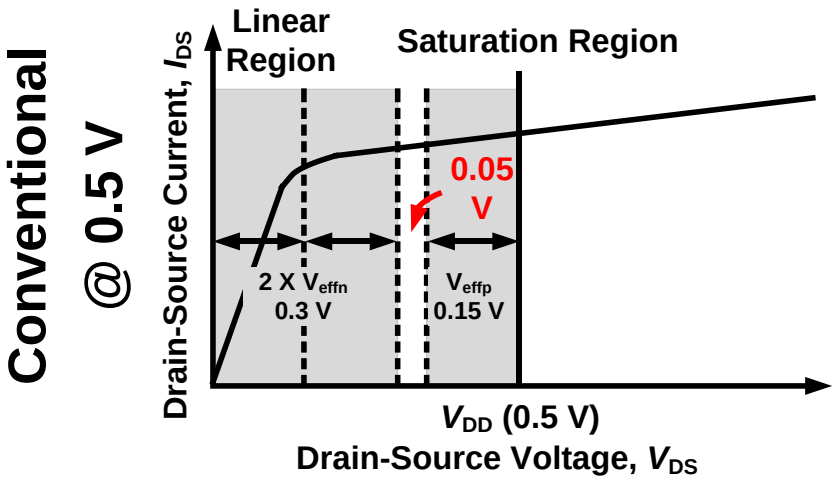
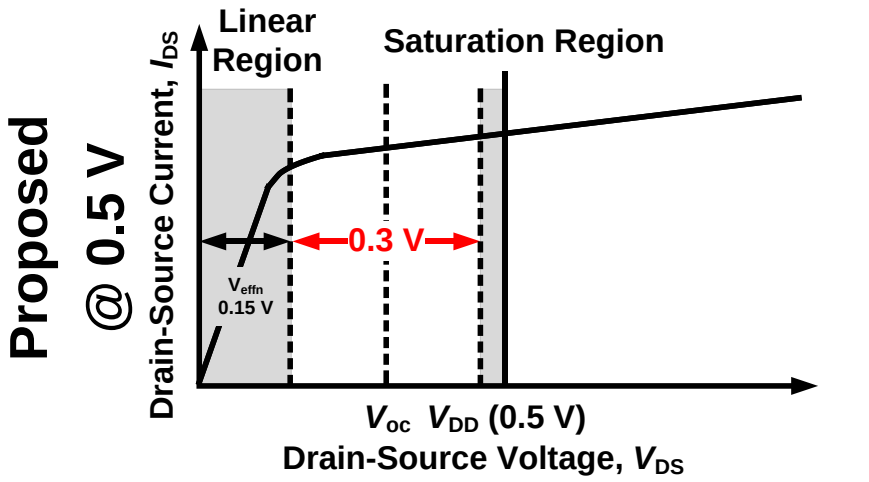
- **Minimally stacked architecture gives extra margin for signal swing**









Key Features

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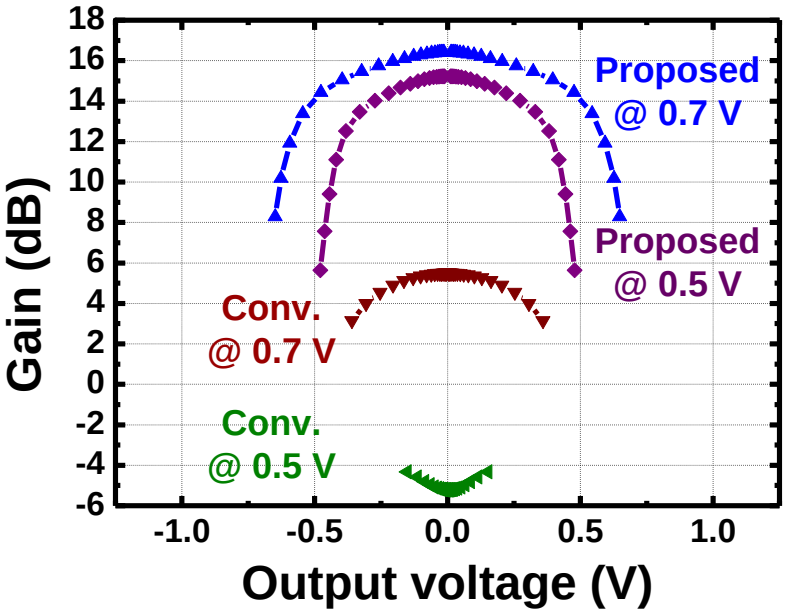
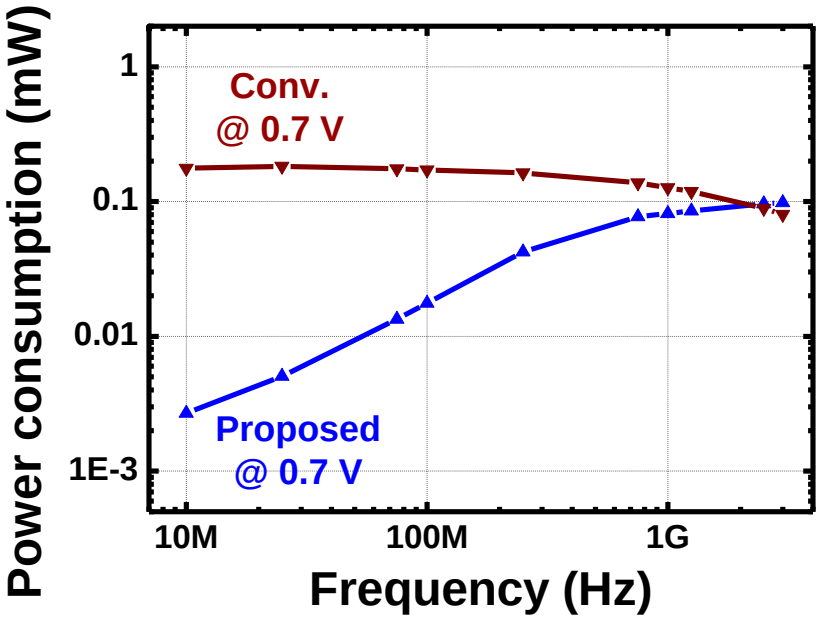
Signal Swing



Power Consumption

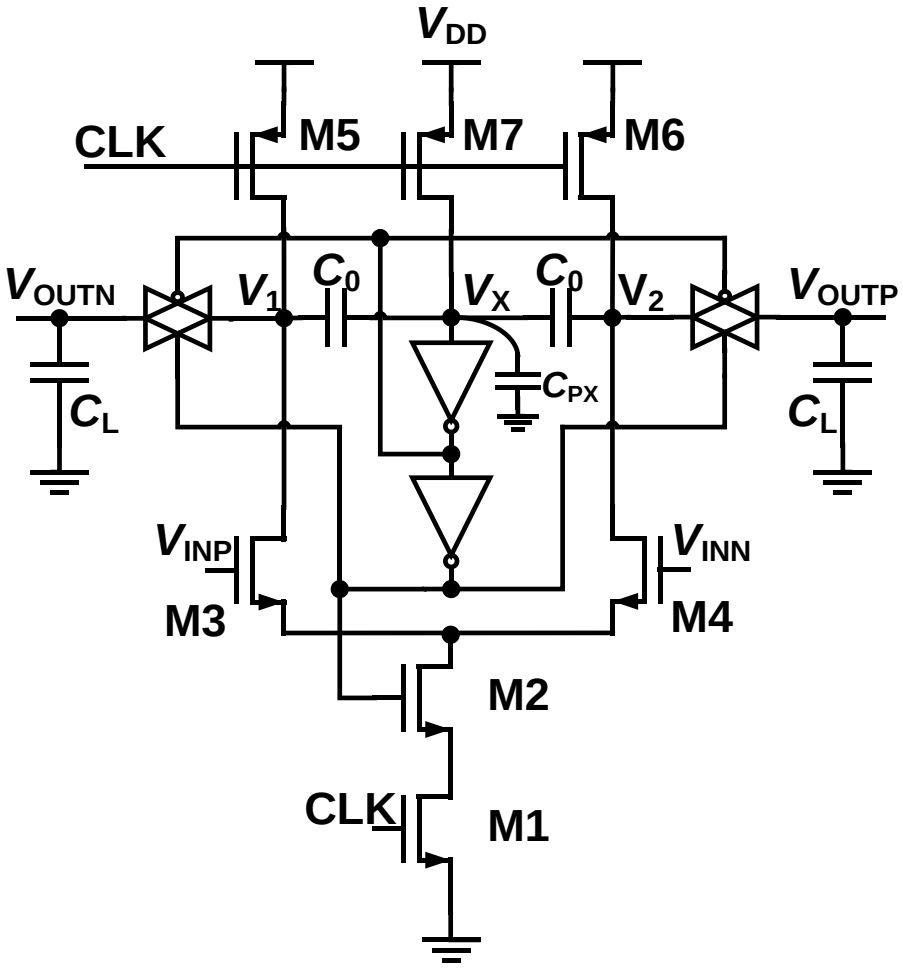


- Wider output signal swing
- Robust to voltage lowering
- Operational at 0.5 V

- Consumes dynamic power
- Clock-scalable

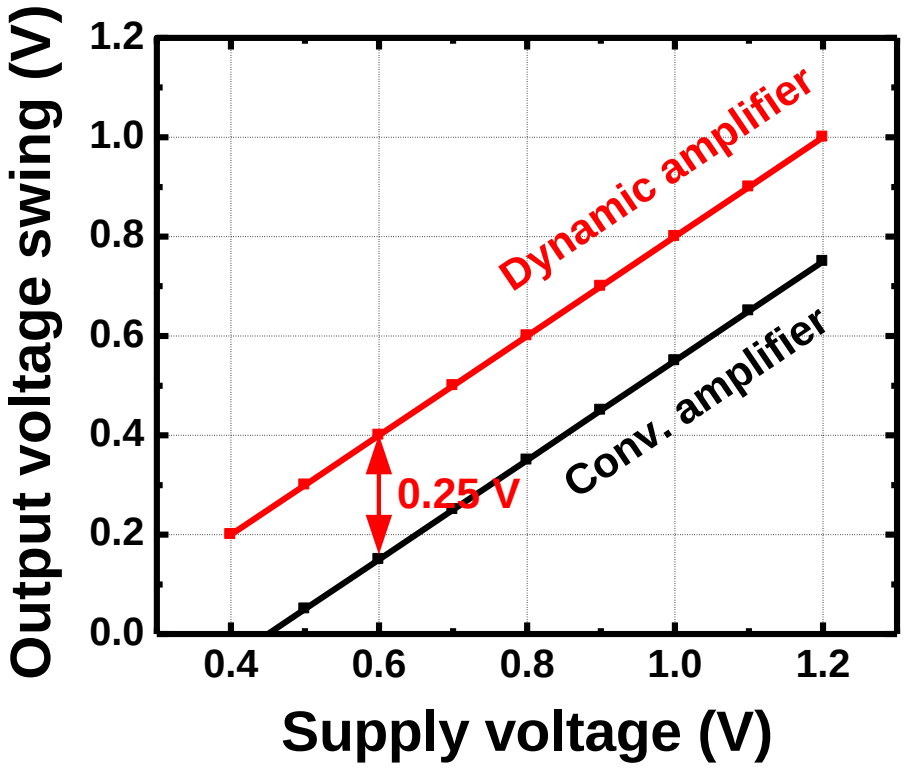
Circuit Implementation

- **CMD implemented in a dynamic amplifier with switches to terminate the discharging**



Conclusion

- **The proposed dynamic amplifier realizes**
  - **0.5 V ultra low voltage operation**
  - **Wider signal swing**
  - **Clock-scalable power consumption**



0.5 V Opportunities

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- **Ultra-low-power electronics**
  - **Mobile applications, ubiquitous wireless sensor systems, and green IT**
- **Ultra-low supply voltage**
  - **Powered by single-junction solar cells [4]**
- **Addressing challenges of future scaled devices**

Future Work

- **Further detail analysis of dynamic amplifiers**
  - **Linearity analysis**
  - **Noise analysis**
  - **Design methodology**
  - **Different topologies**
  - **Calibration techniques**
- **Using dynamic amplifiers to implement a 0.5 V pipeline ADC**

References

[1] International Technology Roadmap for Semiconductors, “2010 update – RF and analog mixed-signal CMOS technology requirements,” Dec. 2009.

[2] A. Matsuzawa, “An ultra low power analog and ADC design,” ISSCC Forum, Feb. 2011.

[3] B. Razavi, “Design of analog CMOS integrated circuits,” McGraw-Hill, 2001.

[4] B. Kayes, H. Atwater, and N. Lewis, “Comparison of the device physics principles of planar and radial p-n junction nanorod solar cells,” Journal of Applied Physics, vol. 97, 2005.

[5] M. Miyahara, H. Lee, D. Paik, and A. Matsuzawa, “A 10b 320 MS/s 40 mW open-loop interpolated pipeline ADC,” in IEEE Symposium on VLSI Circuits Digest of Technical Papers, pp. 126-127, 2011.

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Thank you for your attention.