A High-Speed Clock-Scalable Dynamic Amplifier for Mixed-Signal Applications

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1. Introduction

One of the main building blocks for electronics is an amplifier. However, conventional amplifiers consume static power and have a narrow output signal range with reduced supply voltage. For mixed-signal applications, an effective method to lower this power consumption is to remove the unnecessary static current by switching to dynamic operation [1]. Conventionally, dynamic amplifiers are often used as pre-amplifiers for dynamic comparators to reduce noise [2]. The lack of techniques to provide a linear gain and stable output signals renders dynamic amplifiers unusable as a single-stage amplifier.

In this paper, a common-mode detection technique is proposed to realize a single-stage differential dynamic amplifier. This architecture is suitable for high-speed and low-power mixed-signal applications. Furthermore, it is very robust to supply voltage lowering. A prototype of this circuit is designed and simulated in 90 nm CMOS technology.

2. Circuit Design and Implementation

The proposed dynamic amplifier functions as a single-stage amplifier with its operation waveform shown in Figure 1. The termination of discharging time of the load capacitors is realized with some inverters, sampling capacitors and switches as shown in Figure 2. The two sampling capacitors, C_0, average the voltages at V_1 and V_2 and triggers the inverter connected to V_X when the output common-mode voltage crosses the inverter's threshold. Similar to conventional dynamic amplifiers, the proposed circuit uses a minimally stacked architecture as M1, M2, and M5-8 all act as switches. As a result, this architecture provides a superior output signal swing in comparison to conventional static amplifiers with active loads and a tail current source [3]. Furthermore, the dynamic nature of this amplifier allows its power consumption to be clock scalable. Therefore, both high-speed and low-power applications can be realized using the same circuit.

Simulation results show the proposed design operating up to 1.5 GHz with a gain of 15.5 dB covering an output signal swing of 1.3 V_{P-P} with less than 1 dB drop in gain as shown in Figure 3.

3. Conclusion

A single-stage, high-speed and clock-scalable dynamic amplifier using a common-mode voltage detection technique is proposed. Its performance is summarized in Table 1.

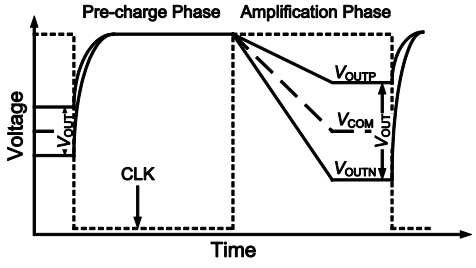

Figure 1: Operation waveform of the proposed dynamic amplifier.

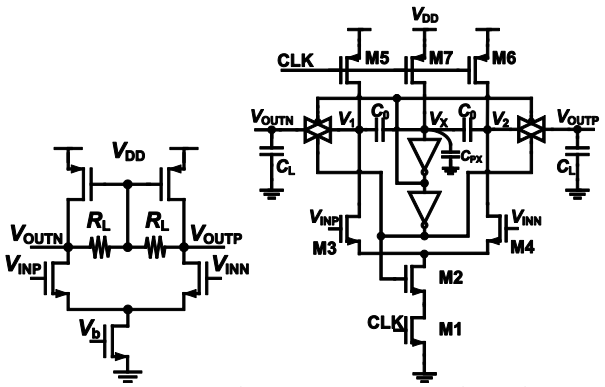

Figure 2: The schematics of the conventional amplifier (left) and the proposed dynamic amplifier with an inverter-based common-mode voltage detector located in its centre (right).

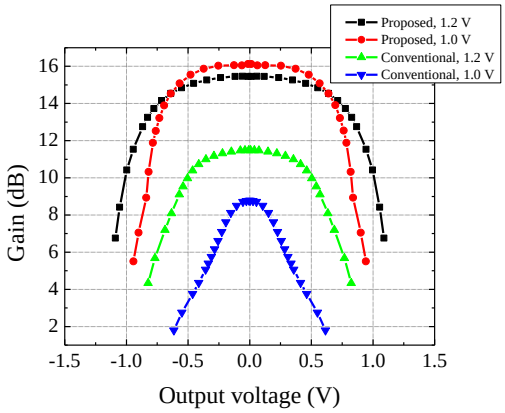

Figure 3: Simulation results show the proposed design offers a wider signal swing and is less sensitive to supply voltage lowering than the conventional design. The simulation conditions are $V_{DD}/2$ input common-mode voltage with 100 fF load capacitance for the proposed design operating at 1.5 GHz.

TABLE 1: PERFORMANCE SUMMARY

Freq. [GHz]	Gain [dB]	Supply [V]	Power Dissipation [mW]	Load Cap. [fF]	Process
1.5	15.5	1.2	1.05	100	90 nm CMOS

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