シャントシリーズピーキングによるミリ波帯広帯域周波数分周器

A Wide Frequency Range 60GHz Static Frequency Divider Using Shunt-Series Peaking

シリブラーノン　ティーラショート　Teerachot Siriburanon
ウェイ　デン　Wei Deng
岡田 健一　Kenichi Okada
松澤 昭　Akira Matsuzawa

東京工業大学大学院理工学研究科電子物理工学専攻
Department of Physical Electronics, Tokyo Institute of Technology

1. Introduction

Increasing demand for high speed data transmission attracts interests for utilizing the 7-GHz unlicensed band around 60GHz. In these system applications, one of the most critical components is frequency divider which operates at the highest speed.

Conventionally, static divider, regenerative (Miller) frequency divider and injection-locked frequency divider (ILFD) are the most popular architectures. Even though ILFDs and Miller divider normally have the higher operational speed, they are not suitable for wideband applications. Therefore, a static frequency divider is used since it has a relatively wider operational frequency range.

2. Proposed Architecture

In a conventional approach, using shunt peaking for high-speed Current Mode Logic (CML) frequency divider, an inductor is placed at drain of transistors where inductor's parasitic capacitance adds up to drain capacitance. Consequently, the time constant increases and thus, reduces the speed. By exchanging the position of the resistor and inductor introducing an architecture used in [1], maximum bandwidth can be achieved.

An even larger bandwidth extension can be expected by inserting a series inductor at the drain node of the first-latch to the drain node of the cross-coupled pair latch. This series inductor will separate the loading of parasitic capacitance of these two latches i.e. only parasitic capacitance of the first latch is initially charged because series inductor delays current to flow to the rest of the circuit. Thereby, this minimizes risetime at the drain and increases bandwidth [2]. This proposed architecture combines a modified shunt peaking and series peaking called shunt-series inductive peaking. This can provide improvement in bandwidth enhancement than the method proposed in [1].

3. Simulation Results

The simulated maximum operating frequency of the proposed architecture (shunt-series peaking) and conventional architecture (shunt peaking) are shown in Fig.1. In case of employing conventional architecture, the maximum operating frequency range of divide-by-2 frequency divider under 0 dBm input power is approximately 85 GHz in its optimum case utilizing a shunt inductance of 400 pH. On the other hand, employing the proposed architecture with a series inductance of 100 pH, the proposed divider can operate up to 86.5 GHz when utilizing shunt inductance of about 200 pH.

Fig. 2. shows the operating frequency range of the proposed and conventional architecture. For the conventional shunt peaking, operating frequency range of the divider is 40 GHz when the shunt inductance is about 400 pH. In case of utilizing the proposed architecture with a series inductance of 100 pH, operating frequency range of the proposed divider is 53 GHz. Therefore, by employing shunt-series peaking, an improvement of 13GHz (32.5%) in operating frequency range can be observed.

4. Conclusion

Comparing to the case of employing only conventional shunt peaking, a shunt-series architecture utilized in a frequency divider can increase operating frequency range by 32.5%.

Acknowledgements

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References

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[2] S. Shekhar, J.S. Walling, and D.J. Allstot, "Bandwidth Extension Techniques for CMOS Amplifiers", *JSSC*, Nov. 2006.

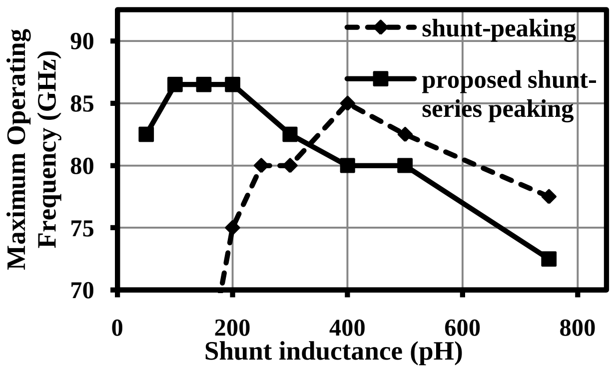

Fig. 1. Maximum Operating Frequency of a 2:1 frequency divider utilizing shunt peaking and shunt-series peaking at different shunt inductance

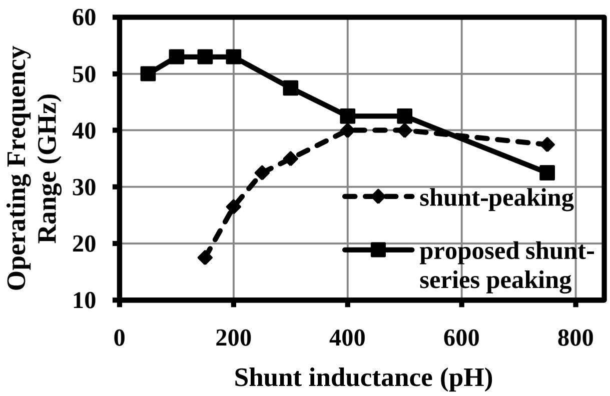

Fig. 2. Operating frequency range of a 2:1 frequency divider utilizing shunt peaking and shunt-series peaking at different shunt inductance