

IEICE Society Conference

**TOKYO TECH**  
Pursuing Excellence

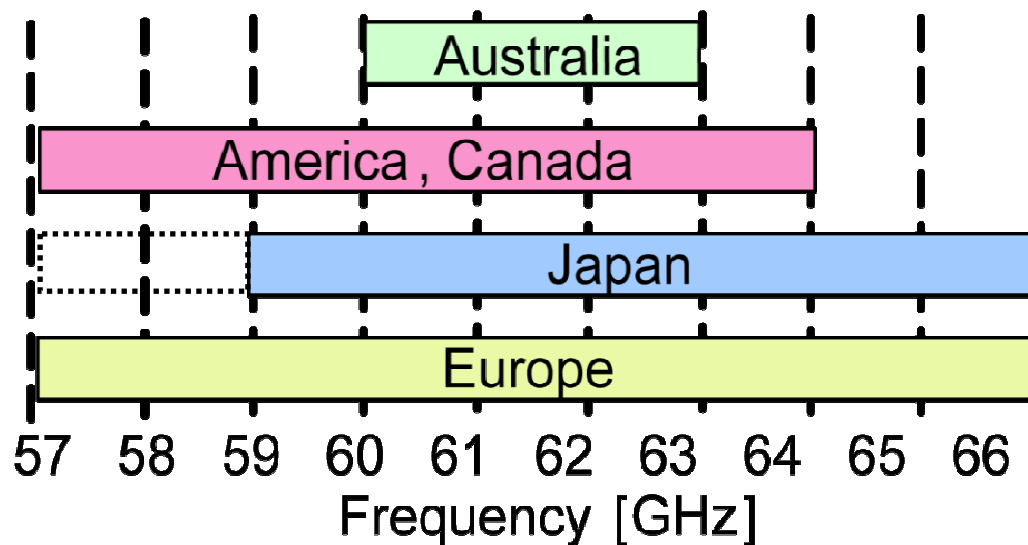
# A 60-GHz Digitally-Controlled Phase Modulator with Phase Error Calibration

**Rui WU, Ning Li, Kenichi Okada,  
and Akira Matsuzawa  
Tokyo Institute of Technology**



# Background

- 9-GHz unlicensed bandwidth
- Several Gbps wireless communication  
e.g. IEEE 802.15.3c  
QPSK → 3.5 Gbps/ch  
16QAM → 7 Gbps/ch

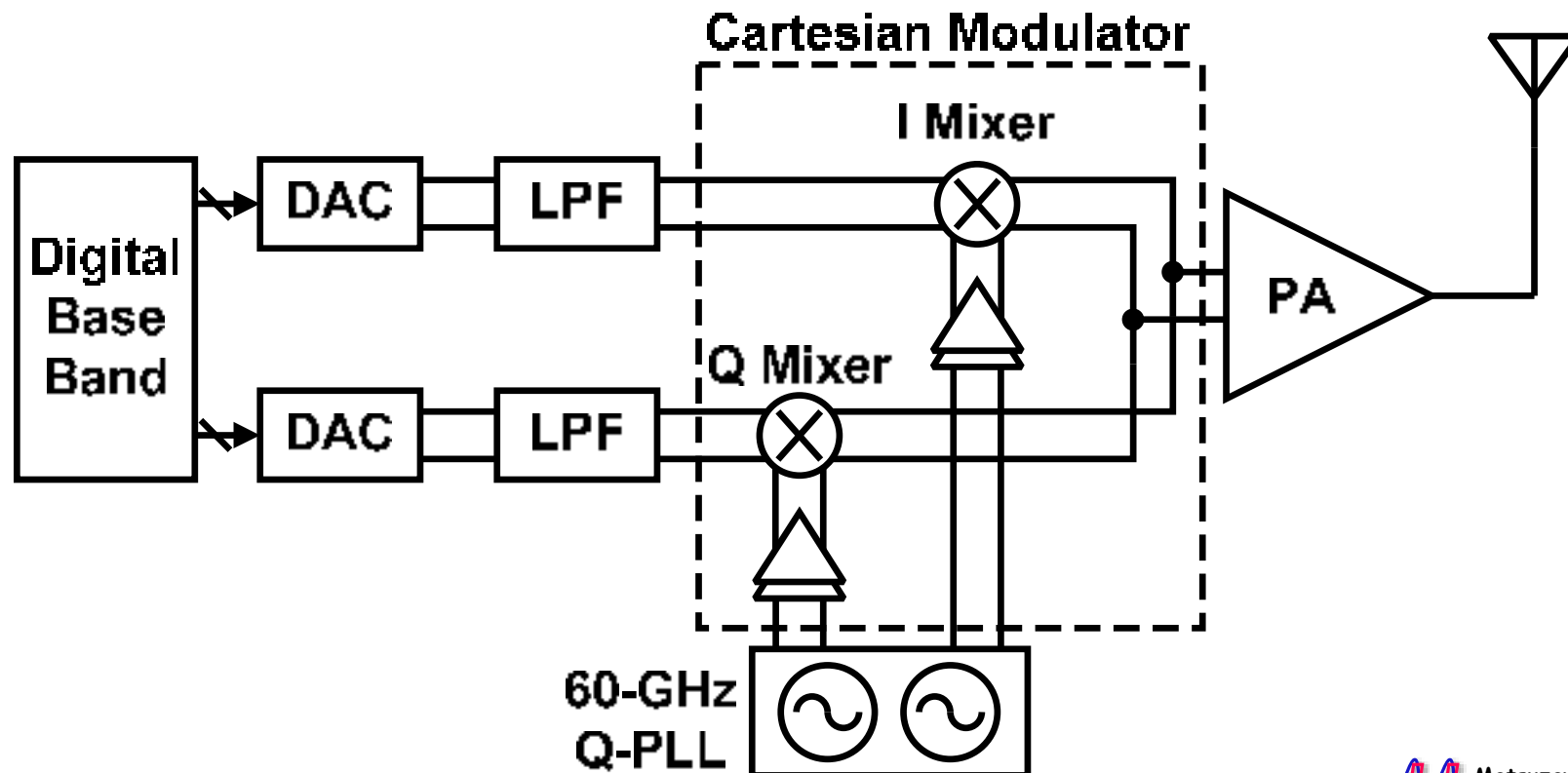


[1] <http://www.tele.soumu.go.jp>

# Conventional 60-GHz Transmitter

2

- Direct-conversion architecture
  - Small area
  - Low power consumption
  - Free of imagine frequency issue



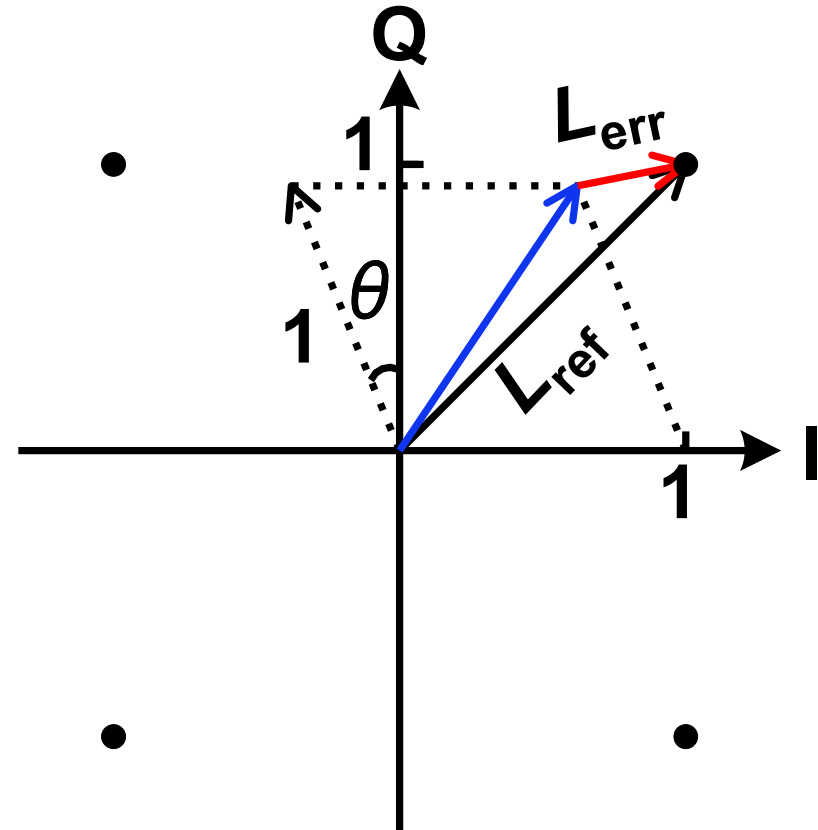
- I/Q phase mismatch

$$EVM(\%) = \frac{L_{err}}{L_{ref}} \times 100\%$$

For  $\theta = 10^\circ$

Phase error =  $5^\circ$

$EVM(\%) \approx 12.7\%$



QPSK Constellation

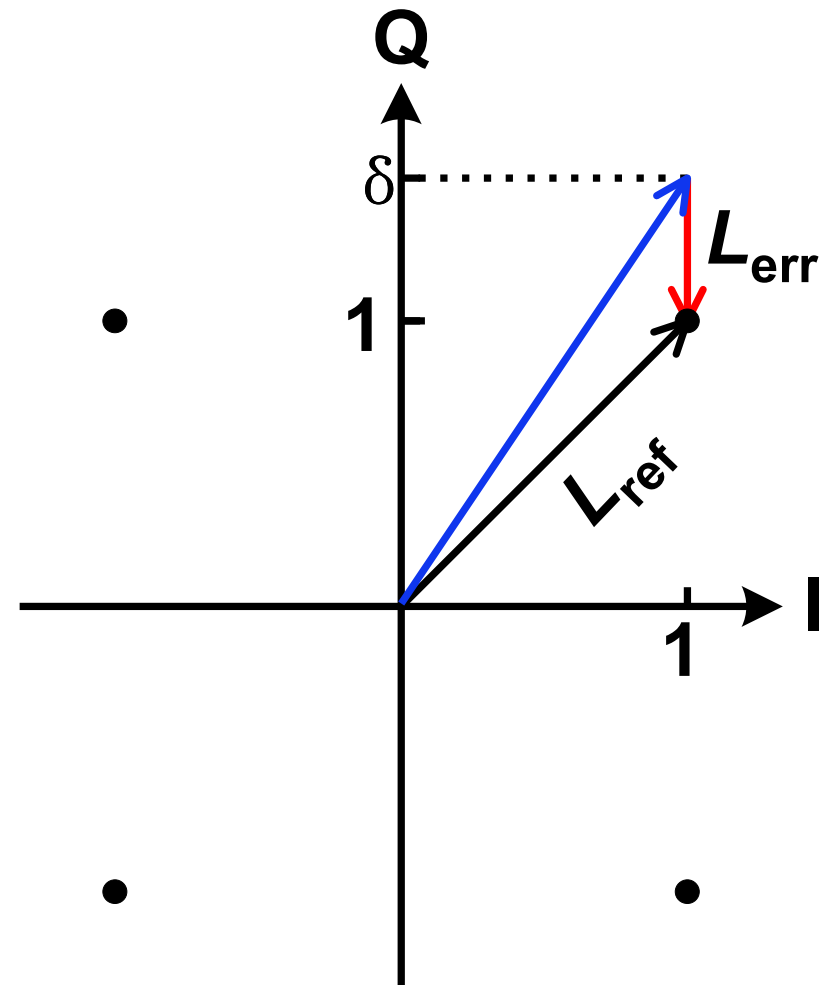
- I/Q gain mismatch

$$EVM(\%) = \frac{L_{err}}{L_{ref}} \times 100\%$$

For  $20 \log_{10} \delta = 1 \text{ dB}$

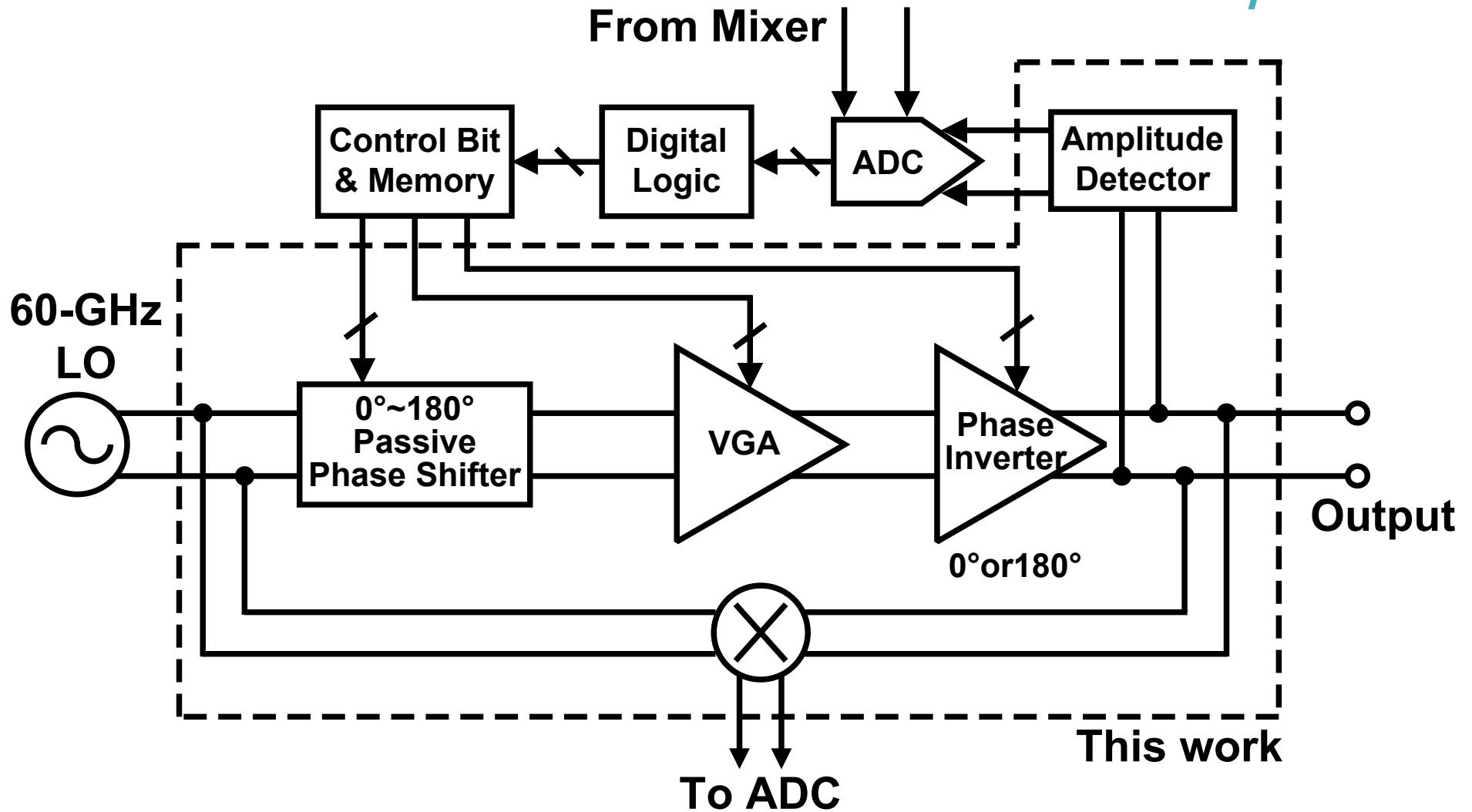
Phase error  $\approx 3^\circ$

$EVM(\%) \approx 8.6\%$

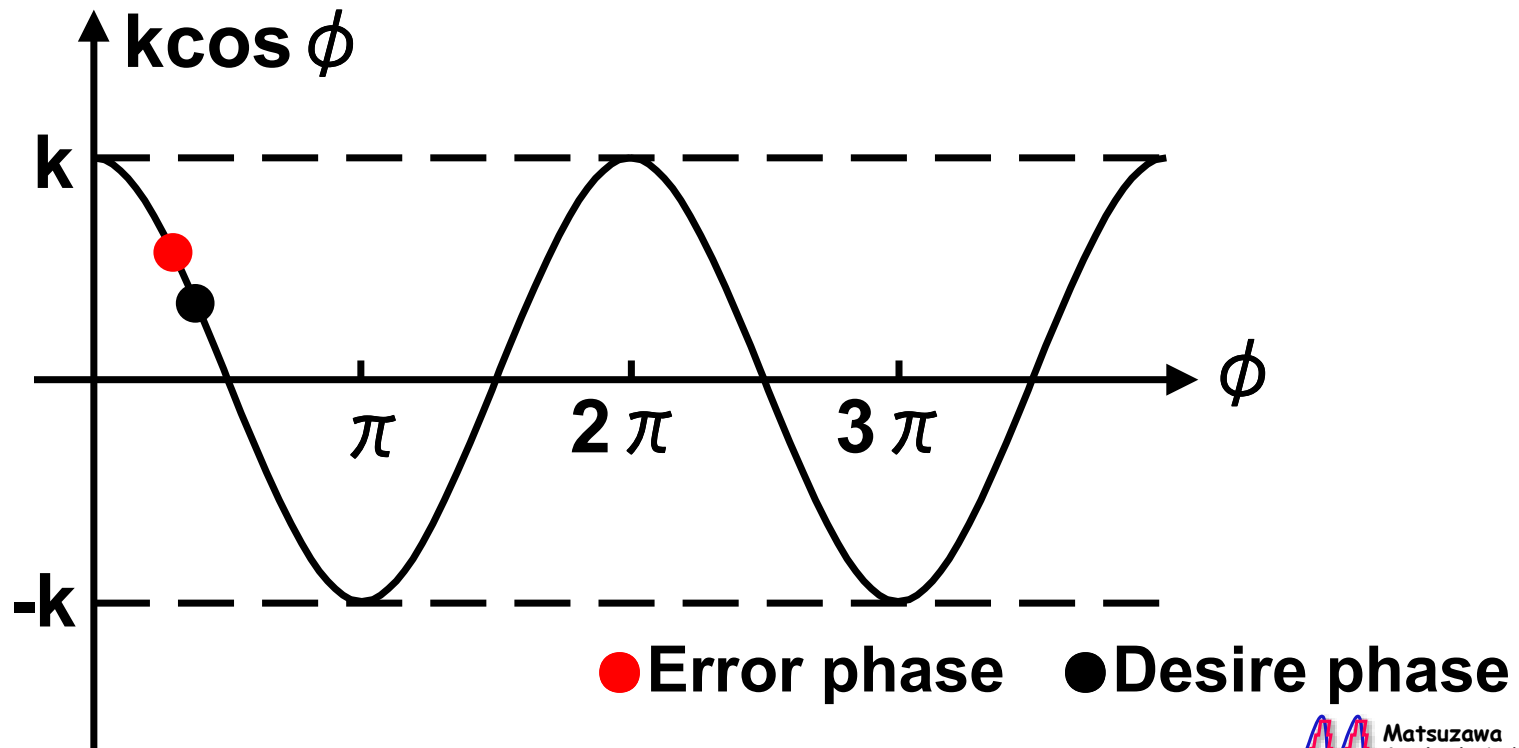
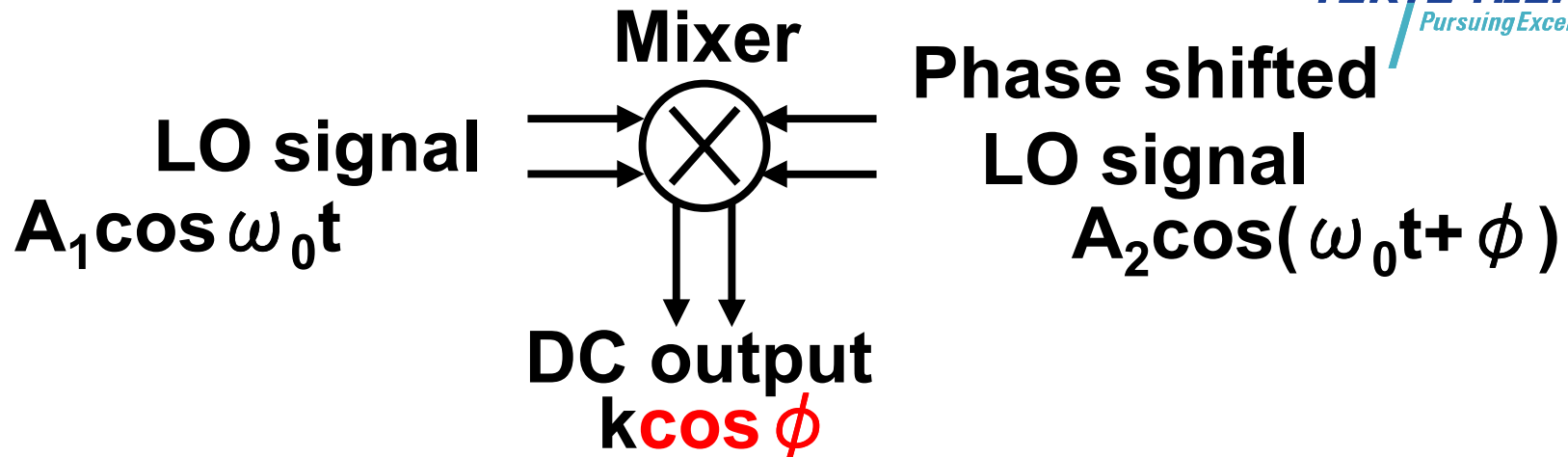


QPSK Constellation

# Proposed Phase Modulator



# Phase Calibration Principle (1/2)



- Insensitivity to the phase shift of mixer.

$$P = k \cos(\phi + \Delta \theta)$$

$$\text{Phase 1: } \phi_1 + \Delta \theta = \arccos(P_1/k)$$

$$\text{Phase 2: } \phi_2 + \Delta \theta = \arccos(P_2/k)$$

Phase 2-Phase 1:

$$\phi_2 - \phi_1 = \arccos(P_2/k) - \arccos(P_1/k)$$



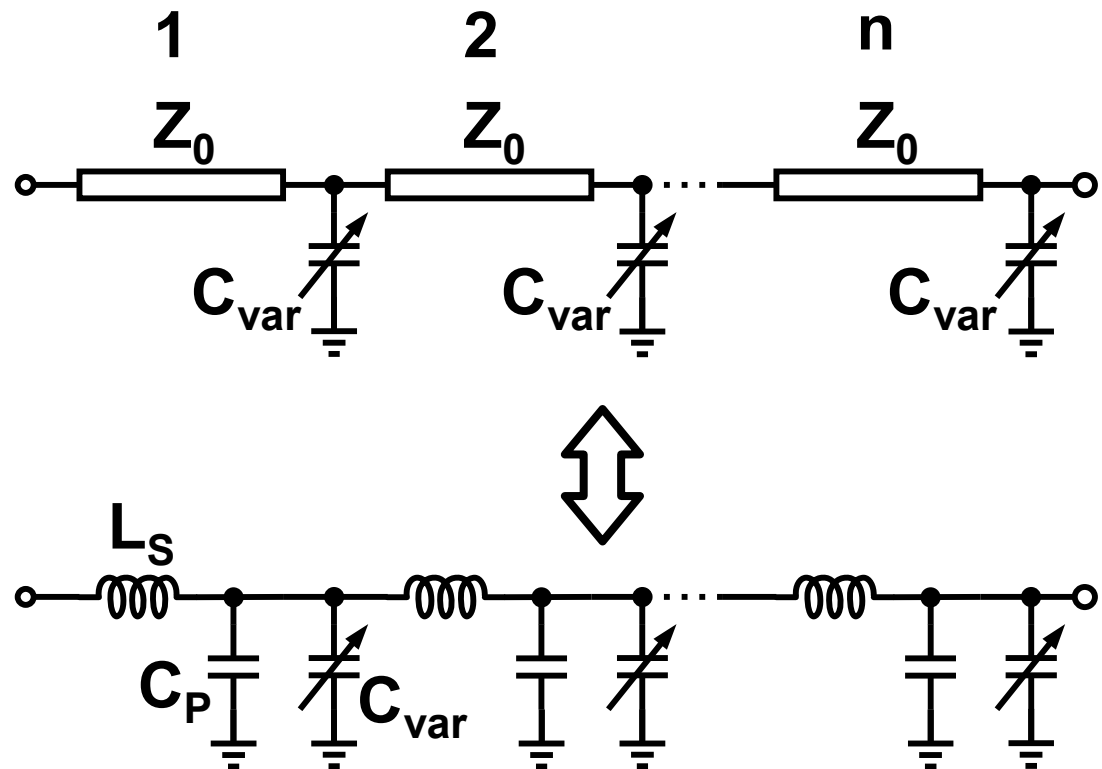
# Varactor-Loaded TL

$$\varphi = \tan^{-1} \left[ \frac{Y_C^2 X_L - 2Y_C - X_L}{2(1 - Y_C X_L)} \right]$$

where

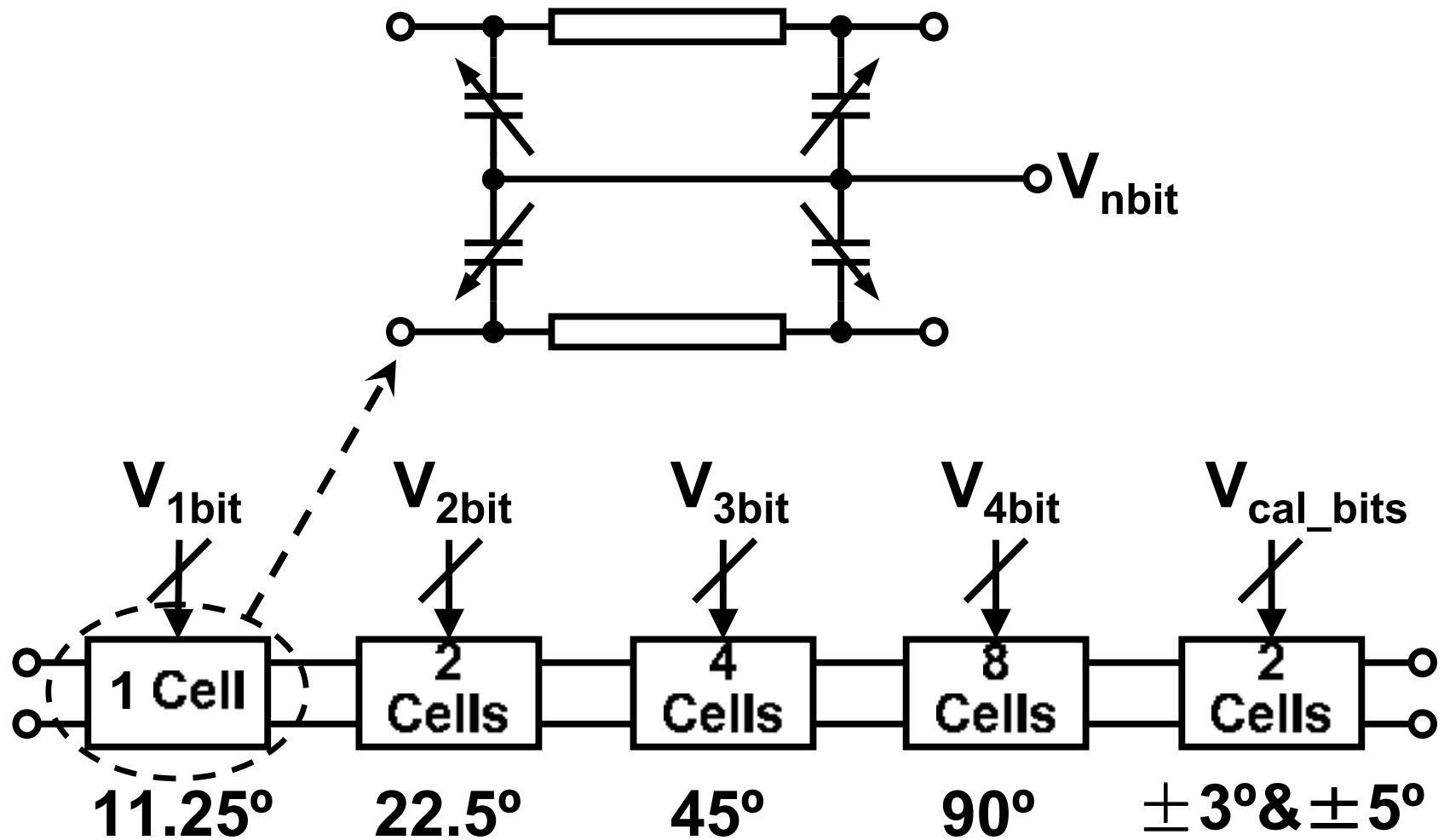
$$Y_C = \frac{1}{2} \omega (C_P + C_{var}) Z_0$$

$$X_L = \frac{\omega L_S}{Z_0}$$

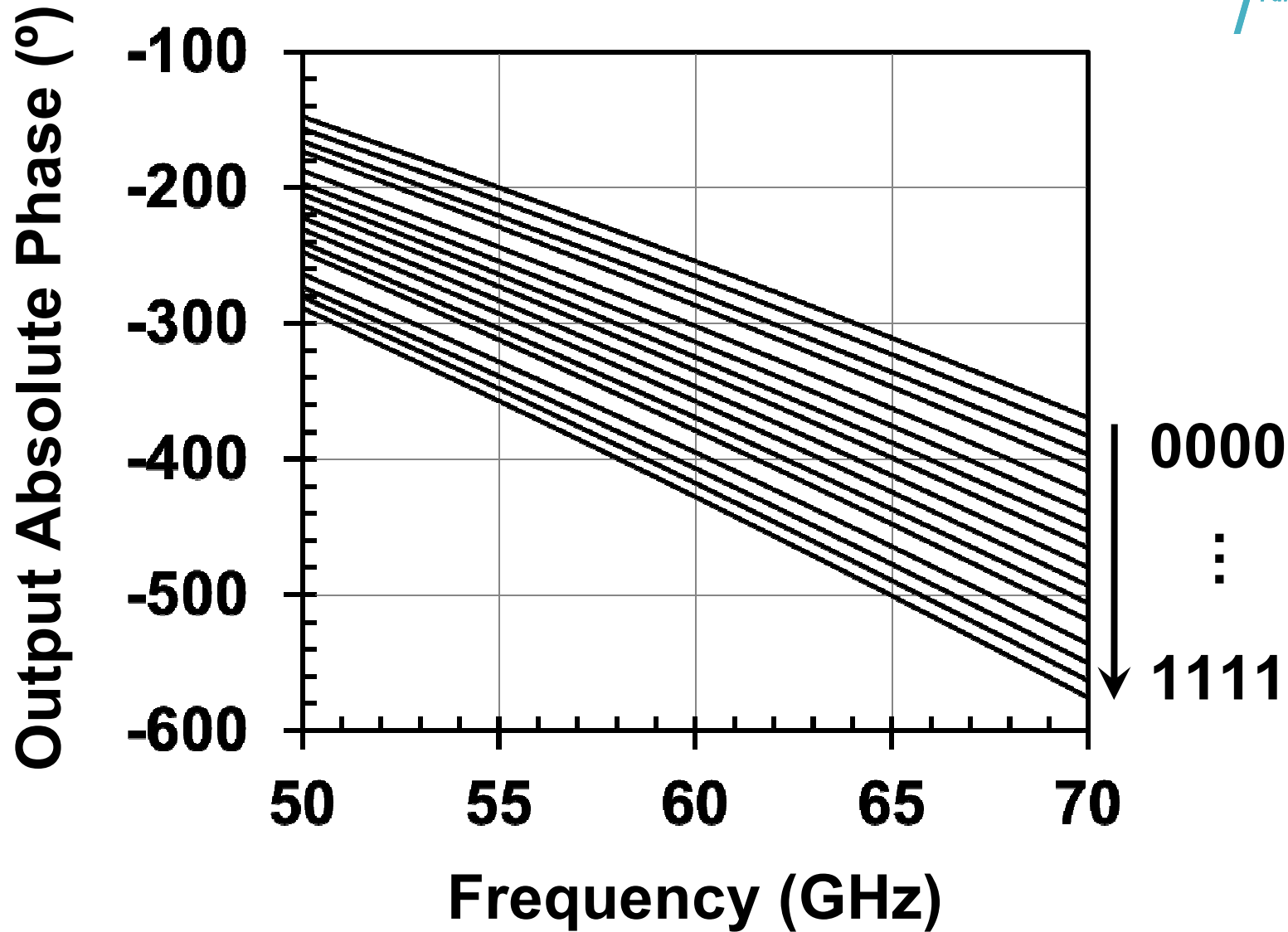


[2] F. Ellinger et. al, TMTT 2003.

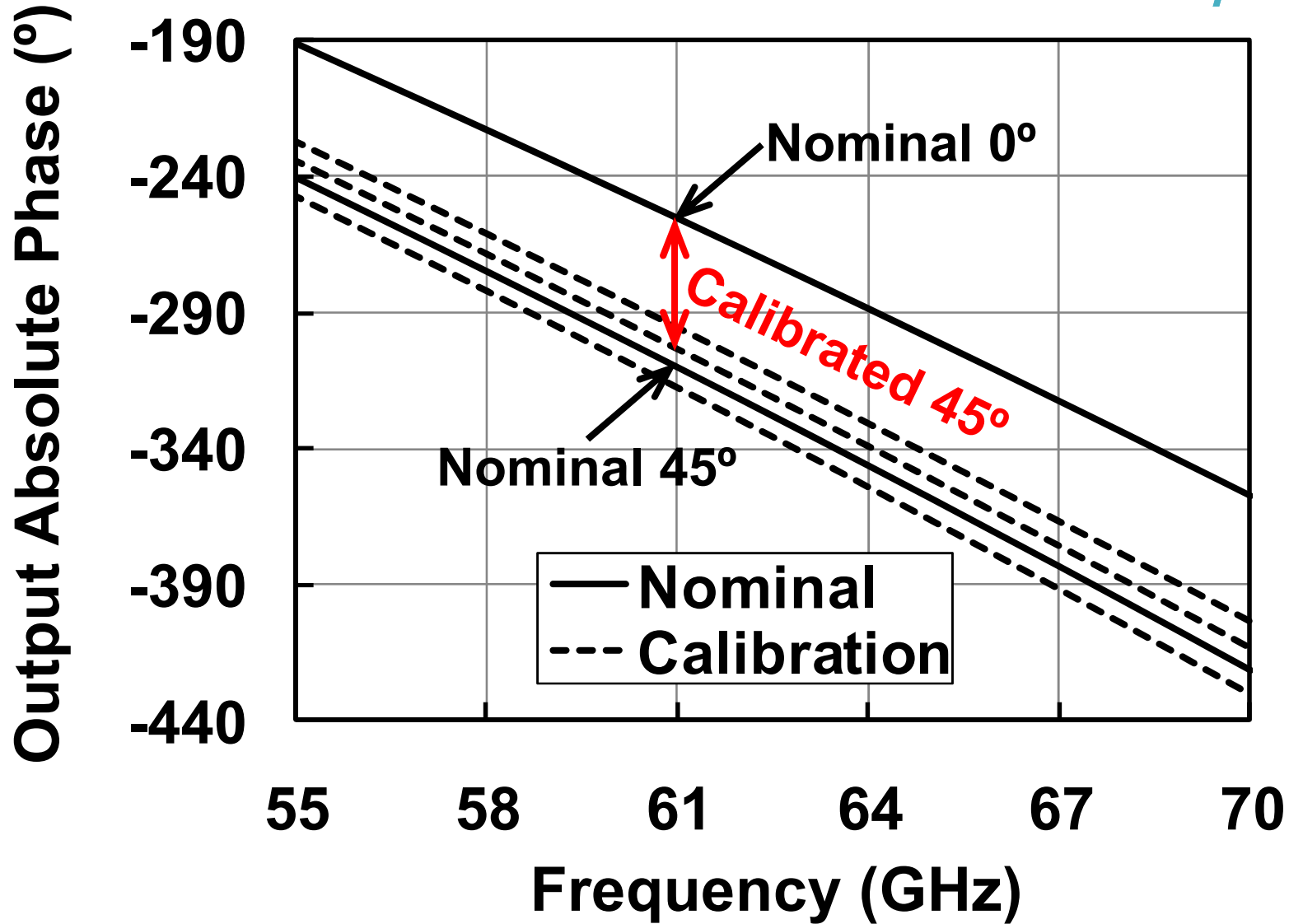
# Phase Shifter Architecture



# Phase Shifter Sim. Result



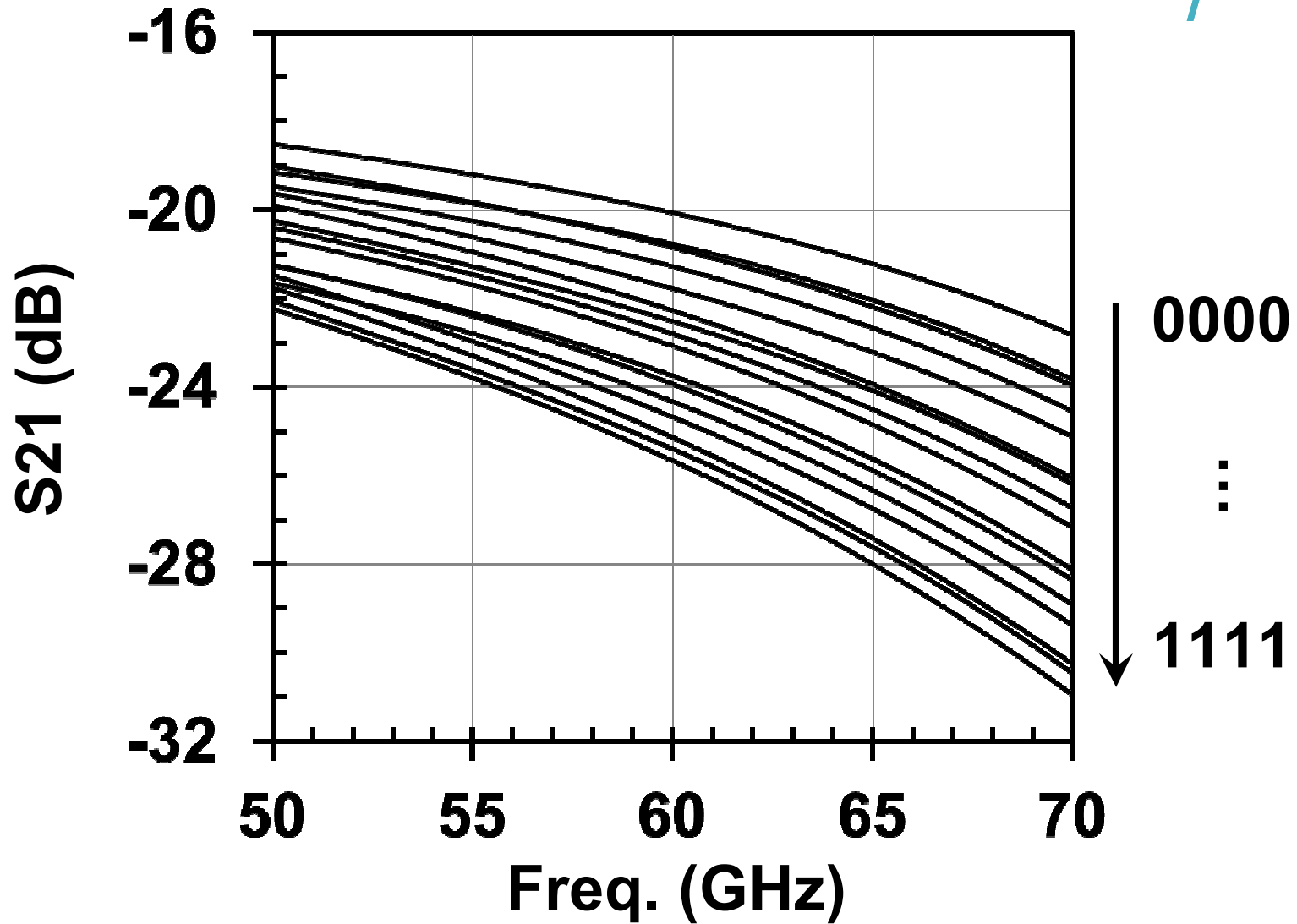
# Phase Shifter Sim. Result



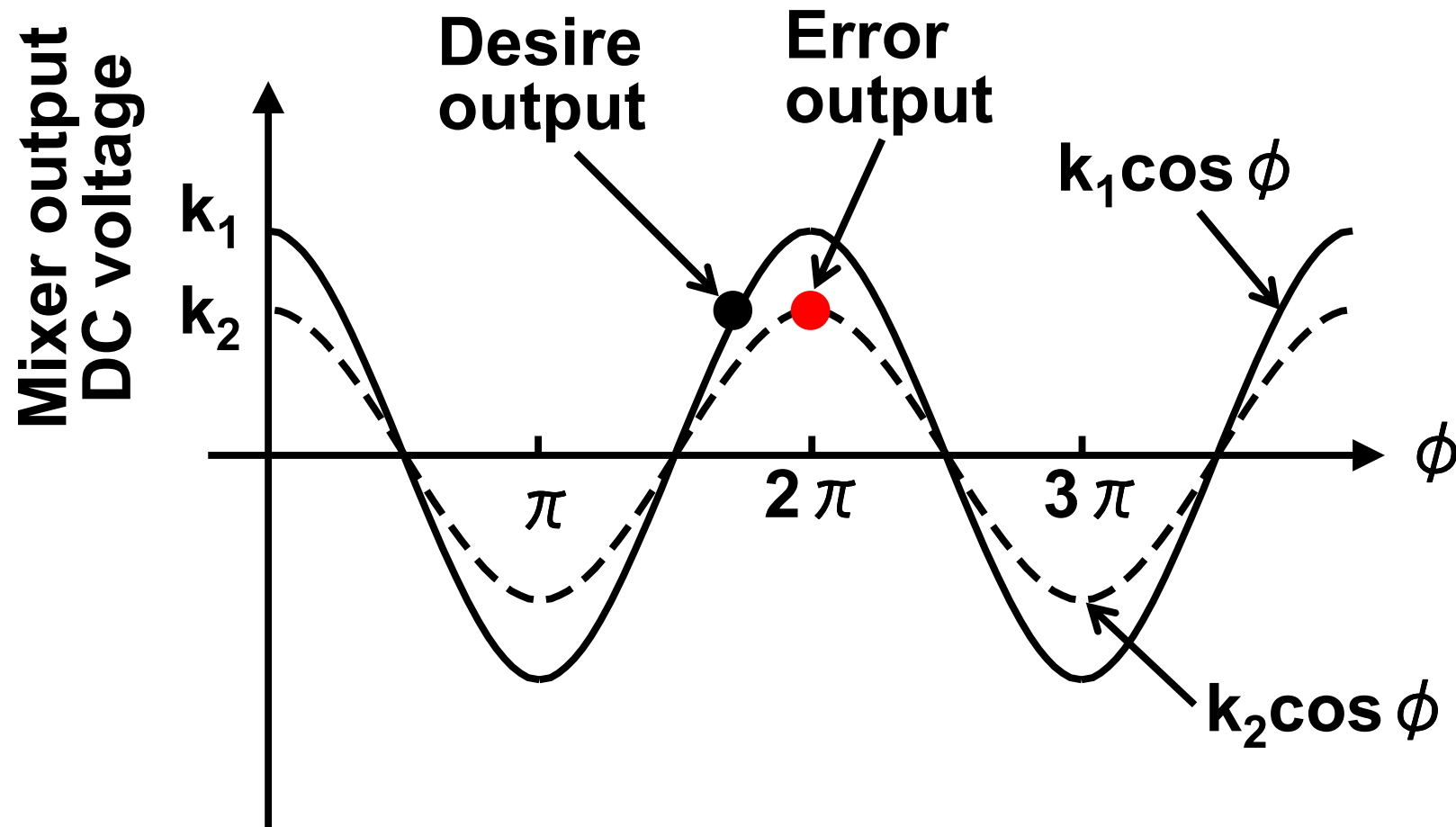
- **The phase accuracy of the modulator will be greatly improved over PVT variations by using the proposed technique.**

**Thank you for your attention!**

# Phase Shifter Loss Variation

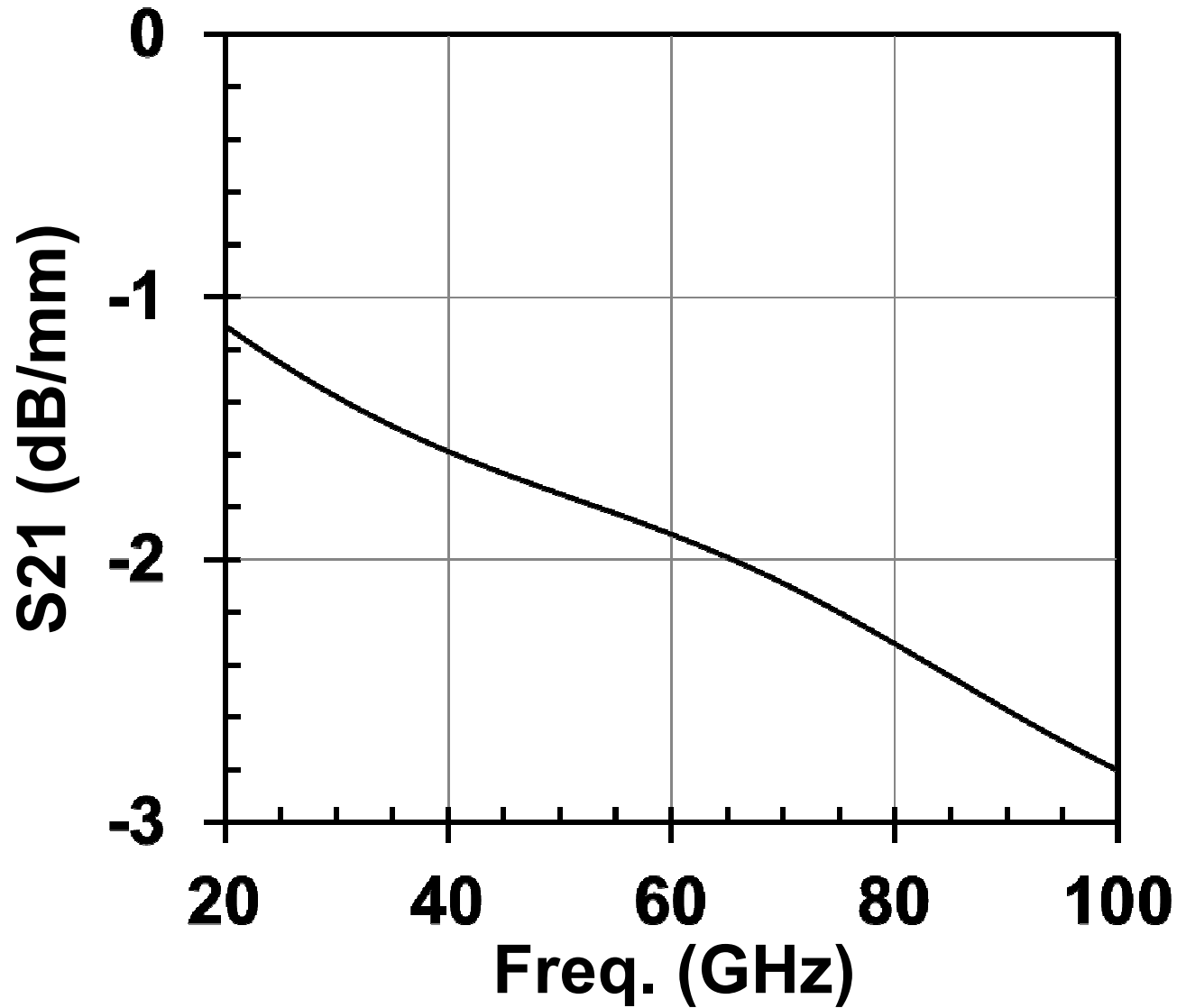


- Calibration error

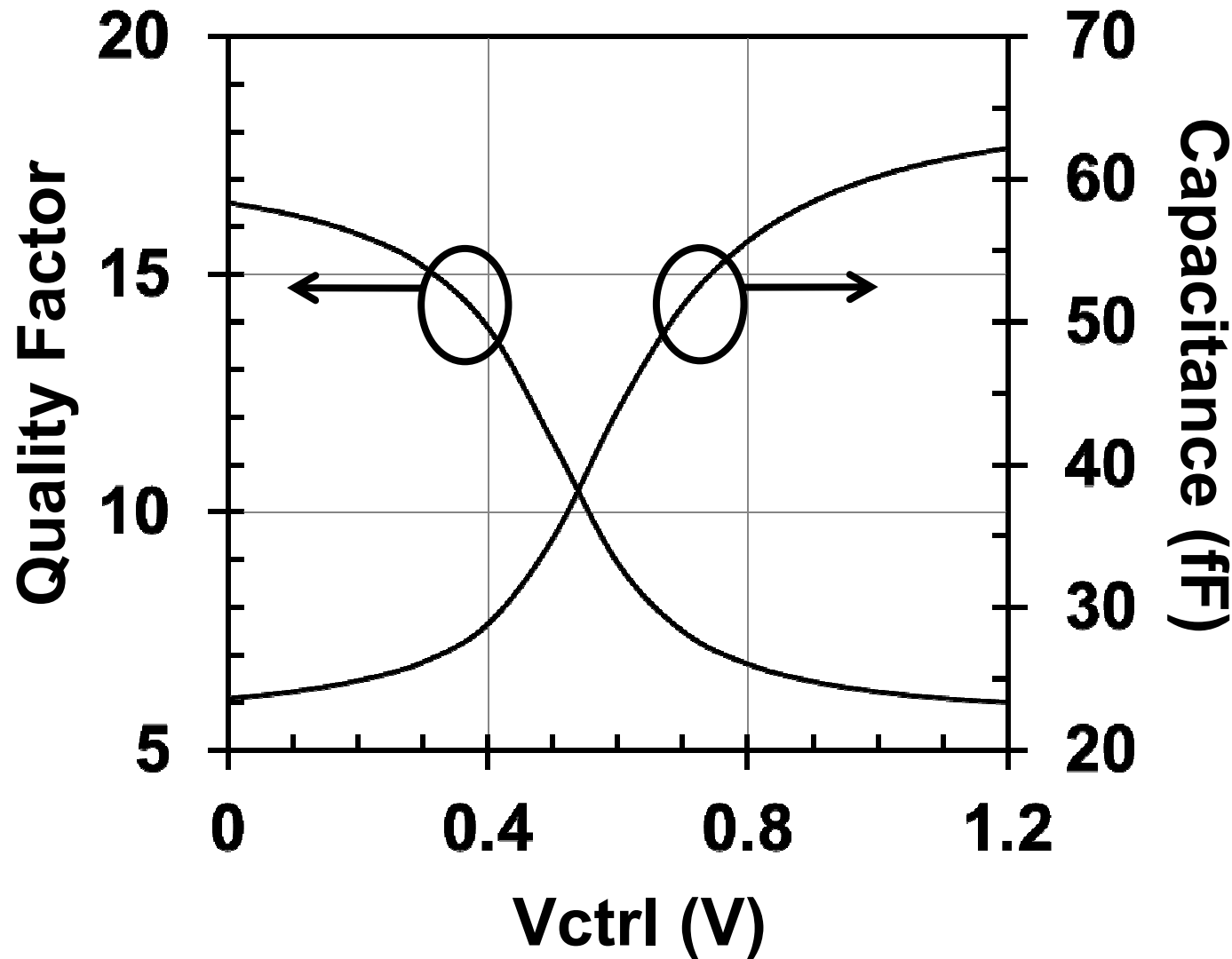




# Transmission Line Loss



# Varactor Quality Factor



Attenuation  
Constant:

$$\alpha \propto \frac{1}{Q^2}$$

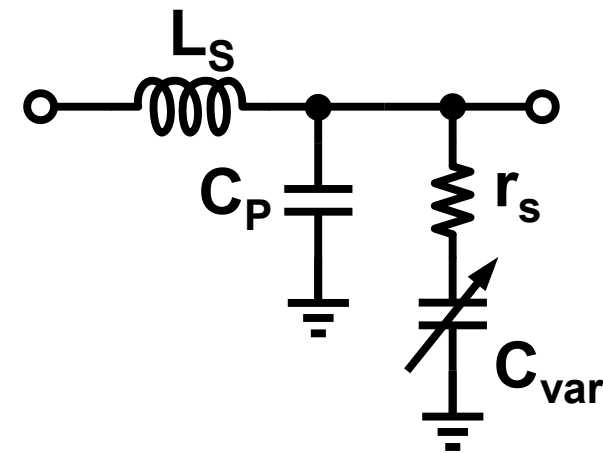
[3] A. S. Nagra et. al, TMTT 1999.

# Loss from Varactor

$$\alpha = (2\pi f) \frac{L_S}{2r_s Q^2 \sqrt{1 - \cos(\beta)^2}}$$

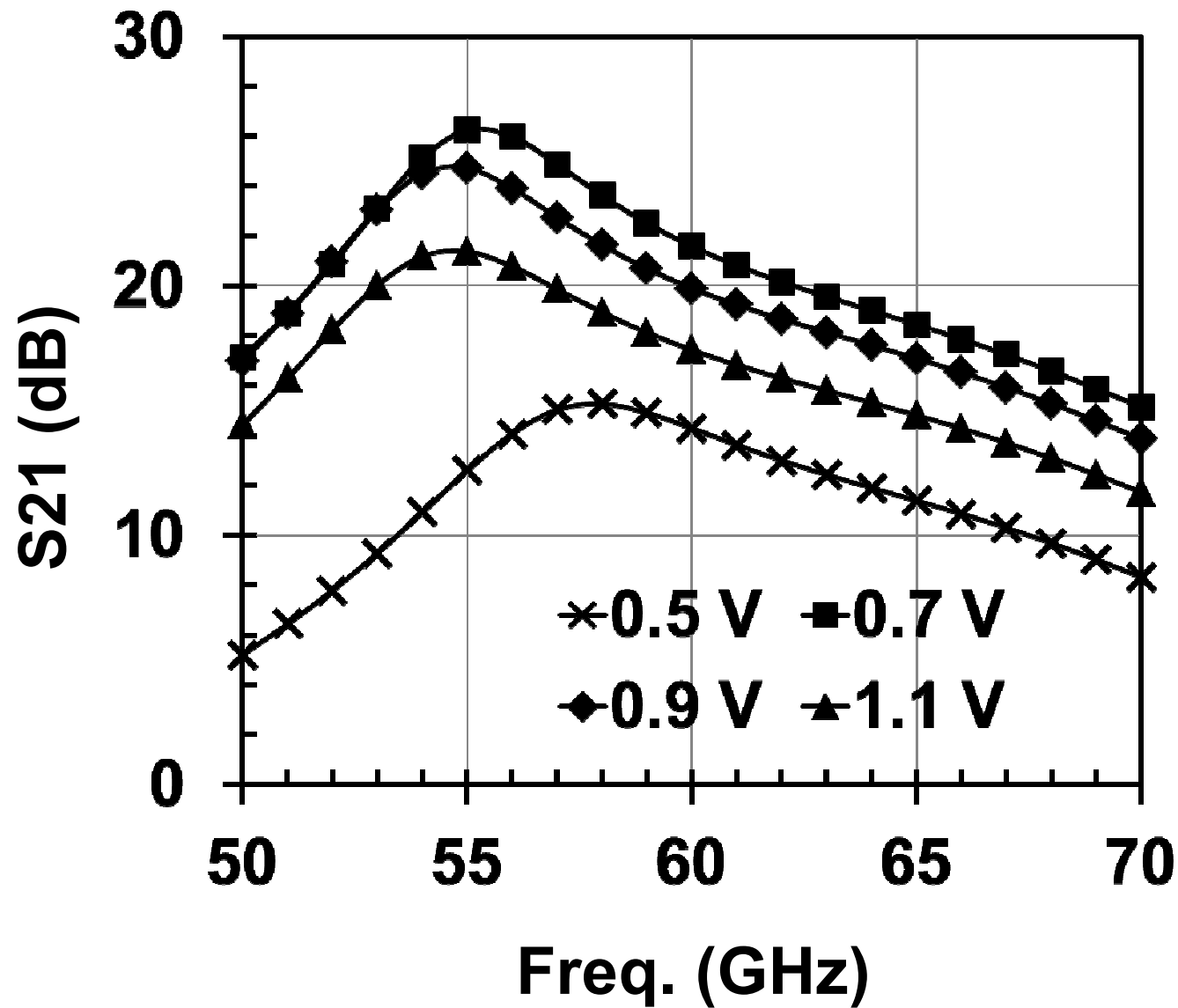
where

$$\cos(\beta) = 1 - (2\pi f)^2 \frac{L_S (C_P + C_{var})}{2}$$



[3]A. S. Nagra et. al, TMTT 1999.

# Variable Gain Amplifier (Sim.)



- **High Speed Interface Mode**

| <b>Data rate</b>            | <b>EVM (dB)</b> | <b>EVM (%)</b> |
|-----------------------------|-----------------|----------------|
| <b>Up to 1.5Gb/s</b>        | <b>-7</b>       | <b>45%</b>     |
| <b>2.1Gb/s to 2.7 Gb/s</b>  | <b>-14</b>      | <b>20%</b>     |
| <b>2.8 Gb/s to 5.3 Gb/s</b> | <b>-21</b>      | <b>9%</b>      |
| <b>Above 5.4 Gb/s</b>       | <b>-23</b>      | <b>7%</b>      |

# Performance Comparison

21

| 60 GHz     | [4]                   | [5]                       | [6]                         | This work (Aim)       |
|------------|-----------------------|---------------------------|-----------------------------|-----------------------|
| EVM        | 9.5%                  | 6%                        | 12%                         | 6%                    |
| Modulation | $\pi/4$ DQPSK         | QPSK                      | QPSK                        | QPSK                  |
| Bandwidth  | 20 MHz                | 20 MHz                    | 1 MHz                       | 1.7 GHz               |
| Topology   | Modified Gilbert-cell | Sub-harmonic Gilbert-cell | Fundamental Reflection-type | Direct Phase Shifting |
| Process    | CMOS                  | CMOS                      | GaAs HBT                    | CMOS                  |

[4] J.-H. Tsai, TMTT 2011.

[5] J.-H. Tsai et. al, TMTT 2007.

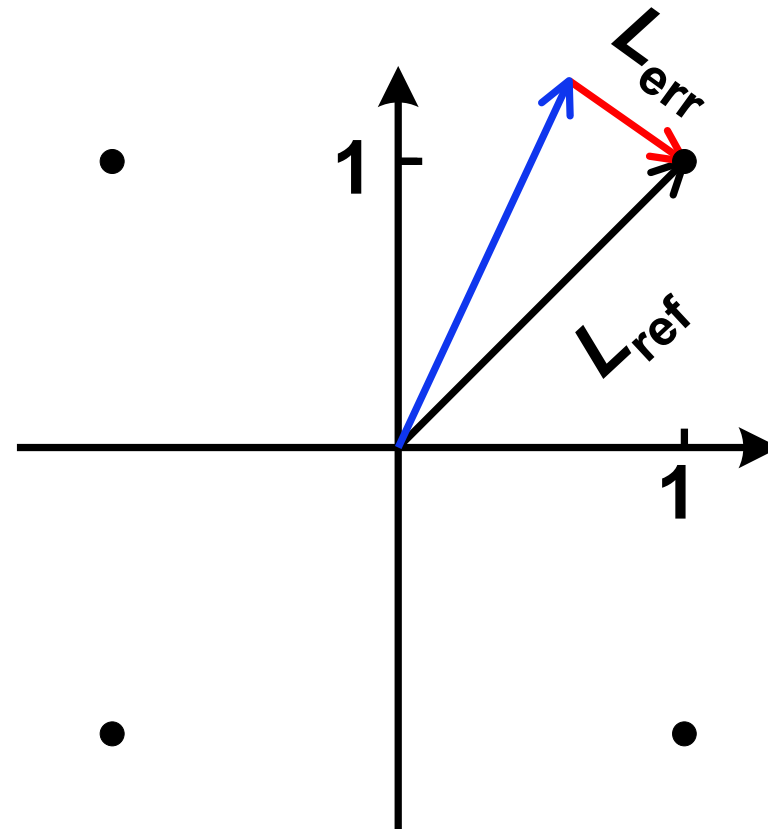
[6] H.-Y. Chang, TMTT 2004.

# Direct Phase Modulation

$$EVM(\%) = \frac{L_{err}}{L_{ref}} \times 100\%$$

Phase error = 3°

$EVM(\%) \approx 5.2\%$



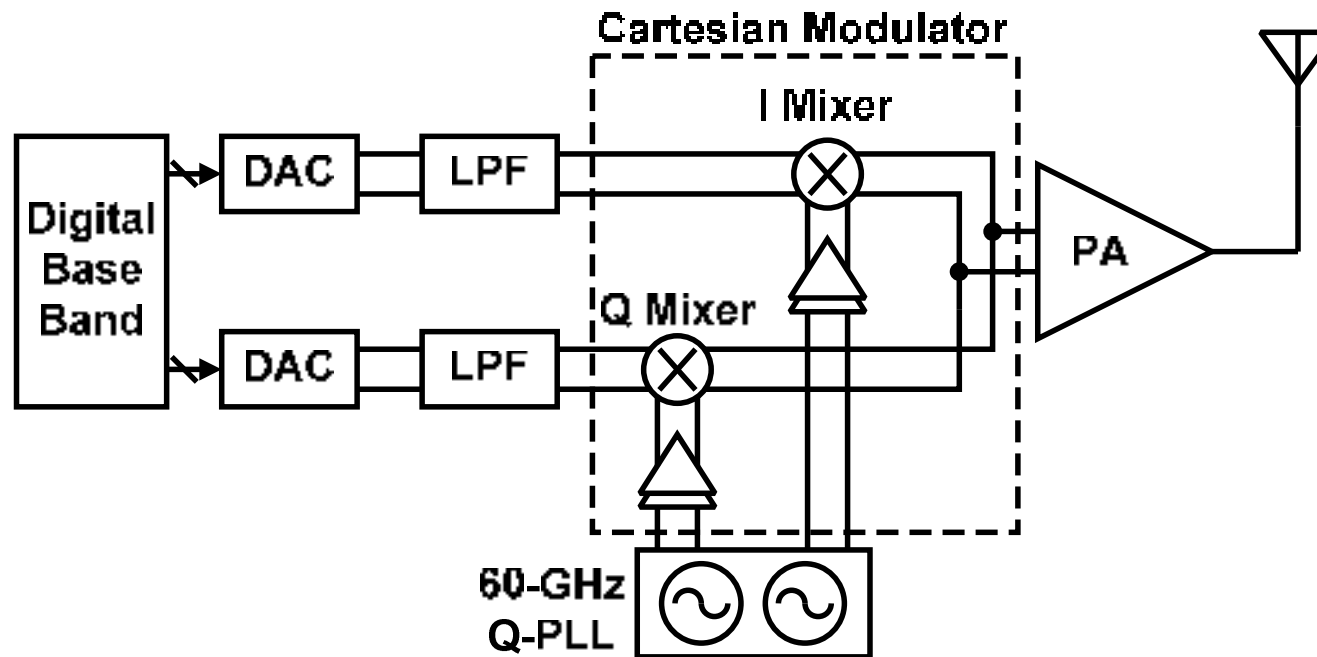
QPSK Constellation

# Power Consumption

|                  | <b>Phase shifter</b> | <b>Phase inverter</b> | <b>Mixer + Amplitude detector</b> |
|------------------|----------------------|-----------------------|-----------------------------------|
| <b>This work</b> | <b>0 mW</b>          | <b>11.5 mW</b>        | <b>7.7 mW</b>                     |



| Pros   | Cons   |
|--|--|
| <ul style="list-style-type: none"><li>➤ Small area</li><li>➤ Low power consumption</li><li>➤ Free of imagine frequency issue</li></ul> | <ul style="list-style-type: none"><li>➤ High linearity PA is required</li><li>➤ Low Power Added Efficiency (PAE)</li><li>➤ High performance 60-GHz Q-PLL is needed</li></ul> |

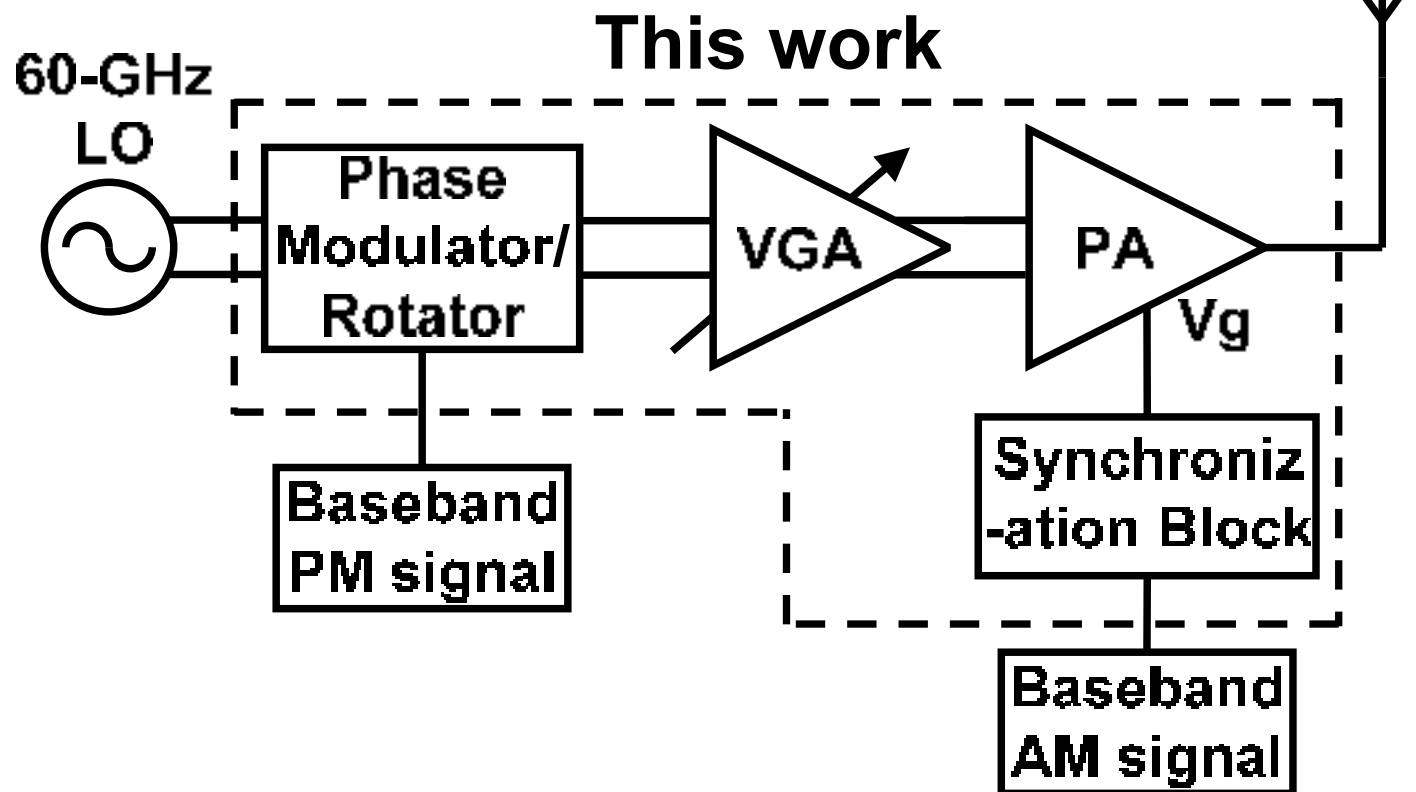


## Direct-Conversion Architecture

# Proposed Polar Tx Block Diagram

25

TOKYO TECH  
Pursuing Excellence



- ☺ PAE can be improved for a wide output power range
- ☺ Gate injection is suitable for wideband (several GHz) AM signal

| <b>Blocks (state)</b>                       | <b>Design Considerations</b>   |
|---|--|
| <b>PA<br/>(designing)</b>                   | <ul style="list-style-type: none"><li>➤ Capable for wideband AM injection</li><li>➤ High peak PAE (&gt; 15%)</li><li>➤ Saturation output power &gt; 10 dBm</li></ul> |
| <b>VGA<br/>(designing)</b>                  | <ul style="list-style-type: none"><li>➤ Gain tuning range of 5dB~10dB</li><li>➤ Small phase shift variation with gain tuning</li></ul>                               |
| <b>Phase Modulator<br/>(designing)</b>      | <ul style="list-style-type: none"><li>➤ Broadband characteristic for all ports</li><li>➤ Phase calibration capability</li></ul>                                      |
| <b>Synchronization Block<br/>(unsolved)</b> | <ul style="list-style-type: none"><li>➤ Compensation for the delay difference between AM and PM signals</li></ul>  |

# Phase Shifter S11 and S22

