# An Analysis of Cascode Structure for 60GHz Amplifier Design in 65nm CMOS

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# Motivation



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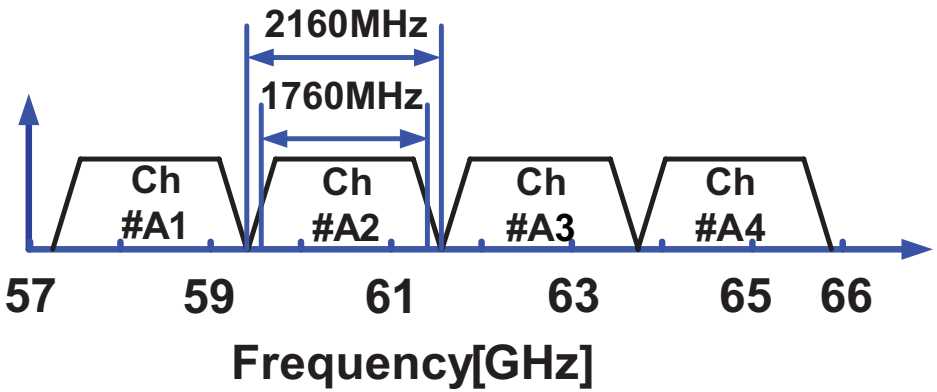
- IEEE 802.15.3c specification
  - 9 GHz unlicensed bandwidth
  - 2.16GHz/ch
  - Several Gbps data transfer
    - QPSK ⇒ 3.5Gbps
    - 16QAM ⇒ 7Gbps
- Amplifier in 60GHz transceiver
  - LNA
  - PA
  - IF buffer amplifier
  - Variable amplifier



# mmW CMOS amplifiers



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- **Gain**
  - The basic characteristic of an amplifier.
  - MAG is inversely proportional to the logarithm of the operating frequency.
- **Stability**
  - Always important for amplifiers
  - Large parasitic components
- **Power consumption**
  - Low power consumption is critical considering the battery life

# Cascode structure at mmW frequency



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- At lower frequencies, get a high gain.
- At mmW frequencies, a reduction of the reverse isolation $S_{12}$.
  - ✓Increase MSG
  - ✓Large K
  - ×Larger parasitic capacitance in the inter-stage node

# Cascode structure with inductance (1)



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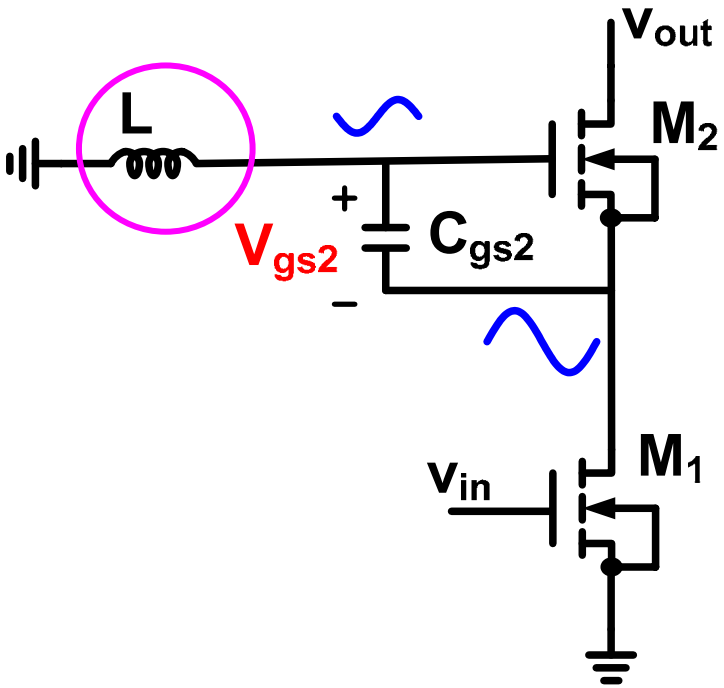
- **Large parasitic capacitance decreases the gain**
  - **Gain robust technique is utilized to increase gain**

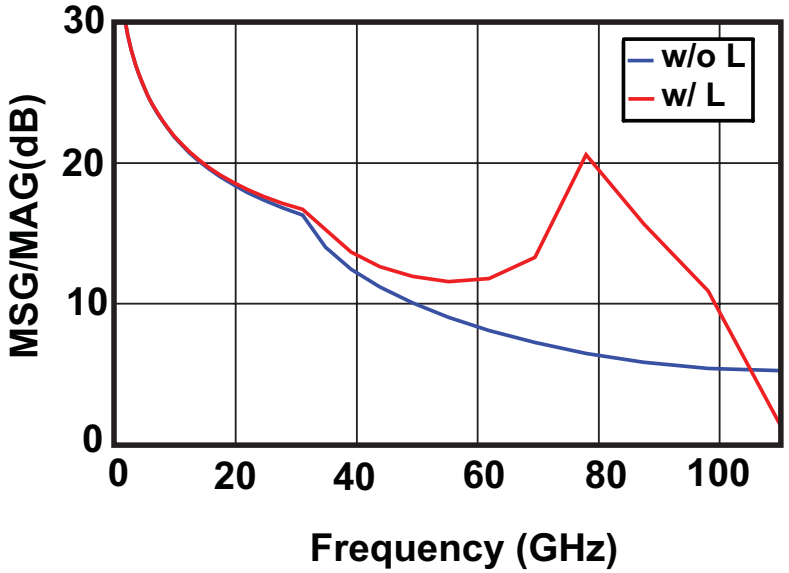


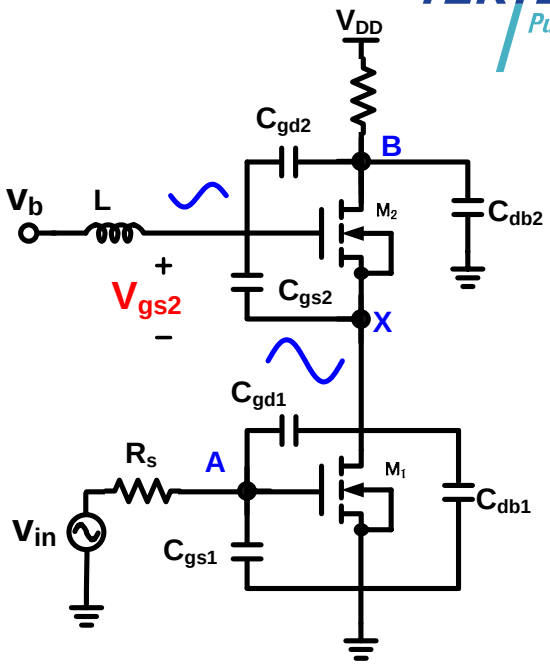

**Cascode structure with inductance**

*H. Hsieh, et al, *IEEE RFIC*, Jun. 2011

# Cascode structure with inductance (2)






- **A double zero and a double pole are added when using L**
  - **The pole frequency is much lower than the zero frequency.**
  - **At 60GHz, only the poles have a**

# Cascode structure with inductance (2) 

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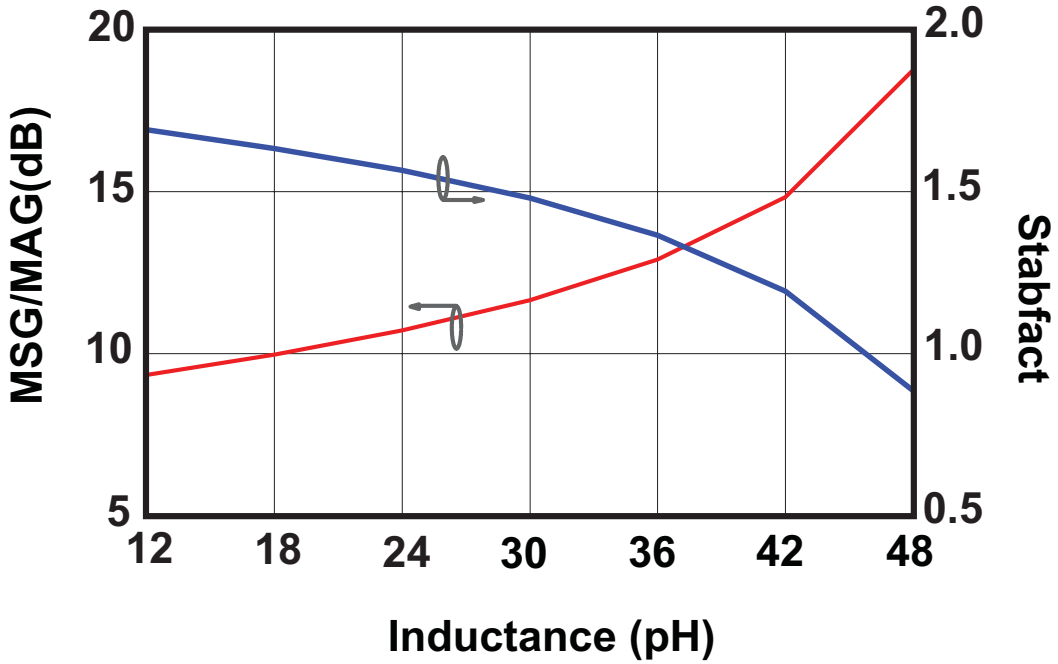
◆The trade-off between $G_{max}$ and stability factor




**Inductance has to be optimized reasonably**

# Measurement results



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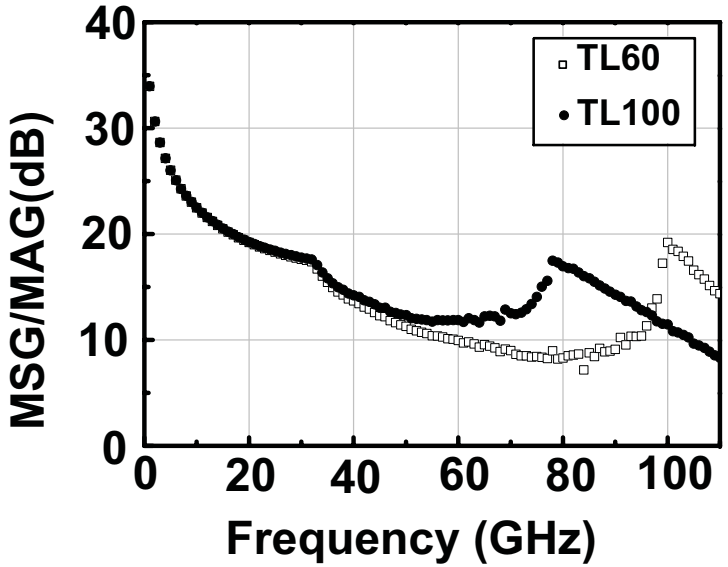
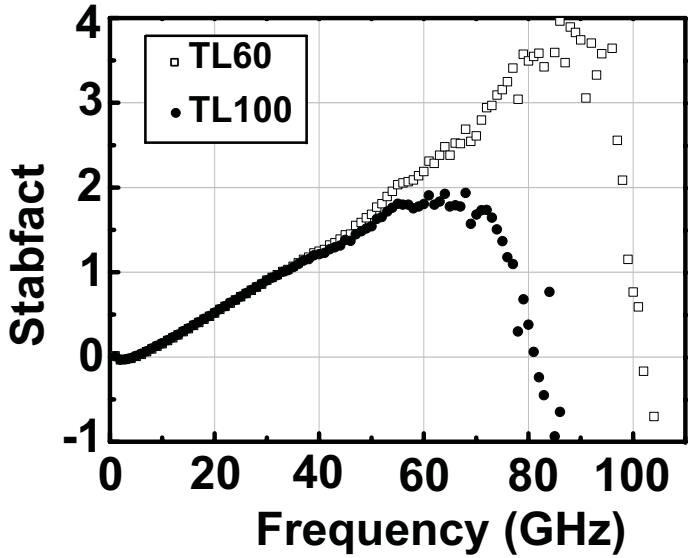
- The cascode structure with 60μm and 100 μm TLs in 65nm CMOS (about 0.3pH per μm).
  - CS $W_f$=20×2 μm ( $N_f$=20)
  - CG $W_f$=20×2 μm ( $N_f$=20)




MaxGain

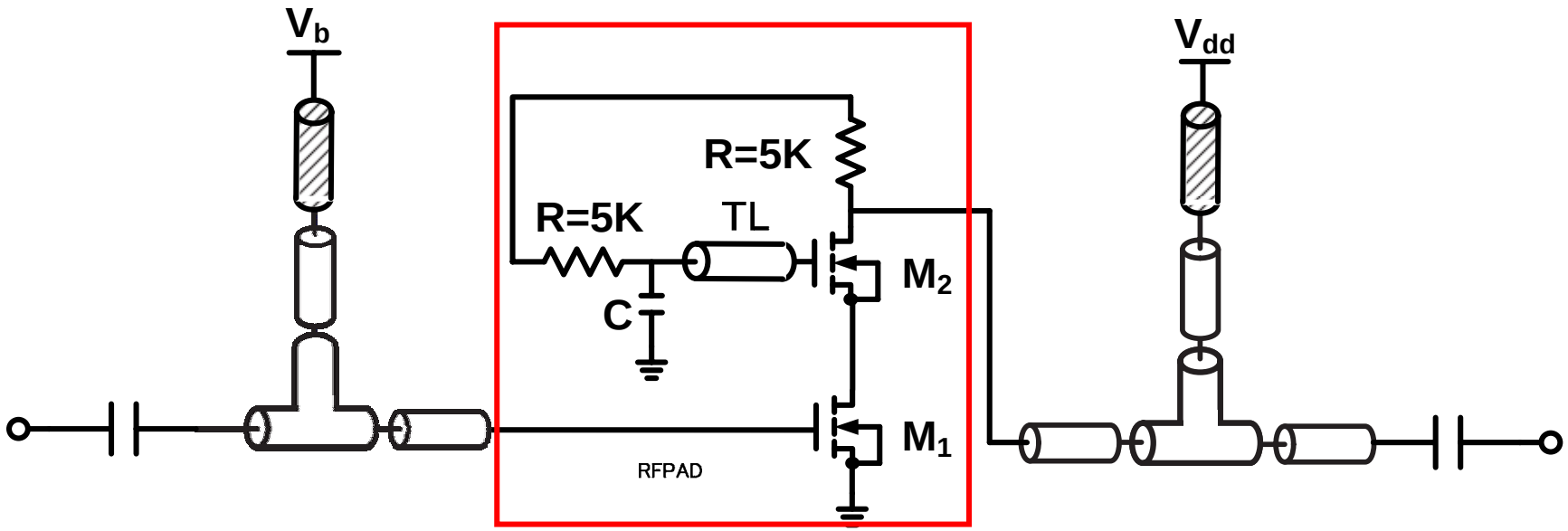



Stability factor

# 1-stage amplifier using cascode structure

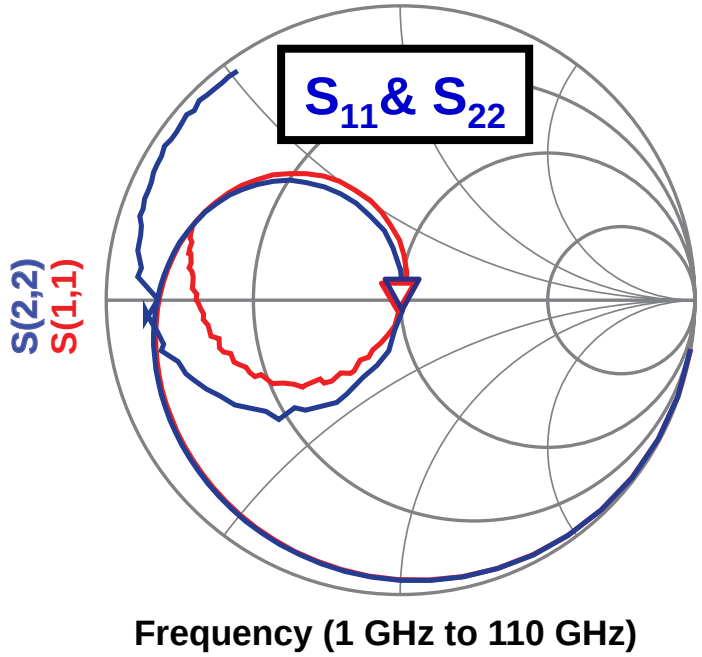


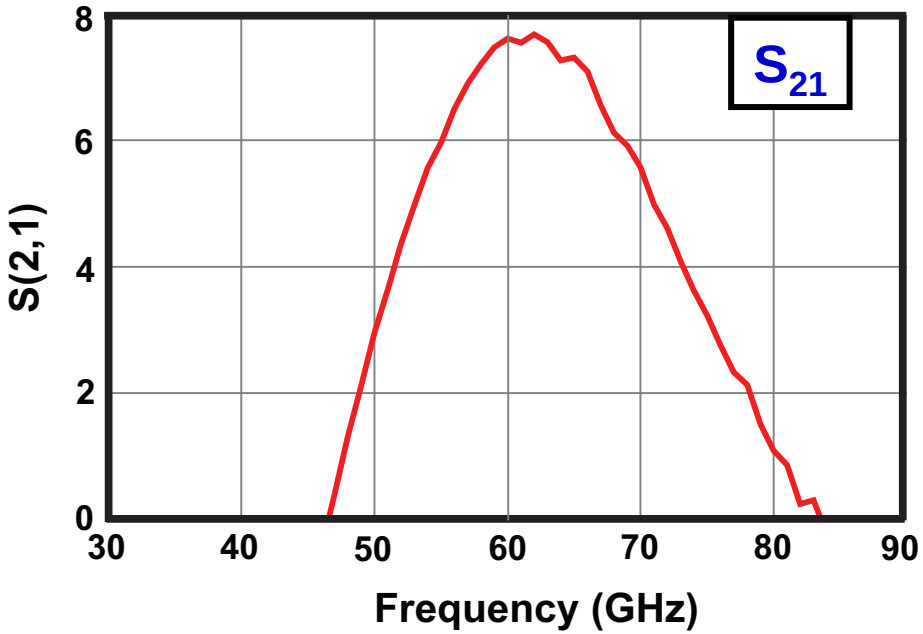
- The measurement S-parameter is used
- TL are utilized for impedance matching
- Decoupling MIM transmission line is used for AC ground



# Simulation results of the 1-stage amplifier






## Cascode structure size:

- CS Wf=20×2 μm ( Nf=20)
- CG Wf=20×2 μm ( Nf=20)
- TL 100 μm

## Power Consumption:

## 7.2 mW

# Conclusion



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- Cascode structure is attractive for the good reverse isolation $S_{12}$ at 60GHz amplifiers
- Gain robust technique is utilized to increase gain, while decreases the stability. Inductance has to be optimized reasonably.
- A 20-finger CS and 20-finger CG transistors with 100 μm TL cascode structure achieves 12 dB MSG and unconditional stability.
- 1-stage amplifier is simulated utilizing the cascode TEG measurement results, 7.6 dB gain and 7.2 mW power consumption are obtained.

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# Thank you

# Q&A



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