A 0.5-V CMOS Power Amplifier with Adaptive Bias for Short-Rang Low-Power Applications

呉 鋭 岡田 健一 松澤 昭
Rui Wu Kenichi Okada Akira Matsuzawa

東京工業大学 大学院理工学研究科 電子物理工学専攻
Department of Physical Electronics,Tokyo Institute of Technology

1 Introduction

CMOS power amplifiers (PAs) are dominant in modern short-rang wireless applications, such as wireless sensor networks and biomedical implantable electronic systems, owing to their low cost and the capability of high-level system integration [1]. As the scaling of the device size in CMOS technologies continues, the nominal supply voltage of the ICs has to be reduced accordingly due to reliability issues leading to significant degradations in the RFIC performances. Especially, the linearity deterioration of the CMOS PAs under the ultra-low supply voltage conditions can not be tolerated by non-constant envelop modulation schemes commonly adopted by the short-range applications [2]. Therefore, it is necessary to investigate a high-linearity CMOS PAs operating under the ultra-low supply voltage.

2 Circuit Design

A 0.5-V parallel class-AB and -C power amplifier with the adaptive bias is proposed to cope with the low supply voltage issues, as shown in Fig. 1. The parallel combination of a class-AB and a class-C amplifier, which is actually a variation of the derivative superposition approach [3], can improve both the linear operation range and the power efficiency. The folded cascode topology is utilized for maintaining the proper operation of the transistors at the 0.5-V supply voltage. Adaptive bias circuits are designed to offer large gate bias voltages for high input power situation compensating for the gain depression.

The PA is implemented in a commercial 0.18-μm CMOS process. Simulation results show 9.4-dB power gain, 7.5-dBm output power, 5.3-dBm P_{1dB}, and 27.9% maximum power-added efficiency (PAE) at 2.45 GHz, as illustrated in Fig. 2. The P_{1dB} of the proposed PA is 3.6 dB larger than that of a conventional class-AB PA while having the same small-signal gain. At the output power range of interest (-3dBm∼5dBm), the maximum difference of the third-order intermodulation distortion (IM3) between the linearized PA and the conventional class-AB PA is 11dB, as depicted in Fig. 3. It also can be observed from Fig. 2, the PAE of the proposed PA is improved by 8.1% at the P_{1dB} point.

3 Conclusions

In this paper, a linearized CMOS PA with improved efficiency suitable for 0.5-V supply voltage operation is implemented. This work demonstrates the feasibility of the ultra-low supply voltage CMOS PA for short-rang, low-power applications using non-constant envelop modulation.

Acknowledgment

This work was partially supported by MIC, MEXT, STARC, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

References

[1] T.-K. Nguyen, *et al.*, "A low-power RF direct-conversion receiver/transmitter for 2.4-GHz-band IEEE 802.15.4 standard in 0.18-μm CMOS technology," IEEE Trans. Microwave Theory and Techniques, vol. 54, pp. 4062-4071, Dec. 2006.

[2] M. J. Deen, *et al.*, "Low-power integrated CMOS RF transceiver circuits for short-range applications," IEEE Midwest Symposium on Circuits and Systems, pp. 1544-1549, Aug. 2007.

[3] Y. Ding, *et al.*, "A high-efficiency CMOS +22-dBm linear power amplifier," IEEE J. Solid-State Circuits, vol. 40, pp. 1895-1900, Sep. 2005.

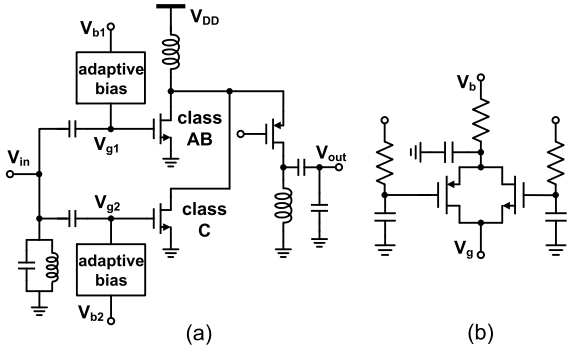

Fig. 1 (a) The proposed PA and (b) the adaptive bias circuit

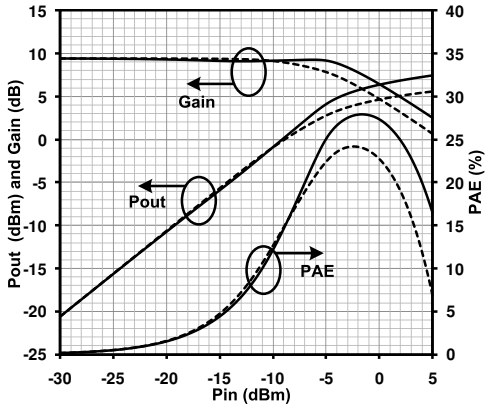

Fig. 2 The output power (Pout), gain and PAE of the proposed PA (solid lines) and the conventional class-AB PA (dash lines)

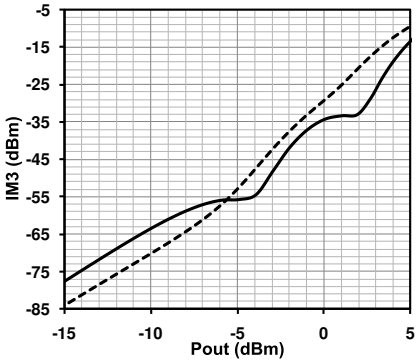

Fig. 3 The IM3 of the linearized PA (solid line) and the conventional class-AB PA (dash line)