Class-A および Class-AB によるミリ波帯高効率電力増幅器
A 14.3% PAE, 9.4- dBm P_{1dB} parallel Class A and AB 60 GHz CMOS PA

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1 Introduction

Accompanying with the scaling down of the CMOS technology, f_T and f_{max} of transistors are achieved above 100 GHz, making an all-CMOS solution at 60 GHz feasible. The merits of low cost compared with other technology such as GaAs and SiGe, and high integration of CMOS process make it a good candidate for the 60 GHz applications [1]. As the most difficult part, design of high linearity and high efficiency power amplifier (PA) is a real challenge, especially at mm-wave frequency. For 64 QAM and OFDM systems, the power amplifier needs a large back-off. Therefore, high efficiency at low input power is very important. This paper describes a 60 GHz PA with high output power and efficiency.

2 Power Amplifier Design

Doherty PA is famous for its high efficiency and linearity [2]. However, $\lambda/4$ transmission lines are needed for power splitting and combining, which occupy a large chip area and cost notable loss at 60 GHz. A two-stage PA is designed as shown in Fig. 1 by avoiding using the $\lambda/4$ transmission lines. The first stage is a normal common source (CS) stage, while the second stage consists two CS in parallel. One is biased as Class A while the other as deep Class AB. As we all know, Class A has good linerity, however, the power added efficiency (PAE) is poor. Compared to Class A, deep Class AB has good linearity and high PAE, but the output power is small. By combining Class A/AB, a high PAE at low input power and good output power can be realized.

3 Experimental Results

The PA is implemented in CMOS 65 nm process. The chip photo is shown in Fig. 2 and the chip area is 0.6 mm². The chip is measured on wafer by using a probe station. Small signal gain is shown in Fig. 3(a). A peak gain of 14.64 dB at 49 GHz and a 9.84-dB gain at 60 GHz are achieved. Fig. 3(b) gives the large signal measurement results at 60 GHz. The measured saturation output power is 11.7 dBm and the power at 1 dB compression point is 9.4 dBm. A maximum power added efficiency (PAE) of 14.3% and 12% at 1 dB compression point are realized. The chip consumes 45~58 mW power at a 1.2-V supply voltage. The performance is summarized in Table 1 and compared to [3].

4 Conclusion

A pseudo Doherty PA is designed in CMOS 65 nm process. The PA achieves a peak small signal gain of 14.64 dB at 49 GHz and a 9.84-dB gain at 60 GHz. The measured large signal results shows that a maximum power added efficiency (PAE) of 14.3% and 12% at 1 dB compression point

are realized.

References

[1] C. H. Doan, *et al. Radio Frequency Integrated Circuits Symposium*, June 2004, pp. 225–228.

[2] W. H. Doherty, Proceeding of the Institute of Radio Engineers, Vol. 24, No. 9, pp. 1163–1182, 1936.

[3] B. Wicks, *et al.*, *Radio Frequency Integrated Circuits Symposium*, May 2008, pp. 69–72.

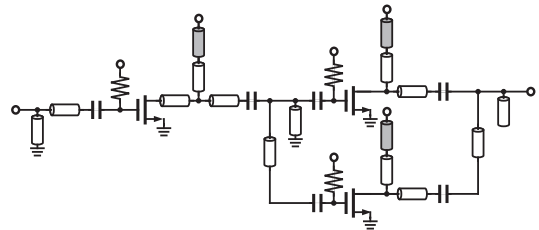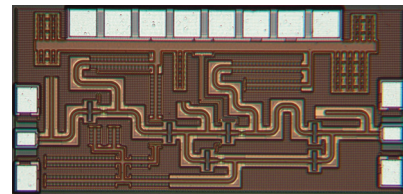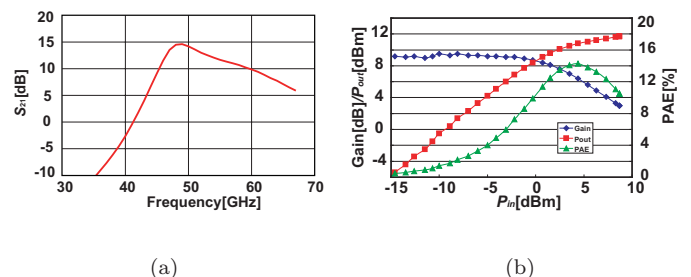Fig. 1　Schematic of PA.

Fig. 2　Chip photo.

(a)　　　　　　　　　　　(b)

Fig. 3　Measurement results. (a) S_{21}. (b) Large signal power gain, P_{out} and PAE.

Table 1　Performance summary.

Ref.	Topo.	Gain [dB]	P_{1dB} [dBm]	P_{sat} [dBm]	PAE@1dB [%]	PAE_{sat} [%]	Area [mm²]
[3]	Doherty	13.5	7.0	9.3	3	3	1.8
This work	Parallel ClassA/AB	9.84	9.4	11.7	12	14.3	0.6