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An ultra-compact LC-VCO using a stacked-spiral inductor

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Abstract: This paper proposes an ultra compact LC-VCO. Due to the speed-up of CMOS digital circuits, jitter of ring oscillators is becoming a critical problem. Even though an LC-VCO has a better phase noise, a layout size of on-chip inductor is a problem as a clock generator. Thus, the proposed LC-VCO consists of a very compact stacked-spiral inductor and active components placed are beneath the inductor. The VCO is implemented by a 65-nm CMOS process, and the chip area is only 594 μm^2. This VCO achieves a phase noise of −93 dBc/Hz@1 MHz, power consumption of 0.36 mW, and FOMA of 210 dBc/Hz.

Keywords: LC-VCO, stacked-spiral inductor, small area, FoMA

Classification: Integrated circuits

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1 Introduction

Clock generators have usually been implemented by ring oscillators, especially at lower frequencies. Due to the miniaturization of CMOS process technology, a low supply voltage, V_{DD}, is required for scaled CMOS transistors. The jitter characteristic of ring oscillators is seriously degraded by the low supply voltage [1], and it also causes the performance degradation in data converters and high-performance digital circuits. To avoid the degradation, a low jitter performance is required for clock generators. LC oscillators are less sensitive to the supply voltage while ring oscillators are much degraded [2]. In addition, the phase noise of LC oscillators is theoretically about 30 dB better than that of ring oscillators with the same power consumption [2]. Thus, LC oscillators are expected to replace ring oscillators. However, one of the weaknesses in LC oscillators is large layout area caused by an on-chip inductor. A compact LC oscillator has been expected.

In this paper, an ultra compact LC-VCO, as small as ring oscillators, is presented, which consists of a very compact stacked-spiral inductor [3] and active components are placed beneath the inductor [4, 5]. This paper explains design consideration to minimize layout area and reduce the influence of circuit stacking.

2 Stacked-spiral inductor

In this section, downscaling of on-chip inductors is discussed, especially for a stacked-spiral inductor. Then, the influence of downscaling of VCO is analyzed.

The phase noise can be derived from the following equation [6]:

$$\mathcal{L}(f_{\mathrm{offset}}) = 10\log\left[\frac{2\mathrm{k}T}{P_{\mathrm{sig}}}\left(\frac{f_0}{2Q_{\mathrm{tank}}f_{\mathrm{offset}}}\right)^2\right] \quad (1)$$

where k is Boltzmann's constant, T the absolute temperature, P_{sig} the output power, f_0 the oscillation frequency and f_{offset} the offset frequency, Q_{tank} the quality factor of the resonator. According to Eq. (1), Q_{tank} is very important for the performance of VCOs.

Fig. 1 shows structures of on-chip inductors for a 10 GHz LC resonator. Fig. 1 (a) is a proposed differential stacked-spiral inductor using 6 metal layers, and Fig. 1 (b) shows a mono-layer inductor. The stacked-spiral inductor

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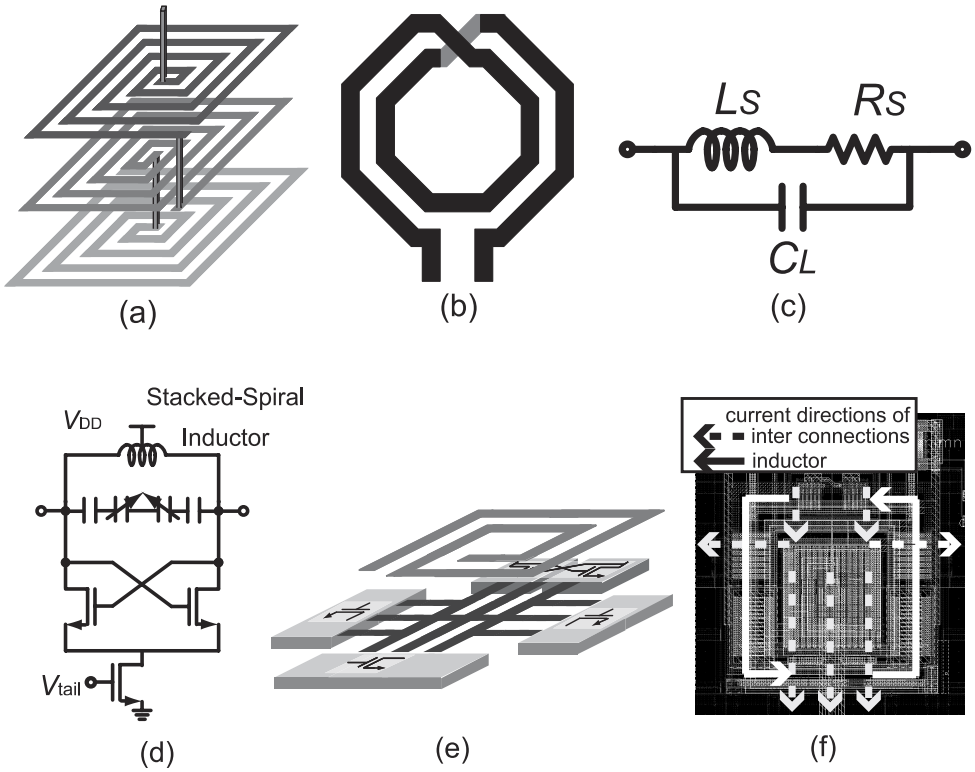

Fig. 1. (a) Stacked-spiral inductor (b) Mono-layer inducor (c) An equivalent circuit of inductor (d) Circuit schematic of LC-VCO (e) Circuit stacking beneath the inductor (f) Current directions of circuit and inductor

has 20-μm outer diameter and 1.2-μm line width, and the mono-layer one has 126-μm outer diameter and 5-μm line width.

On-chip inductor models can be simplified as shown in Fig. 1 (c). The characteristics of the inductors are estimated by the 3D electromagnetic simulator HFSS. The mono-layer inductor has a 7.9 Ω series resistance R_s and a 14.4 of quality factor Q due to the wide line width. On the other hand, the stacked-spiral inductor also has an inductance L_s of 3.44 nH. However, the quality factor is only 4.35, because the resistance R_s has a high value as 53.6 Ω due to a long narrow spiral line. If an LC-VCO uses the staked-spiral inductor, the VCO consumes more power or has worse phase noise because of the degraded quality factor. On the other hand, the layout area can be dramatically shrank. The stacked-spiral inductor has 40 times smaller area than the mono-layer inductor.

3 Rest part placement beneath the spiral inductor

Fig. 1 (d) shows a circuit schematic of the proposed LC-VCO, which is a simple NMOS-topology LC-VCO. The NMOS topology can reduce the layout area while PMOS and CMOS topologies require larger cross-coupled transistors. Even if the layout area of on-chip inductors can be shrank, rest parts like transistors and capacitors remain large. A further minimization requires

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an area reduction of the rest parts. One of the ways is to place the rest parts beneath the inductor as shown in Fig. 1 (e). While this contributes to reduce the total layout area dramatically, it becomes an issue to consider the interaction between the inductor and the rest parts. The rest parts do not only consist of transistors and capacitors but also metal wires. The metal wires might build a loop with transistors and capacitors, so a carefull design is required. The loop causes degradation of inductors in terms of inductance and quality factor, which also causes degradation in VCO performances, *e.g.*, phase noise, output power, and power consumption.

Due to the stacked placement, inductive coupling becomes larger because the coil trace also becomes closer to metal wires in rest circuit parts. The coupling might cause degradation of inductance and quality factor. To understand the influence, mutual inductance M can be estimated by the following equation [7].

$$M = 2m\left\{\ln\left(\frac{m}{d}+\sqrt{1+\frac{m^2}{d^2}}\right)+\frac{d}{m}-\sqrt{1+\frac{m^2}{d^2}}\right\} \tag{2}$$

where m is the length and d the distance between parallel lines. To reduce inductive coupling, the parallel length should be shorter or distance should be farther.

The mutual inductance also affects as a eddy current, which is generated by a current loop in metal lines and plates. The effect of eddy current can be estimated by the following equation.

$$\begin{aligned} L_{\text{total}} &= L_{\text{ind}}\left(1-\frac{k^2\omega^2 L_{\text{eddy}}^2}{R_{\text{eddy}}^2+\omega^2 L_{\text{eddy}}^2}\right) \\ &= L_{\text{ind}}\left(1-\frac{k^2 Q_{\text{eddy}}^2}{1+Q_{\text{eddy}}^2}\right) \end{aligned} \tag{3}$$

where L_{total} is the total inductance, L_{ind} the original inductance of the inductor, k coupling factor, L_{eddy} the indcutance, R_{eddy} the resistance and Q_{eddy} the quality factor of eddy current. To reduce the effect of eddy current, the value of eddy current and the diameter of eddy current loop should be small.

Therefore, to prevent inductive coupling, two layout techniques were used. To reduce eddy current, interconnections have slits as shown in Fig. 1 (e). In addition, to reduce parallel metal lines, transistors and interconnections should be placed orthogonally to the inductor trace such as shown in Fig. 1 (f). The influence of the inductive coupling is simulated by HFSS with a metal-line model. The results show that the inductance is barely reduced and the quality factor is degraded by 7-%, which is equal to a 0.6-dB degradation in phase noise.

The influence of the core circuit on phase noise is very little, while the benefits of area saving is much larger than the degradation of phase noise. Thus, the proposed technique utilizing both the stacked-spiral inductor and beneath-placed devices is practical.

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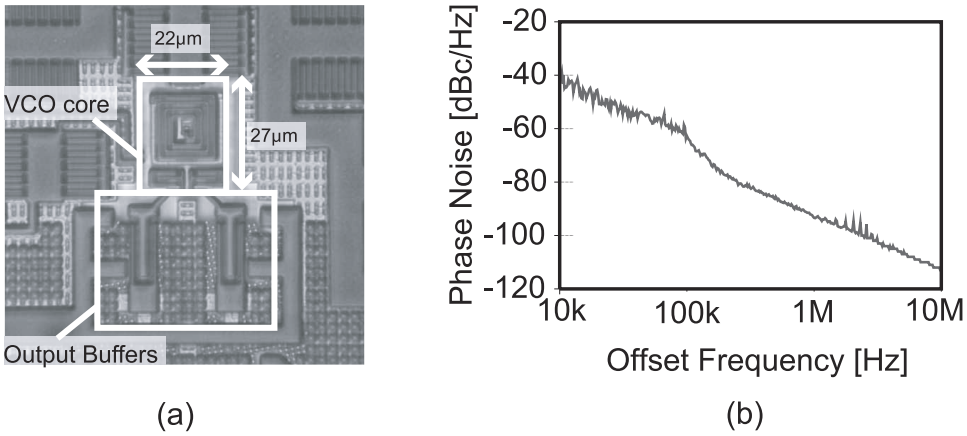

Fig. 2. (a) Chip micrograph (b) Measured phase noise

4 Measurement result

This proposed LC-VCO is implemented by using a 65-nm CMOS process. Fig. 2 (a) shows the chip micrograph, and the core area is 594 μm^2. It is measured by using a signal source analyzer (Agilent E5052B and E5053A) and an external buffer amplifier. The supply voltage is 0.5 V. The power consumption is 0.36 mW, and the oscillation frequency is 9.9 GHz with a 0.2-GHz tuning range. Fig. 2 (b) shows the measured phase noise, and it is -93 dBc/Hz at 1 MHz offset and -113 dBc/Hz at 10 MHz offset.

In general, the figure-of-merit (FoM) is used to evaluate the performance of VCOs. FoM is a normalized phase noise by oscillation frequency, offset frequency and power consumption, which can be defined by the following equation [8],

$$FoM = -\mathcal{L}(f_{\text{offset}}) + 20\log\left(\frac{f_0}{f_{\text{offset}}}\right) - 10\log\left(\frac{P_{\text{DC}}}{1\text{mW}}\right) \tag{4}$$

where P_{DC} is power consumption. The fabricated VCO achieves FoM of 177 dBc/Hz, and it is almost impossible for ring oscillators to achieve such high FoM.

There is a trade-off between the area and FoM, because a larger diameter is required to obtain a higher quality factor of inductors. LC-VCOs should also be evaluated with the figure-of-merit normalized by area (FoMA), which is expressed by the following equation [9].

$$FoMA = FoM - 10\log\left(\frac{\text{Area}}{1\text{mm}^2}\right) \tag{5}$$

The proposed LC-VCO achieves the best FoMA of 210 dBc/Hz. Table I summarizes the state-of-the-art results of clock generators using CMOS technology. The proposed LC-VCO demonstrates the best FoMA using a stacked-spiral inductor and beneath-placed devices.

5 Conclusion

This paper proposes an ultra compact LC-VCO using a stacked-spiral inductor with a beneath-placed core circuit. The oscillation frequency of the VCO

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Table I. Performance summary

	[3]	[4]	[10]	This Work
Area [μm^2]	2597	40000	2400	584
P_{DC} [mW]	2.8	5.8	9.8	0.36
PN [dBc/Hz]	-103@1 MHz	-125@3 MHz	-101@600 kHz	-113@10 MHz
Freq.	5 GHz	2 GHz	0.9 GHz	9.9 GHz
V_{DD} [V]	1	1.8	3.3	0.5
Tech.	90 nm CMOS	250 nm BiCMOS	350 nm CMOS	65 nm CMOS
FoMA [dBc/Hz]	199	197	182	210
Type	LC (3D-inductor) +Div.	LC	Ring	LC (3D-inductor)

PN:Phase noise

is 9.9 GHz and it consumes 0.36 mW. The VCO has only 584-μm^2 chip area. The performance is better than convensional ring oscillators. The proposed LC-VCO achieves FoMA of 210 dBc/Hz.

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