Design of 0.5-V LC-VCO for Low-voltage and Low-jitter Clock Generator

ウェイ デン 岡田 健一 松澤 昭
Wei Deng Kenichi Okada Akira Matsuzawa

東京工業大学 大学院理工学研究科 電子物理工学専攻
Department of Physical Electronics,Tokyo Institute of Technology

1 Introduction

Conventionally, ring oscillators are widely adopted in clock generation. Along with the scaling of the supply voltage, ring oscillators become infeasible due to too large jitter and power consumption[1], which highlight the necessity of adopting LC-VCOs as clock generators in future 0.5-V LSI. However, LC-VCOs suffer from narrow tuning range which is a key issue for clock generator to deal with different applications and compensate the variations in PVT. In this paper, a 0.5-V LC-VCO with frequency-extension circuit is proposed for low-voltage and low-jitter clock generation.

2 Proposed Architecture

As shown in Fig. 1 the proposed circuit is composed of a core VCO, the first divider and the second stage chain[2]. The first divider is a switchable divider whose divide ratio can be controlled from 2 to 3. The second divider chain consists of 6 successive dividers whose divide ratio is 2. Frequency planning of the proposed architecture is also illustrated in Fig.1. The fundamental frequency f_0 is output of core VCO, which can be tuned from 4.1-to-6.4GHz. $1/2f_0$ and $1/3f_0$ are generated by the first divider with switchable divide ratio, which means that the continuous tuning range of 2.05-to-3.2GHz and 1.37-to-2.13GHz can be obtained with the divide-by-2 and divide-by-3 operation, respectively. Lower frequency range from 0.05-to-1.37GHz can be generated by the second divider chain. As a result, the architecture provides two bands distributed from 0.05-to-3.2GHz (band I) and 4.1-to-6.4GHz (band II), minimizing power consumption.

3 Measure Results

For silicon verification, the proposed circuit is fabricated in a standard 9-metal-layer 90nm CMOS process. Phase-noise characteristics for each divide ratio (divide-by-2 and divide-by-3) of the first divider stage are illustrated in Fig. 2. A die photo is shown in Fig. 3. The core chip area is only 0.15mm^2.

4 Conclusion

As addressed in this paper, the investigation of adopting LC-VCOs to replace ring oscillators will become essential during the design of future low-voltage and low-jitter clock generators.

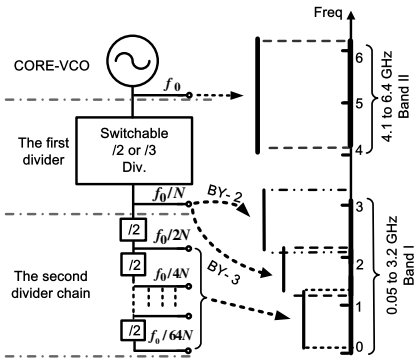

Fig. 1 Proposed architecture.

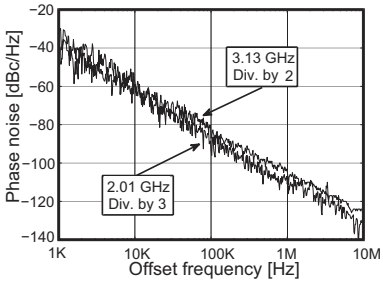

Fig. 2 Phase noise characteristic

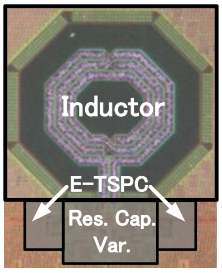

Fig. 3 Chip micrograph

Acknowledgment

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Reference

[1] K. Okada, *et al.*, "A 0.114mW dual-coduction class-C CMOS VCO with 0.2-V power supply, " *IEEE symp. VLSI Circuits,* pp.228-229, Jun. 2009.

[2] W. Deng, *et al.*, "A 0.5-V, 0.05-to-3.2 GHz, 4.1-to-6.4 GHz LC-VCO using E-TSPC frequency divider with forward body bias for sub-picosecond-jitter clock generation," *IEEE A-SSCC Dig. Tech. Papers,* pp.93-96, Nov. 2010.