IEICE Electronics Express, Vol.8, No.13, 1071–1074

A 14.3% PAE parallel class-A and AB 60 GHz CMOS PA

Ning Li[a)], **Kota Matsushita, Kenichi Okada, and Akira Matsuzawa**

Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27 Ookayama, Meguro-ku, Tokyo, 152–8552, Japan
a) *lining@ssc.pe.titech.ac.jp*

Abstract: At 60 GHz, it becomes difficult to achieve a high power added efficiency (PAE) and large output power for CMOS power amplifier (PA). A parallel class-A and AB pseudo Doherty PA is designed in CMOS 65 nm process to obtain a high PAE and large output power. The PA achieves a 9.8-dB gain at 60 GHz. The measured large signal results show that a maximum power added efficiency (PAE) of 14.3% and 12.0% at 1 dB compression point are realized. The chip consumes 45∼58 mW power from a 1.2-V supply voltage. The chip area is 0.6 mm^2 including pads.

Keywords: millimeter wave, power amplifier, CMOS
Classification: Microwave and millimeter wave devices, circuits, and systems

References

[1] C. H. Doan, et al., *Radio Frequency Integrated Circuits Symp.*, pp. 225–228, June 2004.
[2] W. H. Doherty, *Proc. Institute Radio Engineers*, vol. 24, no. 9, pp. 1163–1182, 1936.
[3] N. Li, K. Matsushita, N. Takayama, S. Ito, K. Okada, and A. Matsuzawa, "Millimeter-wave amplifiers design by employing multi-line de-embedding technique," *IEICE Trans. Electron*, vol. E93-A, no. 2, pp. 2733–2744, Feb. 2010.
[4] B. Wicks, et al., *Radio Frequency Integrated Circuits Symp.*, pp. 69–72, May 2008.

1 Introduction

Accompanying with the scaling down of the CMOS technology, f_T and f_{max} of transistors are achieved above 100 GHz, making an all-CMOS solution at 60 GHz feasible. The merits of low cost compared to other technology such as GaAs and SiGe, and high integration of CMOS process make it a good candidate for the 60 GHz applications [1]. As the most difficult part, design of high linearity and high efficiency power amplifier (PA) is a real challenge,

DOI: 10.1587/elex.8.1071
Received May 27, 2011
Accepted June 13, 2011
Published July 10, 2011

especially at mm-wave frequency. For 64 QAM and OFDM systems, the power amplifier needs a large back-off. Therefore, high efficiency at low input power is very important. This paper describes a 60 GHz PA with high output power and efficiency.

2 Power amplifier design

Doherty PA is famous for its high efficiency and linearity [2]. Fig. 1 (a) shows the diagram of a typical Doherty power amplifier. A $\lambda/4$ transmission lines is needed to realize the impedance conversion at the output node as shown in the figure. Another $\lambda/4$ transmission lines is also needed at the input node for power splitting and combining, and phase matching. These transmission lines occupy a large chip area and cost notable loss at 60 GHz. Moreover, at 60 GHz, impedance matching block is needed at high frequency to reduce power reflecting. However, in Fig. 1 (a), there is no impedance matching block.

A pseudo Doherty PA is proposed as shown in Fig. 1 (b). Matching block is considered and it also designed with the function of a power splitter and combiner. One of the two parallel transistors is working in Class-A while the other one working in Class-AB. Thus, the output $\lambda/4$ transmission line is not needed for impedance conversion.

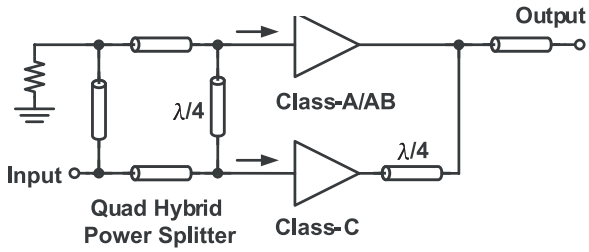
A two-stage PA is designed by using the proposed method. The schematic is shown in Fig. 1 (c). The first stage is a general common source (CS) stage, while the second stage consists of two CS in parallel. As well known, Class-A has good linearity, however, the power added efficiency (PAE) is poor. Compared to Class-A, deep Class-AB has good linearity and high PAE, but the output power is small. By combining Class-A/AB, a high PAE at low input power and good output power can be realized. The building block in Fig. 1 (c) are all tested before the circuit design and accurate models are created to achieve good performance [3].

Phase matching is very important between the two parallel paths. Phase discrepancy will decrease the output power gain. In a Doherty PA, phase matching are achieved by the $\lambda/4$ transmission lines; while in the proposed circuit, phase matching is also realized by the matching blocks, which are carefully designed to reduce the phase discrepancy between the two paths. the simulation results of the currents are shown in Fig. 1 (d). Less than 3 degree is realized for phase discrepancy.

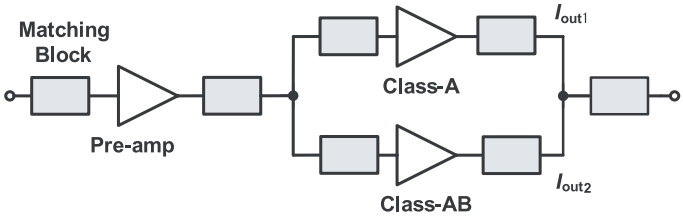
3 Experimental results

The proposed PA is fabricated in CMOS 65 nm process. The chip photo is shown in Fig. 2 (a) and the chip area is 0.6 mm^2 including pads. The chip is measured on wafer by using a probe station. Small signal gain is shown in Fig. 2 (b). A peak gain of 14.6 dB at 49 GHz and a 9.8-dB gain at 60 GHz are achieved. Fig. 2 (c) gives the large signal measurement results at 60 GHz. The measured saturation output power is 11.7 dBm and the power at 1 dB compression point is 9.4 dBm. A maximum power added efficiency (PAE) of

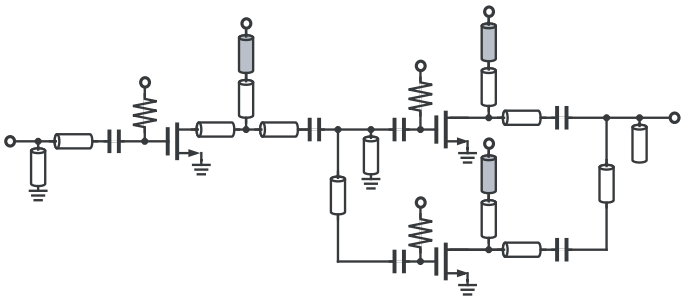
DOI: 10.1587/elex.8.1071
Received May 27, 2011
Accepted June 13, 2011
Published July 10, 2011



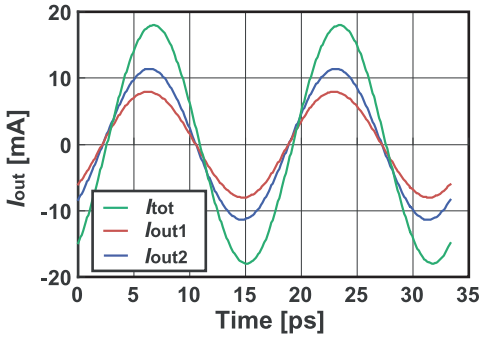
(a)



(b)



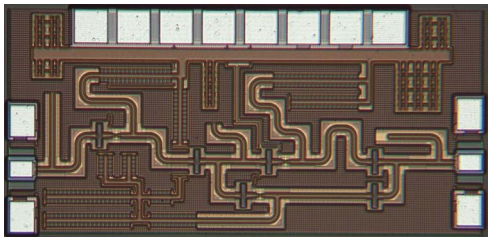
(c)



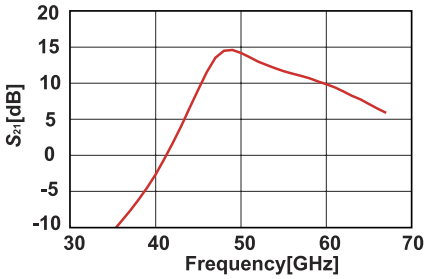
(d)

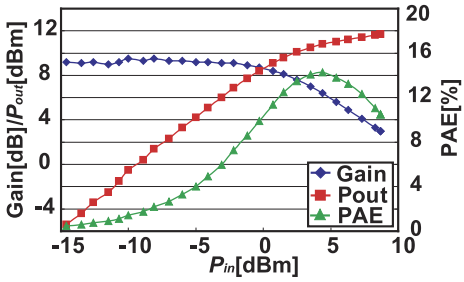
Fig. 1. (a) Diagram of a Doherty power amplifier. (b) Diagram of the proposed power amplifier. (c) Schematic of the proposed power amplifier. (d) Simulated output current of the two parallel power amplifiers.

DOI: 10.1587/elex.8.1071
Received May 27, 2011
Accepted June 13, 2011
Published July 10, 2011



(a)





(b) (c)

Fig. 2. (a) Micro chip photo. (b) Measured S_{21}. (c) Measured large signal power gain, P_{out} and PAE.

Table I. Performance summary.

Ref.	Topology	Gain [dB]	$P_{1\,\text{dB}}$ [dBm]	P_{sat} [dBm]	PAE@1 dB [%]	PAE_{sat} [%]	Area [mm^2]
[4]	Doherty	13.5	7.0	9.3	3	3	1.8
This work	Parallel ClassA/AB	9.8	9.4	11.7	12.0	14.3	0.6

14.3% and 12.0% at 1 dB compression point are realized at 60 GHz. The chip consumes 45∼58 mW power at a 1.2-V supply voltage. The performance is summarized in Table I and compared to the reference [4].

4 Conclusion

A parallel class-A and AB pseudo Doherty PA is designed in CMOS 65 nm process to obtain a high PAE and large output power. The PA achieves a 9.8-dB gain at 60 GHz. The measured large signal results demonstrate that a maximum power added efficiency (PAE) of 14.3% and 12.0% at 1 dB compression point are realized. The chip consumes 45∼58 mW power at a 1.2-V supply voltage.

Acknowledgments

This work was partially supported by MIC, SCOPE, MEXT, STARC, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

DOI: 10.1587/elex.8.1071
Received May 27, 2011
Accepted June 13, 2011
Published July 10, 2011