BRIEF PAPER *Special Section on Analog Circuits and Related SoC Integration Technologies*

Measurement of Integrated PA-to-LNA Isolation on Si CMOS Chip

Ryo MINAMI[†a)], **JeeYoung HONG**[†b)], ***Nonmembers***, **Kenichi OKADA**[†c)], ***Member***, ***and*** **Akira MATSUZAWA**[†d)], ***Fellow***

SUMMARY This paper presents measurement of on-chip coupling between PA and LNA integrated on Si CMOS substrate, which is caused by substrate coupling, magnetic coupling, power-line coupling, etc. These components are decomposed by measurements using diced chips. The result reveals that the substrate coupling is the most dominant in CMOS chips and the total isolation becomes less than −50 dB with more than 0.4 mm PA-to-LNA distance.

key words: *CMOS, power amplifier, substrate coupling, Tx leakage, mutual coupling*

1. Introduction

A low noise amplifier (LNA) is one of the key building blocks in RF transceivers, and it is required to amplify the weak signal even if strong interferes exist. A power amplifier (PA) is also the key building block in RF transceivers. The conventional power amplifier has been implemented by compound semiconductors such as GaAs, which has a superb high-frequency characteristic and high supply voltage. However, it causes the increase of die area and cost, because the power amplifier has to be designed as an external block. The PA is demanded to be integrated as a single-chip transceiver in the view of cost, die occupancy, and so on. Therefore, the PA is preferable to be implemented by CMOS process. Recently CMOS transistors can provide a sufficient ability for power amplifier and realize high frequency operation for RF circuits [1].

As compared with TDD systems, FDD systems have several design issues. One of the most critical issues for one-chip transceivers is Tx leakage. In the FDD systems, a transmitter and a receiver simultaneously work, and a duplexer is utilized to share a single antenna. However, duplexers have leakage between every ports. Tx output power is very large as compared with received signal, so it becomes considerably large interferer at Rx input even if the leakage is very small. This is called as Tx leakage [2]. Tx leakage causes inter-modulation and degrades demodulation quality of the Rx.

Moreover, the integration of the PA with other blocks increases many coupling paths such as substrate coupling, magnetic coupling of inductors, and wire coupling (V_{DD}, GND, etc.). As the result, the level of Tx leakage also increases [3].

To investigate the increased Tx leakage, a PA and some LNAs are placed on the same chip. Moreover, the chip is diced between PA and LNA for measuring an influence of each coupling. In this paper, the effect of substrate coupling and magnetic coupling are shown mainly.

Section 2 describes the coupling mechanisms. Section 3 discusses the simulation and measurement results. Section 4 reveals the conclusion about the dominant coupling mechanisms based on measurements.

2. Evaluation of Tx-Leakage

Integration of PA with other blocks on the same chip causes various coupling paths like Fig. 1. Thus, a PA and multiple LNAs are implemented on the same chip to investigate an influence of the couplings.

The wire couplings through V_{DD} and GND lines are considered as a negligible quantity. In the case of V_{DD} wire coupling, the each supply voltage is different. Moreover, GND wire is connected with a substrate, so that it is very difficult to distinguish the GND wire coupling from the substrate coupling in this case. Thus, the GND wire coupling is included into the substrate coupling in this paper.

Consequently, the substrate coupling and magnetic coupling by inductors are dominant in Tx leakage. Thus, a PA and multiple LNAs are placed on the same chip and measured and simulated.

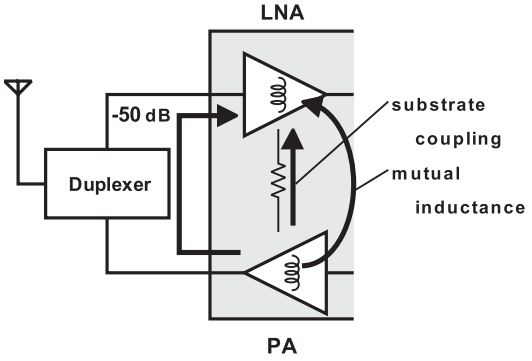
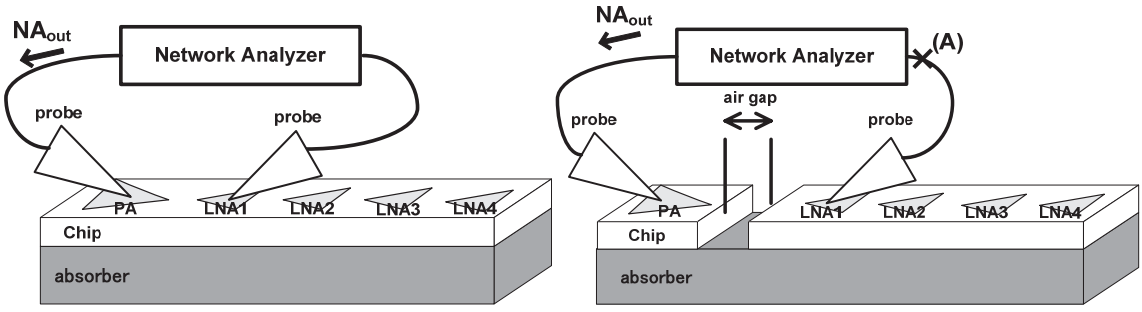


Fig. 1 Tx leakage path.

Manuscript received January 18, 2011.

[†]The authors are with the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, 152-8552 Japan.
a) E-mail: minami@ssc.pe.titech.ac.jp
b) E-mail: hong@ssc.pe.titech.ac.jp
c) E-mail: okada@ssc.pe.titech.ac.jp
d) E-mail: matsu@ssc.pe.titech.ac.jp

DOI: 10.1587/transele.E94.C.1057



(a) before dicing (b) after dicing

Fig. 2 Measurement setup.

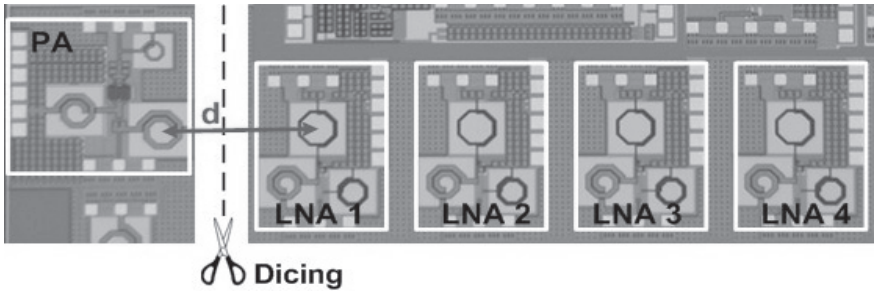


Fig. 3 Chip photograph.

2.1 Measurement Method

Figure 2 shows the measurement setup. To measure the influence of substrate couplings and magnetic coupling of inductors individually, the chip is diced [4]. Figure 3 shows the chip micrograph of the diced PA and LNAs. On this chip, there is a PA and four LNAs. After dicing, the distance between the PA and each LNA is 0.74 mm, 1.55 mm, 2.37 mm and 3.20 mm. As a result, the substrate couplings are blocked by physically separating the PA and LNA. Thus, only magnetic coupling of inductors can be measured by using a Network Analyzer. Concretely, the input is configured as the PA and the output as the LNA. The isolation is calculated by subtracting the sum of power gain (PA and LNA) from S_{21} as the following equation.

$$isolation\ [\mathrm{dB}] = S_{21} - (G_{PA} + G_{LNA}) \tag{1}$$

To separate the substrate coupling from the total coupling, the following equation is used with the measured isolations before and after dicing.

$$coupling_{substrate} = dicing_{before} - dicing_{after} \tag{2}$$

Furthermore, thermal noise which is generated by resistance of LNA's input side is calculated by Eq. (3) and compared with S_{21}. In Eq. (3), the bandwidth (B), temperature (T), and cable loss (LOSS) are assumed 10 Hz, 300 K, and 2 dB, respectively. Measured NF_{LNA} and G_{LNA} are used.

$$Noise_{thermal}\ [\mathrm{dBm}] = 10\log(kTB) + NF_{LNA} + G_{LNA} - Loss_{cable} \tag{3}$$

To compare with the isolation, the above thermal noise level is normalized by the output power of the network analyzer.

$$Noise_{thermal}\ [\mathrm{dB}] = Noise_{thermal}\ [\mathrm{dBm}] - (NA_{out})\ [\mathrm{dBm}] \tag{4}$$

In addition, the noise floor of the network analyzer and probe coupling should be considered, which influence on the coupling measurement. The probe coupling is assumed to be caused by the electromagnetic radiation between probes. These effects are evaluated by the open measurement without chips. The open measurement is done with 0.3 mm distance between probes and absorber, and distance between probes is varied from 0.74 mm to 3.20 mm. The noise floor is measured as S_{21} with 3 cm probe distance and 2 cm distance between probe and absorber. Moreover, the probe coupling is measured changing the probe distance. In this case, the measured probe coupling is considered as the worst case one, because probes behave as monopole antennas and have larger coupling. In case of actual measurement, the probe tip is terminated by DUT, so the coupling will become smaller practically. This thermal noise is the value measured at the point of (A) in Fig. 2(b).

2.2 Simulation Method

Figure 4 shows the schematic of the PA and LNA. The magnetic coupling between the inductor at PA output side and the inductor at LNA input side can be assumed to be the

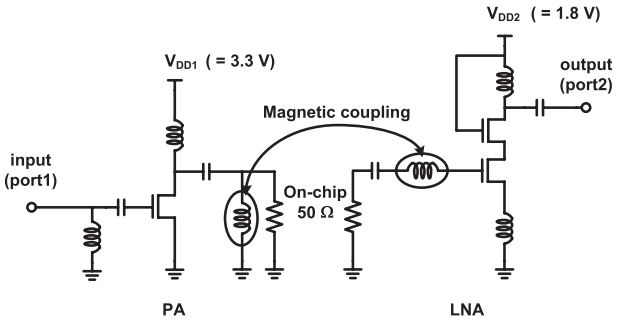


Fig. 4 Schematic of the PA and LNA.

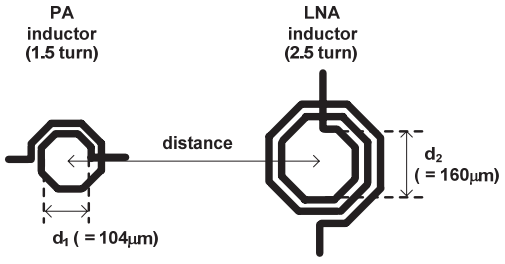


Fig. 5 The simulated inductor model.

most dominant. Thus, the inductors are simulated by an electromagnetic field simulator (Ansoft HFSS) to estimate magnetic coupling between PA and LNA. The distance between these inductors is set to the same distance as the chip measurement condition. Figure 5 shows the inductor model. To simulate S_{21} of the circuit shown in Fig. 4, the circuit simulator (Agilent ADS) is used, and the inductor model is derived by the electromagnetic simulator (HFSS).

3. Measurement Results

The PA and LNAs are implemented by 0.18 μm CMOS process and are designed for 5 GHz. The chip has 6 metal layers and the material of these layers is Aluminum. The thickness of Si substrate is 300 μm and the thickness of metal 1, 2, 3, 4 and 5 are 0.5 μm and that of top metal is 2 μm. The thickness of each inter-dielectric layer is 1.4 μm. The specification of the PA and LNA are summarized in Table 1.

The chip is measured by using RF probes with external DC blocks at input and output nodes. The S-parameters are measured using Agilent E8361A Network Analyzer. The output power of the network analyzer is −5 dBm.

Figure 6 shows the measured S_{21} for each distance with simulation results. The dotted lines are simulation results and the plotted markers are measurement results. The simulation and measurement results agree with each other except the case of 3.2 mm, and both results have the peak at 5 GHz, because the amplifiers have the peak gain at 5 GHz.

The simulated S_{21} is shifted to low value according to the distance. It means that the isolation between the PA and LNA depends on distance. The measured S_{21} is also

Table 1 Specification of the designed PA and LNA.

	PA	LNA
Technology	0.18 μm CMOS process	
Frequency	5 GHz	
V_{DD}	3.3 V	1.8 V
Gain at 5GHz	5.5 dB	15.1 dB
NF at 5GHz		2.7 dB

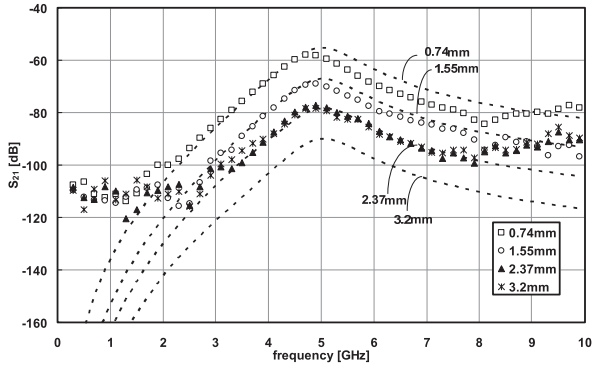


Fig. 6 Measured S_{21} versus frequency.

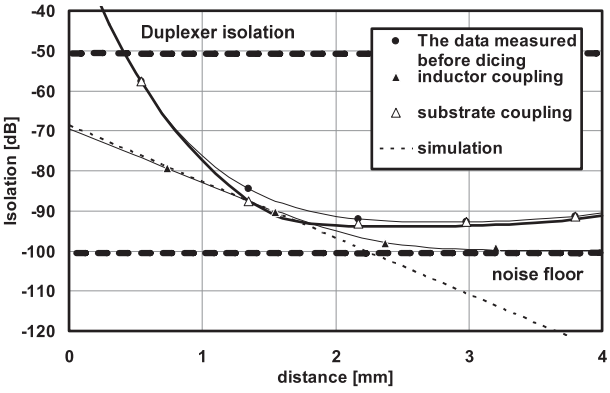


Fig. 7 Comparison of isolation at 5 GHz.

shifted lower up to around 2.37 mm because of the influence of noise. The detailed analysis of various noises is described at the end of Sect. 3. Figure 7 shows the comparison of the isolation value which is derived by Eq. (1) at 5 GHz. The data of inductor coupling is measured after dicing the chip. It has the same tendency with the simulation result up to around 1.8 mm, and some errors are shown in the distance over 1.8 mm. The source of the error is assumed the noise floor of the network analyzer. Moreover, the substrate coupling is also shown in this figure. The substrate coupling is calculated by Eq. (2) and others are the measurement data.

The data measured before dicing consists of substrate coupling, inductor coupling, wire coupling, etc. Compared with the duplexer isolation, it is lower than the duplexer isolation from near 0.4 mm. On the average, the distance be-

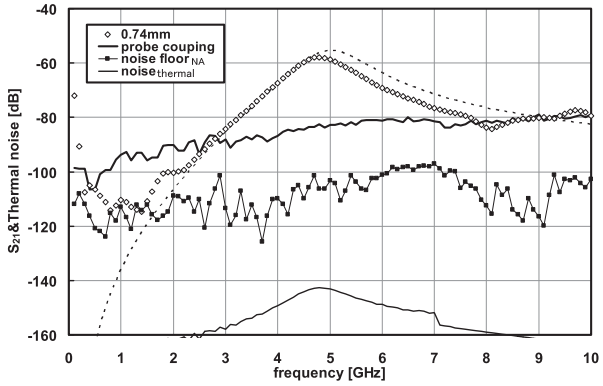


Fig. 8 Thermal noise, noise floor of network analyzer, and probe coupling versus frequency.

tween a PA and a LNA is more than 0.4 mm. Thus when the PA is integrated with other blocks, the increased Tx leakage is not a serious issue if it is placed with more than 0.4 mm distance and is carefully designed.

The data of substrate coupling is calculated by Eq. (2). Compared to the results of magnetic coupling, it is larger than the magnetic coupling all over the distance. Thus, substrate coupling is the most dominant factor.

Figure 8 shows the measured result in the case of 0.74 mm with several possible noise sources such as thermal noise, the noise floor of the network analyzer, the probe coupling. The dotted line is the simulation result. The thermal noise is calculated by Eqs. (3), (4) and the other noise sources are measured.

As shown in Fig. 6, there is some mismatch at the lower-side and higher-side frequency. At the lower frequency, the mismatch is caused by the noise floor of the network analyzer. Thus, S_{21} does not decrease under the -110 dB. The reason why the magnetic coupling does not decrease under the -100 dB in Fig. 7 is the same which is affected by the noise floor of the network analyzer. The probe coupling is larger than S_{21}. However, it has to be considered that the measured probe coupling is the worst case. The reason is that the coupling signal passes through the chip while there is no chip under the calibration. The probe coupling affects the measurement errors with the noise floor of the network analyzer.

At the higher frequency, the mismatch is caused by the probe coupling, because the electromagnetic coupling between probes becomes larger at the high frequency. Thus, the measured S_{21} gets closer to the largest result of the probe coupling.

The calculated thermal noise is very small. Thus, the thermal noise is not a major error source in this measurement.

4. Conclusion

On-chip Tx leakage is one of the most important issues for integrated power amplifiers, which is caused by substrate coupling, magnetic coupling, power-line coupling, etc. In this work, the isolation between PA and LNA is measured, and the result reveals that the substrate coupling is the most dominant in CMOS chips and the total isolation becomes smaller than duplexer isolation with more than 0.4 mm distance. Error in measurement is also analyzed, and the error of over 8 GHz, is caused by the probe coupling and the error of under 3 GHz under, is caused by the noise floor of the network analyzer.

Acknowledgements

This work was partially supported by STARC, MIC, SCOPE, MEXT, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

References

[1] I. Aoki, S. Kee, R. Magoon, R. Aparicio, F. Bohn, J. Zachan, G. Hatcher, D. McClymont, and A. Hajimiri, "A fully-integrated quad-band GSM/GPRS CMOS power amplifier," IEEE J. Solid-State Circuits, vol.43, no.12, pp.2747–2758, Dec. 2008.

[2] D. Imanishi, M. Kanemaru, K. Okada, and A. Matsuzawa, "An evaluation of isolation between on-chip PA and LNA," Proc. IEICE Gen. Conf., C-12-61, March 2009.

[3] J. Hong, D. Imanishi, K. Okada, and A. Matsuzawa, "Measurement of the Coupling Path between Integrated PA and LNA," Proc. Electron. Conf. IEICE, C-12-18, Sept. 2009.

[4] S. Bronkers, G. Vandersteen, L. De Locht, G. Van der Plas, and Y. Rolain, "Study of the different coupling mechanism between a 4 GHz PPA and a 5–7 GHz LC-VCO," IEEE RFIC Symp. Dig., pp.475–478, June 2008.