An Improved Dual-Conduction Class-C VCO Using a Tail Resistor

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***Abstract*—This paper proposes a method to improve the power consumption of dual-conduction class-C VCO. The dual-conduction class-C VCO has two pairs of cross-coupled transistors for low supply voltage operation. One is a main pair for the class-C operation, the other is an auxiliary pair for startup. The auxiliary pair continues to operate after the VCO starts class-C operation, which consumes additional power. Thus, we added a resistor to the source node of the auxiliary pair. Since the resistor reduces the current of the auxiliary pair, the power consumption can be improved. The proposed VCO is fabricated by using a 0.18 μm CMOS technology. It oscillates at 5.4 GHz with 0.20 V supply voltage, consumes 96 μW, and achieves a FoM of -187 dBc/Hz.**

I. Introduction

High-speed digital circuits require low power, low noise clock generation. The scaling of CMOS technology has decreased the supply voltage and the power consumption. However, at lower supply voltages, since the amplitude is small, the phase noise is degraded due to the small signal power. It is difficult to cope with both low power and low phase noise.

The class-C VCO has been proposed for low phase noise operation [1], [2]. It has an independent gate bias and a tail capacitor. The gate bias is set lower than the threshold voltage. Whereas, the tail capacitor makes the current waveform sharp. Due to the lower gate bias and the impulse-shape current waveform, the phase noise is low. However, because of the lower gate bias, it cannot oscillate at low supply voltages.

The dual-conduction class-C VCO has been proposed at ultra-low supply voltage [3]. It has two pairs of cross-coupled transistors. One is a main pair for class-C operation, the other is an auxiliary pair for the startup. The gate bias of the auxiliary pair is higher than that of the main pair. Due to the higher gate bias, it can oscillate at ultra-low supply voltages such as 0.20 V. However, the auxiliary pair degrades the FoM after the VCO starts class-C operation. It consumes additional power, and the higher gate bias degrades the phase noise.

In the proposed topology, a resistor is added to the source node of the auxiliary pair. This simple method does not require additional circuits and power dissipation. Since the resistor increases the source voltage, the transistors current is reduced at the stable state. Hence, the power consumption can be improved.

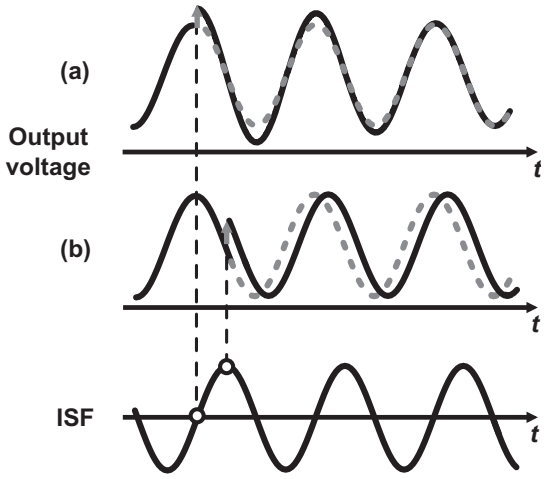

Fig. 1. Impulse Sensitivity Function (ISF).

II. Class-C VCO

This section describes the impulse sensitivity function (ISF) [4], [5] at first, and then describes the operation of class-C VCOs using the ISF.

A. Impulse Sensitivity Function (ISF)

The impulse sensitivity function (ISF) shows the sensitivity to the phase noise of oscillators. In case of Fig. 1(a), the noise is injected at the peak of the voltage waveform, and it increases the amplitude. However, the waveform will return to its original amplitude because of the stability of oscillation amplitude as shown in Fig. 1(a). On the other hand, in case of Fig. 1(b), the noise injection also causes increase the voltage. However, the voltage increase causes a phase shift and it cannot be recovered even though the amplitude is stable. Thus, the noise sensitivity of Fig. 1(b) is higher than that of Fig. 1(a).

As mentioned above, the sensitivity depends on the phase of the voltage waveform. The ISF becomes zero at the peaks of the voltage waveform, and takes a maximum value at zero-crossing points.

B. Class-C VCO

According to the discussion in the above section, the current of oscillators should be conducted at the timings when the ISF

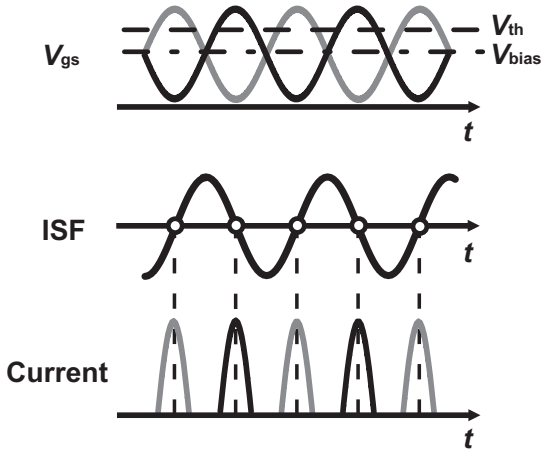

Fig. 2. Operation of class-C VCO.

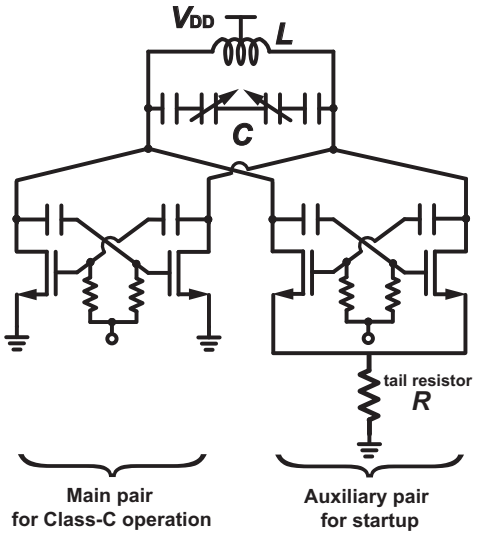

Fig. 3. Resistor added dual-conduction class-C VCO.

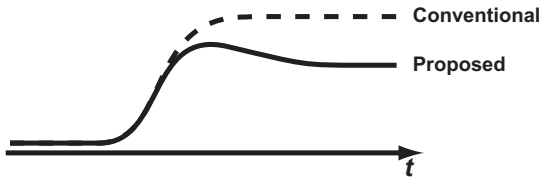

Fig. 4. Current of the auxiliary pair.

becomes zero, and the class-C VCO realizes such the ideal current conduction [1], [2].

The class-C VCO has two features. One is the tail capacitor (C_{tail}), which makes the current waveform sharp. The other is the independent gate bias (V_{bias}), and it is set lower than the threshold voltage. Fig. 2 shows the current waveform. The black line shows the waveform of the left transistor, and the gray line shows that of the right transistor. Since the gate bias (V_{bias}) is set lower than the threshold voltage (V_{th}), the conduction time becomes shorter than the half period. The shorter conduction time and the impulse-shape current waveform improve the phase noise, thanks to their effective ISF.

To improve the phase noise, the gate bias should be set as low as possible. However, the lower gate bias causes the startup problem. To turn on a transistor, the amplitude has to satisfy Eq. (1).

$$\begin{aligned} V_{\mathrm{bias}} + A_{\mathrm{t}} &> V_{\mathrm{th}} \\ A_{\mathrm{t}} &> V_{\mathrm{th}} - V_{\mathrm{bias}} \end{aligned} \tag{1}$$

where V_{bias} is the gate bias of the transistor, V_{th} is the threshold voltage, and A_{t} is the amplitude. At the startup state, since A_{t} is very small, it is difficult to obtain the transconductance with lower V_{bias}. Actually, the oscillators can start oscillating by the sub-threshold current of CMOS transistors. However, it is not so robust. On the other hand, lower V_{bias} is required to improve the phase noise performance. Thus, there is a trade-off between the phase noise and the startup robustness. This is called the startup problem.

III. Dual-Conduction Class-C VCO

A. Dual-conduction class-C VCO

The conventional single-conduction class-C VCO has the startup problem, and it cannot perform well with low supply voltages. To solve the problem, the authors have proposed the dual-conduction class-C VCO [3]. It has two pairs of cross-coupled transistors. One is a main pair for class-C operation, the other is an auxiliary pair for the startup. The gate bias of the auxiliary pair is higher than that of the main pair. Thanks to the auxiliary pair, this VCO can start oscillating at the ultra-low supply voltage such as 0.20 V [3]. Furthermore, the gate bias of the main pair can be set much lower than the single-conduction class-C VCO. Hence, the dual-conduction class-C VCO can operate with low phase noise at ultra-low supply voltages.

However, the auxiliary pair degrades the FoM for two reasons. One reason is the problem of increased power consumption. The auxiliary pair even continues to operate after the VCO starts the class-C operation. Thus, it consumes additional power. The other reason is the problem of the phase noise. Owing to the higher gate bias, the conduction time becomes longer. The longer conduction time degrades the phase noise.

B. The proposed circuit

As mentioned above, the auxiliary pair degrades the FoM. Hence, the auxiliary pair should be suppressed after the VCO enters a steady oscillation state.

Eq. (2) gives the current of the transistor in the saturation region.

$$I_{\mathrm{ds}} = \frac{\mu C_{\mathrm{ox}}}{2} \frac{W}{L} \left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)^2 \left(1 + \lambda V_{\mathrm{ds}}\right) \tag{2}$$

where I_{ds} is the current of the transistor, μ is the charge-carrier effective mobility, C_{ox} is the gate oxide capacitance

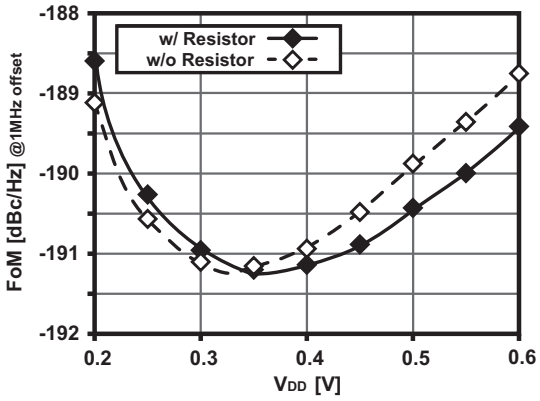

Fig. 5. Simulation results of the FoM.

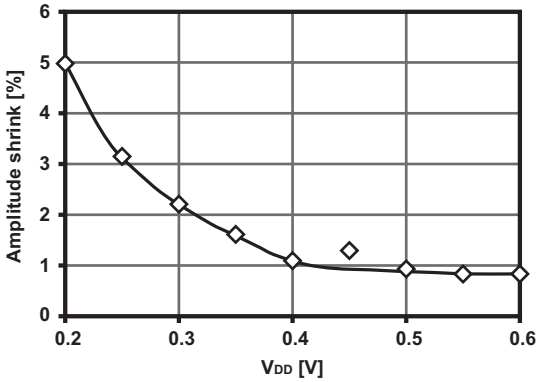

Fig. 6. Amplitude shrink rate.

per unit area, W is the gate width, L is the gate length, $V_{\rm gs}$ is the gate-source voltage, $V_{\rm th}$ is the threshold voltage, λ is the channel-length modulation parameter, and the $V_{\rm ds}$ is the drain-source voltage. According to Eq. (2), $V_{\rm gs}$ and $V_{\rm ds}$ should be reduced to suppress the auxiliary pair current. In other words, the source voltage should be increased to reduce the pair current. To increase the source voltage, a resistor is added to the source node as shown in Fig. 3. Once the VCO starts oscillating, the current becomes larger. Since the source voltage becomes higher due to the resistance, $V_{\rm gs}$ and $V_{\rm ds}$ are reduced. Hence, the current of the auxiliary pair reduces as shown in Fig. 4.

C. Simulation results

Figs. 5 and 6 show the simulation results of a 10 Ω resistor added to the dual-conduction class-C VCO using 0.18 μm CMOS parameters. Fig. 5 shows a comparison between the conventional and proposed dual-conduction class-C VCOs. The FoM is calculated by Eq. (3) [6], which can be improved with more than 0.35 V supply voltage.

$$\mathrm{FoM} = \mathcal{L}(f_{\rm offset}) - 20\log_{10}\left(\frac{f_0}{f_{\rm offset}}\right) + 10\log_{10}\left(\frac{P_{\rm DC}}{1[\mathrm{mW}]}\right) \tag{3}$$

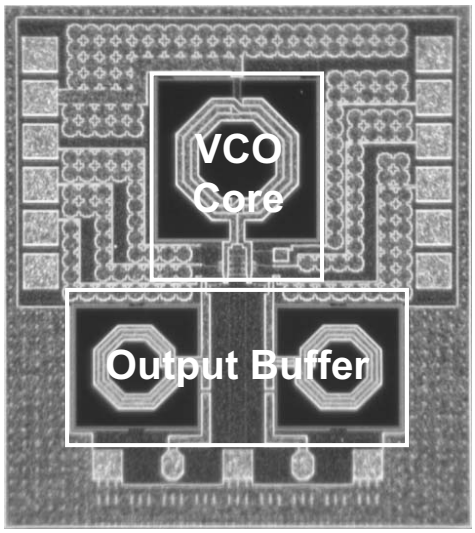

Fig. 7. Chip micrograph.

where $\mathcal{L}(f_{\rm offset})$ is the phase noise, $f_{\rm offset}$ is the offset frequency, f_0 is the oscillation frequency, and $P_{\rm DC}$ is the power consumption. To determine why the FoM do not improve below 0.35 V supply voltage, the amplitude change is investigated. Fig. 6 shows the amplitude shrink rate calculated by Eq. (4).

$$(\text{Amplitude shrink rate})\,[\%] = \frac{A_{\rm t(0\Omega)} - A_{\rm t(10\Omega)}}{A_{\rm t(0\Omega)}} \times 100 \tag{4}$$

where $A_{\rm t(0\Omega)}$ is the amplitude without the resistor, and $A_{\rm t(10\Omega)}$ is the amplitude with 10 Ω resistor. Since the phase noise is calculated by Eq. (5) [4], reduction of the amplitude degrades the phase noise and the FoM.

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log_{10}\left[\frac{2F\mathrm{k}T}{P_{\rm sig}} \cdot \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{5}$$

where $\Delta\omega$ is the offset frequency, F is the noise factor, k is Boltzmann constant, T is the absolute temperature, $P_{\rm sig}$ is the signal power, ω_0 is the oscillation frequency, and Q is the Q-factor of the oscillator.

Since excessive reduction of the amplitude degrades the phase noise as shown in Figs. 5 and 6, the resistance should be carefully optimized.

IV. Measurement Results

The proposed VCO is fabricated by using a 0.18 μm CMOS technology. Fig. 7 shows the chip micrograph, and the core area is 0.18 mm^2. The VCO can oscillate at 5.4 GHz with 0.20 V supply voltage. The power consumption is 96 μW. The phase noise is -102 dBc/Hz at 1 MHz offset, and the FoM is -187 dBc/Hz. Fig. 8 shows the measurement result of the phase noise, and Fig. 9 shows the measurement result of the FoM. In Fig. 5 (simulation), the FoM takes minimum value at 0.35 V. However, in Fig. 9 (measurement), it becomes around

TABLE I
PERFORMANCE SUMMARY.

	[1]	[7]		[3]		This work	
Technology	CMOS 0.13μm	CMOS 0.18μm		CMOS 0.18μm		CMOS 0.18μm	
Supply voltage[V]	1.0	0.50	0.35	0.30	0.20	0.50	0.20
DC Power[μW]	1300	570	1460	159	114	630	**96**
Frequency[GHz]	4.9	3.8	1.4	4.5		5.4	
Phase noise[dBc/Hz]	-130 @3MHz offset	-119 @1MHz offset	-129 @1MHz offset	-109 @1MHz offset	-104 @1MHz offset	-113 @1MHz offset	-102 @1MHz offset
FoM[dBc/Hz]	-196	-193	-190	-190	-187	-190	-187
Topology	Class-C	Transformer feedback		Dual-conduction class-C		Dual-conduction class-C	

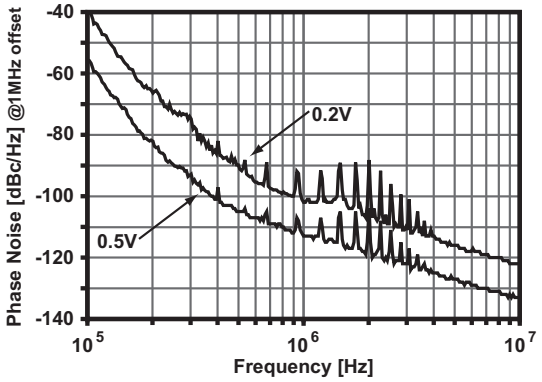

Fig. 8. Measurement results of the phase noise.

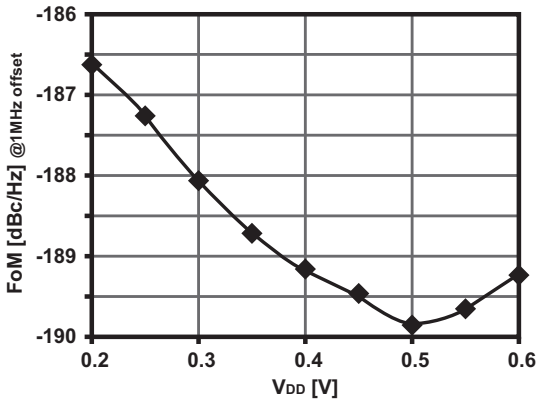

Fig. 9. Measurement result of the FoM.

0.50 V. That is caused by the series parasitic resistor of the tail resistor. It reduces the current more than that of the simulation. Therefore, the signal power is reduced more, and then the phase noise and the FoM is degraded below 0.50 V.

Table I summarizes state-of-the-art results of LC-VCOs. The proposed circuit can realize very low power consumption with an excellent phase noise performance.

V. CONCLUSION

In this paper, a new dual-conduction class-C VCO is proposed, which has an additional tail resistor to reduce power consumption of the auxiliary pair at the steady oscillation state. The proposed circuit can successfully perform at low supply conditions, and it can oscillate at 5.4 GHz with FoM of -187 dBc/Hz. It consumes only 96 μW from a 0.20 V supply voltage. Thus, the proposed class-C VCO realizes an ultra-low power operation with the excellent phase noise performance.

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