A 60 GHz CMOS Power Amplifier Using Capacitive Cross-Coupling Neutralization with 16 % PAE

Hiroki Asada, Kota Matsushita, Keigo Bunsen, Kenichi Okada, and Akira Matsuzawa
Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo, 152-8552, Japan
Tel & Fax: +81-3-5734-3764
Email: asadah@ssc.pe.titech.ac.jp

***Abstract*— This paper presents a 60 GHz power amplifier using a capacitive cross-coupling neutralization. The capacitive cross-coupling neutralization contributes to improve power gain and reverse isolation. Moreover, the transmission line for matching networks is optimized to achieve highly power-efficient amplifier. The 3-stage differential power amplifier is fabricated in a 65 nm CMOS process and evaluated with 1.2 V power supply. The power amplifier achieves power gain of 23.2 dB, output power of 10 dBm at 1 dB compression point, saturated output power of 14.6 dBm, peak PAE of 16.3 %, and power consumption of 135 mW.**

I. Introduction

Recently, researches of high-speed wireless communications in 60 GHz ISM band are actively conducted. In the 60 GHz frequency range, a wide band width can be used without license for wireless personal network in many countries. 60 GHz circuits have been implemented by using compound semiconductor processes so far because of highly cut-off frequency and high-voltage operation. However, the cut-off frequency of CMOS transistor has been increased in recent days, and CMOS circuits has obtained 60 GHz capability, which contributes to realize a 60 GHz wireless communication which can be implemented in consumers' mobile terminals. To achieve this, one of the challenges is design of 60 GHz power amplifier. It is difficult to obtain a high gain and a high stability by CMOS transistors. Many researchers are studying this issue [1], [2]. In this work, a capacitive cross-coupling neutralization and low-loss transmission line are applied to enhance a power gain and a stability. Three kinds of guided micro-strip lines are utilized to achieve low-loss and highly efficient amplifier.

II. Capacitive Cross-Coupling Neutralization

One of the most important issues for a 60 GHz CMOS power amplifier is low reverse isolation. Transistors in the power amplifier are enormously large, so the parasitic gate-to-drain capacitance is also enormous, *e.g.*, several hundred fF. The capacitance lowers the reverse isolation, the power gain, and the stability. Fig. 1 shows a simplified circuit to explain the capacitive cross-coupling neutralization[1]. A cross-coupled capacitor $C_{\rm x}$ between gate and drain of the opposite-side transistor works as -$C_{\rm x}$, and cancels the parasitic gate-to-drain capacitance and improves the reverse isolation.

Fig. 2 shows the small signal equivalent circuit of capacitive cross-coupling neutralization. Y-parameter can be written as follows.

$$Y_{11} = \frac{1}{R_{\rm G}} + j\omega C_{\rm GS} + j\omega(C_{\rm GD} + C_{\rm x}) \quad (1)$$

$$Y_{12} = -j\omega(C_{\rm GD} - C_{\rm x}) \quad (2)$$

$$Y_{21} = g_{\rm m} - j\omega(C_{\rm GD} - C_{\rm x}) \quad (3)$$

$$Y_{22} = \frac{1}{R_{\rm D}} + j\omega C_{\rm DB} + j\omega(C_{\rm GD} + C_{\rm x}) \quad (4)$$

where $C_{\rm x}$ is the cross-coupled capacitance, $C_{\rm GD}$ is the gate-to-drain capacitance, $C_{\rm GS}$ is the gate-to-source capacitance, $C_{\rm DB}$ is the drain-to-bulk capacitance, $R_{\rm G}$ is the gate resistance, $R_{\rm D}$ is the drain resistance, and $g_{\rm m}$ is the transconductance. Eq. (2) shows that effective gate-to-drain capacitance can be reduced by the capacitive cross-coupling neutralization, which means the reverse isolation is increased by cross-coupled capacitors.

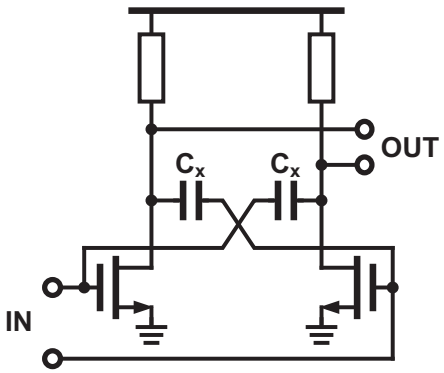

Fig. 1. Capacitive cross-coupling neutralization.

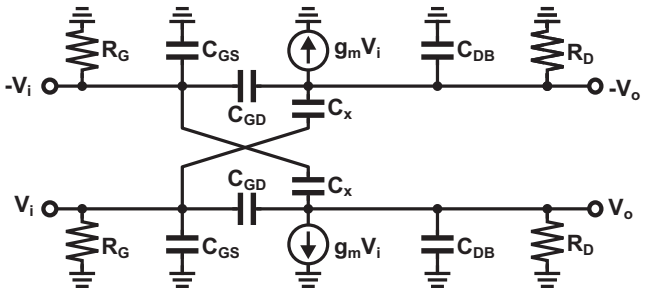

Fig. 2. Small signal equivalent circuit of CCC.

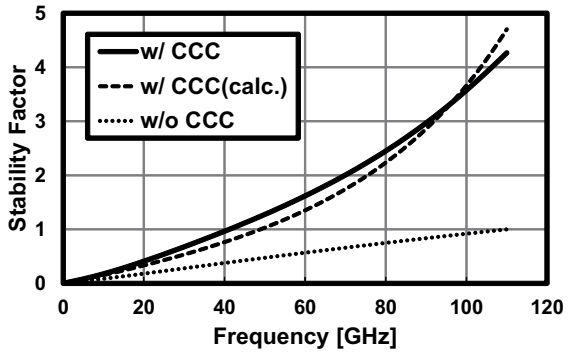

Fig. 3. Simulated stability factor.

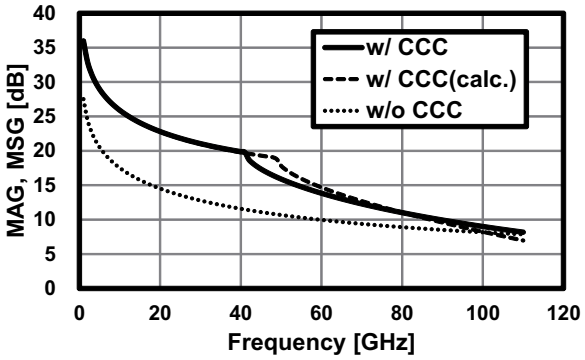

Fig. 4. Simulated maximum gain.

A. Stability

The amplifier is unconditionally stable when the stability factor is larger than one[3]. The stability factor k can be expressed as

$$k = \frac{2\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|}. \tag{5}$$

Using Eqs. (1)-(4), the stability factor of capacitive cross-coupling amplifiers can be expressed by the following equation.

$$k = \frac{2 + \omega^2(C_{\mathrm{GD}} - C_{\mathrm{x}})^2 R_{\mathrm{G}} R_{\mathrm{D}}}{\omega|C_{\mathrm{GD}} - C_{\mathrm{x}}|R_{\mathrm{G}}R_{\mathrm{D}}\sqrt{\omega^2(C_{\mathrm{GD}} - C_{\mathrm{x}})^2 + {g_{\mathrm{m}}}^2}} \tag{6}$$

According to Eq. (6), when C_{x} is equal to C_{GD}, the stability factor is the largest. Fig. 3 shows simulation results of the stability factor. From the graph, capacitive cross-coupling can improve the stability across entire frequency, and the theoretical value and the simulation result are matched very well.

B. The Maximum Available Gain And The Maximum Stable Gain

The maximum available gain is the theoretical maximum power gain[3]. It is obtained when the input and output ports are simultaneously matched to their conjugate impedances. The maximum available gain G_{MA} can be expressed as

$$G_{\mathrm{MA}} = \left|\frac{Y_{21}}{Y_{12}}\right|(k - \sqrt{k^2 - 1}). \tag{7}$$

The maximum available gain of capacitive cross-coupling amplifiers can be expressed by the following equation by using Eqs. (1)-(4).

$$G_{\mathrm{MA}} = \frac{\sqrt{\omega^2(C_{\mathrm{GD}} - C_{\mathrm{x}})^2 + {g_{\mathrm{m}}}^2}}{\omega|C_{\mathrm{GD}} - C_{\mathrm{x}}|}(k - \sqrt{k^2 - 1}) \tag{8}$$

When the stability factor is less than one, the maximum stable gain is defined instead of the maximum available gain. The maximum stable gain G_{MS} is defined as the maximum available gain with k=1. The maximum stable gain of capacitive cross-coupling amplifiers can also be expressed by the following equation.

$$G_{\mathrm{MS}} = \left|\frac{Y_{21}}{Y_{12}}\right| \tag{9}$$

$$= \frac{\sqrt{\omega^2(C_{\mathrm{GD}} - C_{\mathrm{x}})^2 + {g_{\mathrm{m}}}^2}}{\omega|C_{\mathrm{GD}} - C_{\mathrm{x}}|} \tag{10}$$

Eqs. (8) and (10) shows that the capacitive cross-coupling neutralization also contributes to improve the maximum available gain and the maximum stable gain.

Fig. 4 shows the maximum available gain and the maximum stable gain in simulation. From the graph, capacitive cross-coupling can improve the maximum available gain about 5 dB at 60 GHz, and the theoretical value and the simulation result are matched very well.

III. Transmission Line Optimization

The loss of matching networks is a serious issue of the power amplifier. In this work, a Guided Micro-Strip Line(GMSL) is used to build matching networks. GMSL is a micro-strip line with a wall of GND as shown in Fig. 5. To optimize a transmission line, three GMSLs are compared. The first one has a narrow line whose width is 5 μm. The second one has a wide line whose width is 10 μm. The last one uses two metal layers and has the same width as the second one, which consists of top Al layer and beneath Cu layer as a signal line.

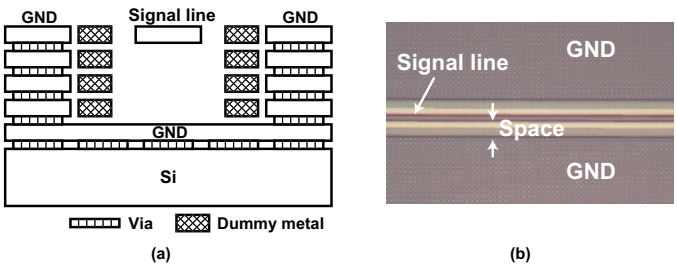

Fig. 5. Guided micro-strip line (a) structure (b) die photo.

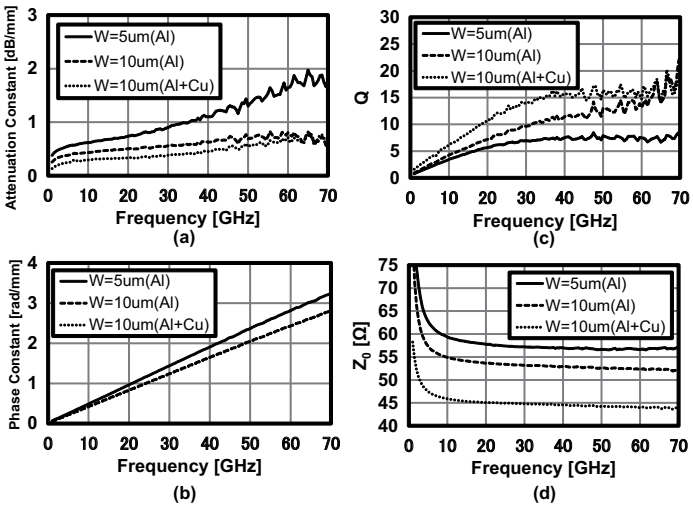

Fig. 6. (a)the attenuation constance (b)the phase constance (c)Q-factor (d)the characteristic impedance

Fig. 6 shows the measurement results of attenuation constance, phase constance, Q-factor, and characteristic impedance. The narrow one has a higher loss than the others, and Q-factor of the thick line is the highest. However, the characteristic impedance of the thick line is too lower to convert impedances to 50 Ω. These three lines have to be chosen depending on requirements, and the second one is mainly used in this work.

IV. Power Amplifier Design

A power amplifier design is shown in Fig. 7. The differential power amplifier consists of three amplifier stages. The first stage and the second stage are designed as a differential amplifier using the capacitive cross-coupling neutralization, and the final stage is designed as a pseudo differential amplifier with class-A biasing. Transistors in the 3-stage PA have a finger width of 2 μm for a better power gain[4], and the total gate width of the final stage is 80 μm.

The guided micro-strip line is used for matching network. The transmission line is low-loss, which has a loss of 0.8 dB/mm. The output matching is optimized according to the load-pull simulation. And the de-coupling is implemented MIM transmission line(MIM TL)[5]. It is power line with capacitor array to lower the characteristic impedance and it is characterized as a scalable transmission line.

V. Measurement Results

The power amplifier is fabricated in a 65 nm CMOS technology. The die photo is shown in Fig. 8. The chip size was $1.0\times0.6\,\mathrm{mm}^2$. The test circuit is measured by a 4-port network analyzer, and the measured 4-port S-parameters are converted to mixed-mode ones. For differential measurement, balun probes are used.

Fig. 9 shows the power gain. The measured power gain at 60 GHz is 23.2 dB. Fig. 10 shows the output power, the power gain and PAE(Power Added Efficiency). The solid line is the output power, the dashed line is PAE, and the dotted line is the power gain. The measured output power at 1 dB compression point and the measured saturated output power are 10.0 dBm and 14.6 dBm, respectively. The measured PAE at 1 dB compression point and the measured peak PAE are 7.9 % and 16.3 %, respectively. The power amplifier consumes 135 mW from a 1.2 V supply.

Table I summarizes the performance of the 60 GHz CMOS PA presented in this paper and also shows the comparison with other 60 GHz PAs.

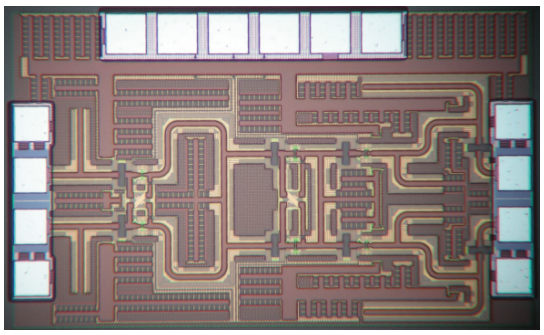

Fig. 8. Die photo.

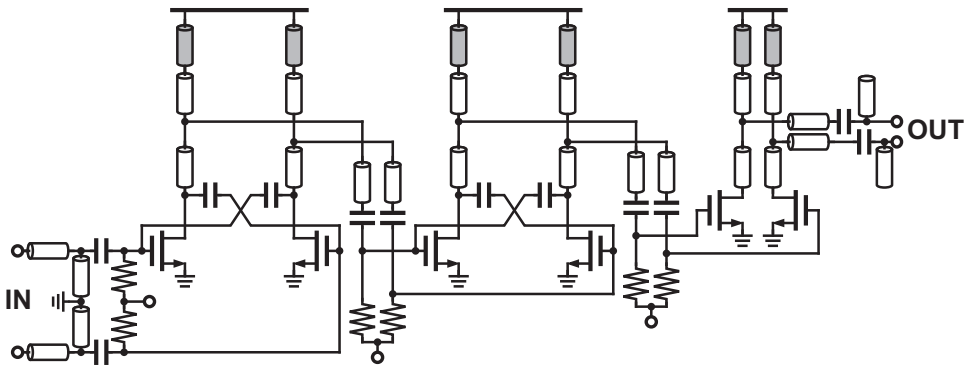

Fig. 7. Capacitive cross-coupling power amplifier.

TABLE I

PERFORMANCE COMPARISON.

	Technology	Power Gain[dB]	P_{1dB}[dBm]	P_{sat}[dBm]	Peak PAE[%]	Power[mW]	V_{DD}[V]
[1]	65 nm	16	2.5	11.5	11	43.5	1.0
[2]	65 nm	19.2	15.1	17.7	11.1	480	1.0
[5]	90 nm	8.3	8.2	10.6	5	228.6	1.0
[6]	90 nm	20.6	18.2	19.9	14.2	-	1.2
[7]	90 nm	10	8.8	12.6	6.9	211	1.0
[8]	90 nm	4.4	12.1	14.2	5.8	145	1.0
[9]	90 nm	30	10.3	13.8	12.6	178	1.8
[10]	90 nm	20	8.2	12	9	146	1.2
[11]	90 nm	25	5	8	7	110	1.5
[12]	90 nm	17	5.1	8.4	5.8	54	1.8
[13]	90 nm	15.2	10	11	8.2	150	1.0
[14]	90 nm	5.5	9	12.3	8.8	-	1.0
[15]	65 nm	14.3	11	16.6	4.9	732	1.2
This Work	65 nm	23.2	10.0	14.6	**16.3**	135	1.2

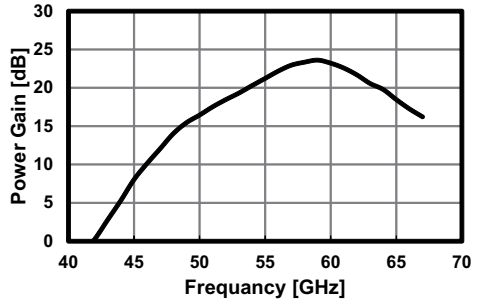

Fig. 9. Power gain.

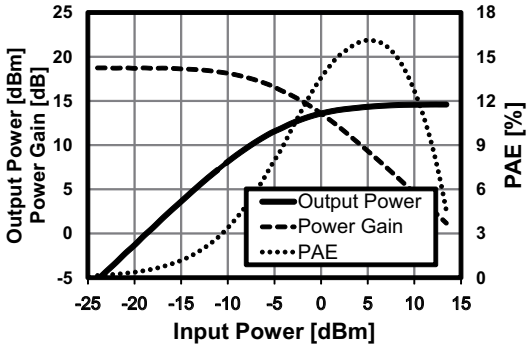

Fig. 10. Output power, power gain and PAE.

VI. CONCLUSION

This paper presents a 60 GHz power amplifier using the capacitive cross-coupling neutralization with the optimized transmission line. The capacitive cross-coupling neutralization and the low-loss transmission line enhance power gain and stability. The 3-stage differential power amplifier in 65 nm CMOS achieves power gain of 23.2 dB, saturated output power of 14.6 dBm, peak PAE of 16.3 % and power consumption of 135 mW.

ACKNOWLEDGMENT

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