A 20GHz ILFD with Locking Range of 31% for Divide-by-4 and 15% for Divide-by-8 Using Progressive Mixing

Ahmed Musa, Kenichi Okada and Akira Matsuzawa
Dept. Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27, Ookayama, Meguro-ku, Tokyo 152-8552 Japan.
Tel: +81-3-5734-3764, Fax: +81-3-5734-3764, E-mail: musa@ssc.pe.titech.ac.jp

Abstract—This paper proposes Progressive Mixing Injection Locked Frequency Divider (PMILFD) technique that enhances the locking range for higher division ratios. The wide locking range is achieved through the use of progressive mixing approach contrary to the conventional method that uses direct mixing to generate the injection signal. This allows for the use of lower and much stronger harmonics in the mixing process resulting in a stronger injection effect. Two 20GHz PMILFDs were designed based on this approach to perform division by 4 and 8 using 65nm CMOS process. The divide-by-4 PMILFD achieves a 7.9GHz (31.4%) locking range and the divide-by-8 achieves 3.4GHz (15.5%) while consuming 3.9mW and 7.1mW, respectively.

Fig. 1. High frequency synthesizer architecture

I. INTRODUCTION

Applications requiring high data rate transfer has been growing lately especially in the area of multimedia applications like high definition video. Since the lower frequency band around few GHz is already crowded with standards, higher frequency bands that has lower number of standards became more attractive. Moreover, since an affordable process like CMOS has enough bandwidth to cover these bands, implementation cost is reduced .

To design such high frequency transceivers, high frequency PLL systems like the one in Fig.1 are needed to generate the Local Oscillator (LO) signal. These PLLs employ frequency dividers to downconvert the VCO signal since the reference frequency is usually much lower than the VCO frequency. Usually, digital counters are used as frequency dividers in PLLs operating at few GHz frequency. However, for much higher frequency analog dividers are employed. They are implemented as Current Mode Logic (CML) dividers and Injection Locked Frequency Dividers (ILFD). CML dividers are more robust and have a wide locking range for a divide-by-2 operation but have a high power consumption. They are often cascaded [1] to achieve a frequency where digital dividers can operate. ILFDs on the other hand consume much less power and can divide by higher than 2, which further saves power. However, they suffer from a narrow locking range especially for division ratios that are higher than 2. Several ILFDs with a divide ratio of 4 have been reported in literature that use various methods to improve the locking range. These methods include cascading two divide by 2
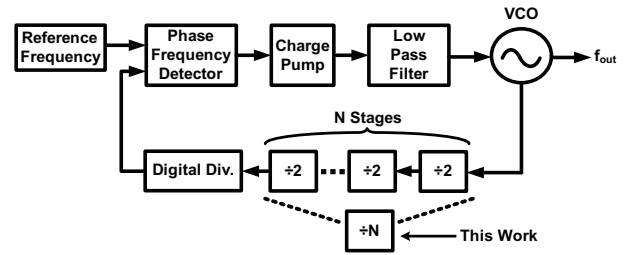
ILFDs [2] [3] [4], varactor tuning [5], inductive peaking [6] and filtering [7]. Still, these dividers have relatively narrow locking range. For higher division ratio ILFDs, locking range is much narrower [8] [9] which make them not suitable for practical applications. However, all these ILFDs use the same principle of direct mixing to generate the correct harmonic to be injected into the oscillator for locking. As this method is not suitable for higher division ratios, progressive mixing is proposed to enhance the locking range for higher division ratios. In addition, the proposed method avoids phenomenas like locking range overlapping were regular ILFDs fail to operate or false locking in which an ILFD would lock to a false division ratio due to PVT variations that would change the free-running frequency.

II. INJECTION LOCKING

A. Conventional ILFD Model

Conventional ILFDs follow a model similar to the one shown in Fig.2. In this model, the fundamental frequency f_o passes through the nonlinear transconductance of the transistor, which generates many higher order harmonics. When the oscillator is not injected, these harmonics will be much attenuated by the built-in LPF in the oscillator. However, in the case of an injection applied to the oscillator, these harmonics will mix with the injected signal and many additional harmonics are generated. If one of these harmonics is close to the oscillator free-running frequency and has enough power, the oscillator frequency will be pulled and it will lock to that harmonic [10]. This is mainly a direct conversion where
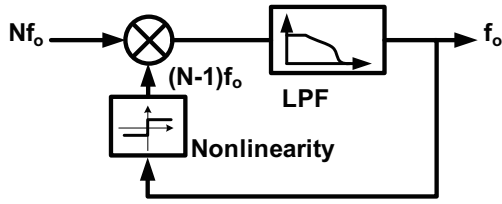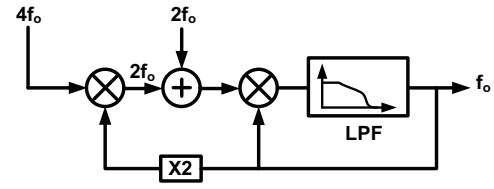
Fig. 2. Conventional ILFD model

(a) Two step divide-by-4 model

(b) Three step divide-by-8 model

Fig. 3. Proposed PMILFD model

the $(N-1)^{th}$ harmonic is mixed with the injected signal at the Nth harmonic to generate a harmonic that is close to the oscillator fundamental harmonic and thus pull it. Therefore, as N becomes higher, the locking range becomes narrower since the $(N-1)^{th}$ is much weaker. Moreover, level of the desired harmonic of the ILFD cannot be controlled since the generation process is not linear and is affected by many factors like topology, PVT variations and mismatch. As a consequence, any change in the level of other harmonics might disrupt the locking process which reduces the locking range and might limit the injection power required for a certain division ratio [7].
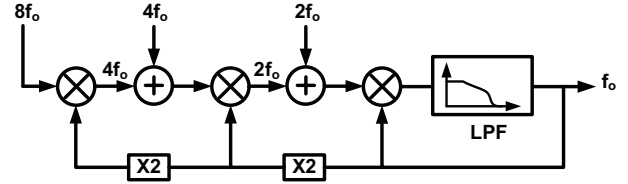
B. Proposed ILFD Model

The proposed PMILFD uses a multistep conversion model as shown in Fig.3 for a two-step divide-by-4 and a three-step divide-by-8 configuration. In this configuration the injected signal at the Nth harmonic is mixed with the $(\frac{N}{2})^{th}$ harmonic of the oscillator fundamental frequency and then again by the $(\frac{N}{4})^{th}$ harmonic and so on $\log_2 N$ times until a harmonic that is close to the oscillator fundamental is generated. So for a divide-by-4 configuration as shown in Fig.3 (a), the injected signal is mixed first with the second harmonic and again by the fundamental to generate a harmonic that is close to the fundamental in order to pull and lock it. As for the divide-by-8 configuration shown in Fig.3 (b), the injected signal is mixed with the fourth harmonic and then again by the second and finally by the fundamental to generate a signal that is close to the fundamental to lock it. The main advantage is that the injected signal is mixed with $(\frac{N}{2})^{th}$ harmonic instead of the conventional $(N-1)^{th}$ since the former is much stronger than the later and thus will produce a stronger injection signal. The figure shows that in order to implement a PMILFD, higher harmonics of the fundamental need to be generated. This can be performed by using a push-push architecture that combines N phases of a signal to cancel all the harmonics up to the N−1 and to generate and enhance the Nth harmonic. Using this approach will filter out all the lower and much stronger harmonics that would disrupt the injection process and will leave the desired one that will be mixed with the injected signal. Therefore, overlapping between division ratios is eliminated since the injected signal will be mixed with the strongest harmonic at each mixing stage.

A feature of such an architecture is that the intermediate stages can also be used to inject a signal for lower division ratios. Fig.3 (a) shows that by switching the injection point from $4f_o$ input to $2f_o$ input, the ILFD can be used as a divide-by-2 where both can have a wide locking range. Also, overlapping between the locking ranges at different input would not disrupt locking but allows the PMILFD to be used as a dual modulus divider without tuning.

III. CIRCUIT IMPLEMENTATION

Fig.4 shows the circuit topology that is used to implement divide-by-4 PMILFD. It consists of a four-stage differential ring oscillator. The delay cell diagram is depicted in Fig.4 (b) where PMOS transistors are used as a variable resistor load for frequency tuning. The common node at the bottom of
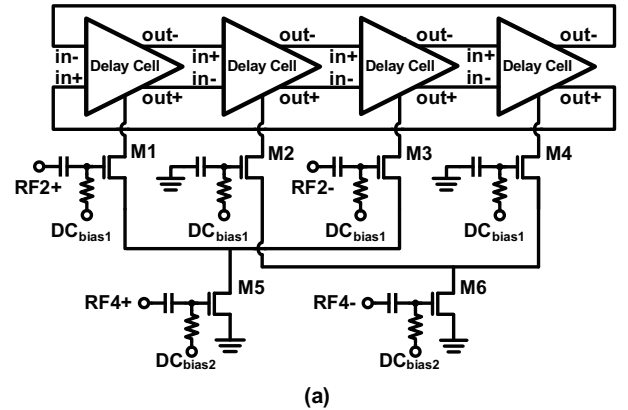
(a)
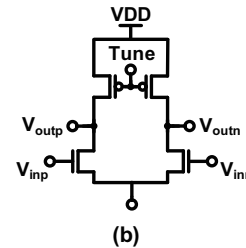
(b)

Fig. 4. Proposed PMILFD divide-by-4 circuit: (a) Complete (b) Delay cell

the delay cell where the tail transistors is connected oscillates at twice the fundamental and it is the point where push-push operation takes place. In a conventional ILFD topology, the tail transistors M1-M5 source terminals are connected to ground. However, in the proposed topology the source of M1 is connected to the source of M3 to the tail transistor M5 since they operate in a differential fashion at the second harmonic. The sources of M2 and M4 are also connected together with M6 in a similar fashion. This makes M1-M4 form an oscillator that is running at twice the fundamental where it will be suitable to inject the fourth harmonic at RF4 input at the tail transistors M5-M6. Also, as mentioned in the previous section, intermediate stages can be used as an injection point for lower division ratios. Therefore, the gate of transistors M1 and M3 were used as a second input (RF2) if the PMILFD is to be used as a divide-by-2 circuit.

For the divide-by-8 PMILFD, a similar structure is used that consists of an eight-stage differential ring oscillator with a similar delay stage structure to the divide-by-4 one. The tail transistors of each delay stage were connected in a similar way as the divide-by-4 to generate the second harmonic at the first tail transistors. However, the second tail transistors were not connected to ground and instead connected together as the previous ones to create a differential oscillator running at the fourth harmonic with two additional tail transistors with sources that are connected to ground. The final tail transistors were used to inject the signal at the 8th harmonic to perform a divide-by-8 operation. As for the intermediate points of injection, only divide-by-4 (RF4) inputs were used due to a measurement setup limitation. However, theoretically, the divider can have three inputs for division by 8,4, and 2.

IV. MEASUREMENT RESULTS

The two PMILFD dividers were fabricated in a 65nm CMOS process to verify their operation. On-chip probing is used to measure both dividers where the differential input is generated using a 180° hybrid coupler. The divide-by-4 PMILFD consumes 3.9mW from a 1.2V supply and has a free-running tuning range from 2GHz to 8GHz. Fig.5 shows the locking range for divide-by-2 operation at RF2 input in the divide-by-4 PMILFD with 2.5GHz (53.7%) and up to 11.6GHz (92.1%) locking range at the highest frequency. The divide-by-4 input (RF4) has a 3.7GHz (39.7%) and up to 7.9GHz (31.4%) at the highest frequency around 20GHz as shown in Fig.6. Measurement also showed that there is an overlap between divide-by-2 operation with input applied to RF2 terminal and divide-by-4 operation with input applied to RF4 terminal. Since the overlap is at different inputs, the divider will only switch from divide-by-4 to divide-by-2 operation when the input terminal is switched from RF4 to RF2 contrary to the conventional divider that fails to operate in such a region. Fig.7 shows the locked spectrum at 5.57GHz with an input 22.28GHz applied to RF4 terminal.

As for the divide-by-8 PMILFD, it consumes 7.1mA from a 1.2V supply and has a free-running tuning range from 1.6GHz to 5.3GHz. Locking range for divide-by-4 input (RF4), as
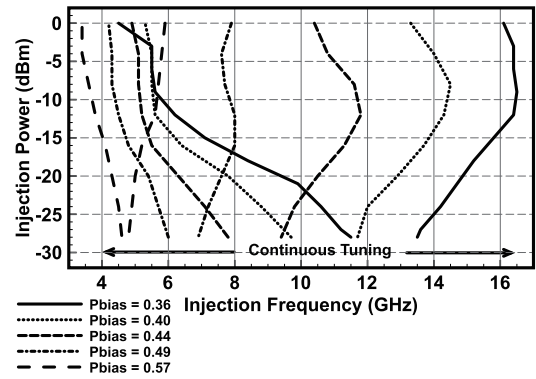

Fig. 5. Divide-by-2 locking and operation range with input applied to RF2 terminals of the divide-by-4 PMILFD
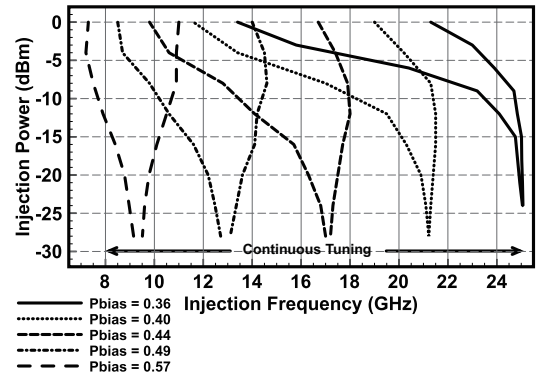

Fig. 6. Divide-by-4 locking and operation range with input applied to RF4 terminals of the divide-by-4 PMILFD
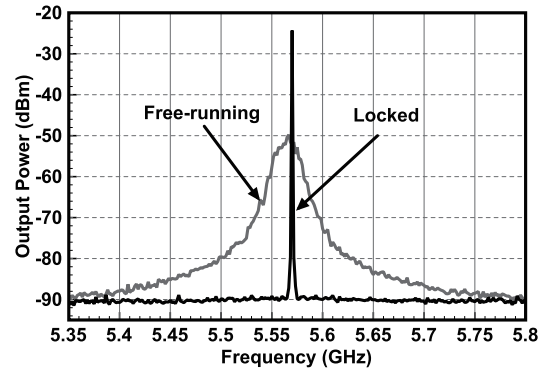

Fig. 7. Free-running and Locked PMILFD output spectrum

given in Fig.8, is 2.1GHz (30.4%) and up to 4GHz (31.8%) at the highest frequency. Fig.9 plots the locking range for the divide-by-8 input which shows a 2.1GHz (15.2%) and up to 3.8GHz (14.6%) locking range at the highest frequency around 23GHz. Frequencies higher than 26GHz and divide-by-2 measurements were not possible because of measurement setup and equipment limitations. Chip photo is given in Fig.10 in which the divide-by-4 PMILFD active area occupies 52μm×48μm and 66μm×86μm for the divide-by-8 one. Table I gives a comparison between this work and recently published ILFD papers with higher division ratios showing that both ILFDs achieve the widest locking range in their class.

TABLE I
PERFORMANCE COMPARISON BETWEEN PROPOSED WORK AND SIMILAR STATE-OF-THE-ART ILFDs

		PMILFD4	PMILFD8	[6]	[3]	[5]	[2]	[11]	[9]
CMOS Process		65nm	65nm	90nm	65nm	90nm	180nm	130nm	180nm
Supply [V]		1.2	1.2	0.5	1.2	0.5	2.5	1.2	18
Division Ratio		2, 4	4, 8	2, 4	2, 4	4	4	4	2, 4, 6, 8
Lock Range [GHz] (without tuning)	$\div 2$	**11.6 (92.1%)**	–	23 (34.3%)	12.1 (15.3%)	–	–	–	2 (55.6%)
	$\div 4$	**7.9 (31.4%)**	4 (31.8%)	6.5 (7.3%)	1.9 (2.4%)	1.6 (2.3%)	2.3 (5.8%)	5.4 (21.7%)	1.6 (22.2%)
	$\div 8$	–	3.8 (15.1%)	–	–	–	–	–	0.25 (1.7%)
Power [mW]		3.9	7.1	3.0	12.4 ($\div 4$)	2.75	30.8	6	6.8
Area [mm^2]		0.003	0.006	0.064	0.978	0.014	0.350	0.140	0.007

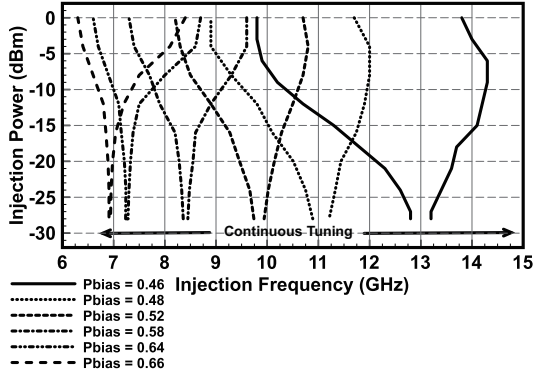Fig. 8. Divide-by-4 locking and operation range with input applied to RF4 terminals of the divide-by-8 PMILFD

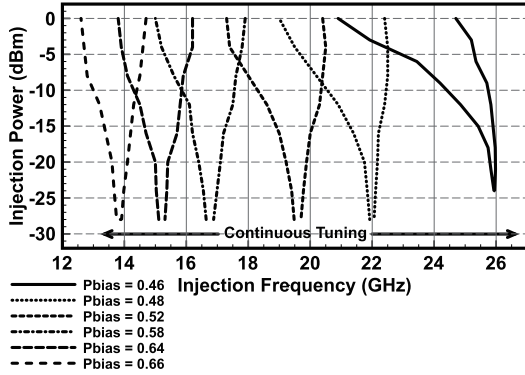Fig. 10. Divide-by-4 PMILFD (on the left) and divide-by-8 PMILFD (on the right) chip photos

Fig. 9. Divide-by-4 locking and operation range with input applied to the bottom tail transistors of the divide-by-8 PMILFD

V. CONCLUSION

This paper proposes the concept of Progressive Mixing ILFD (PMILFD) to widen the locking range of higher division ratios. This is done through a multistep downconversion of the injected signal instead of the conventional approach that uses direct conversion to generate the necessary harmonic. Using this concept, two 20GHz PMILFDs were designed to divide-by-4 in two steps and to divide-by-8 in three steps. Measurement results show that both dividers achieve a very wide locking range compared to recently reported ILFDs.

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