A 60 GHz 16 Gb/s 16QAM Low-Power Direct-Conversion Transceiver Using Capacitive Cross-Coupling Neutralization in 65 nm CMOS

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***Abstract*— This paper presents a 16QAM direct-conversion transceiver in 65 nm CMOS, which is capable of 60-GHz wireless standards. The capacitive cross-coupling neutralization contributes a high common-mode rejection and a high reverse isolation, and a fully-balanced mixer can improve the error vector magnitude due to the reduced local leakage. The maximum data rates with an antenna built in a package are 10 Gb/s in QPSK mode and 16 Gb/s in 16QAM mode and the transmitter and the receiver consume 181 mW and 138 mW, respectively.**

I. Introduction

According to IEEE 802.15.3c standard, four 2.16GHz-bandwidth channels are defined around the 60-GHz frequency, which are capable of achieving 3.5 Gb/s in QPSK and 7 Gb/s in 16QAM in raw data rate. This channel allocation is also common for IEEE 802.11ad, WiGig, WirelessHD, and ECMA standards. Recently, a couple of direct-conversion transceivers for the 60 GHz wireless communication have been reported[1], [2]. However, it is still difficult to realize the 16QAM direct-conversion even though 16QAM has to be supported for achieving a data rate of more than 5 Gb/s within a limited frequency bandwidth[3], [4]. This paper proposes a fully-balanced direct-conversion tranceiver to improve modulation quality of 16QAM. The capacitive cross-coupling neutralization[5] is employed to achieve a high common-mode rejection and a high reverse isolation, and a fully-balanced mixer can improve the error vector magnitude due to the reduced local leakage. The following sections present detailed implementation and experimental results.

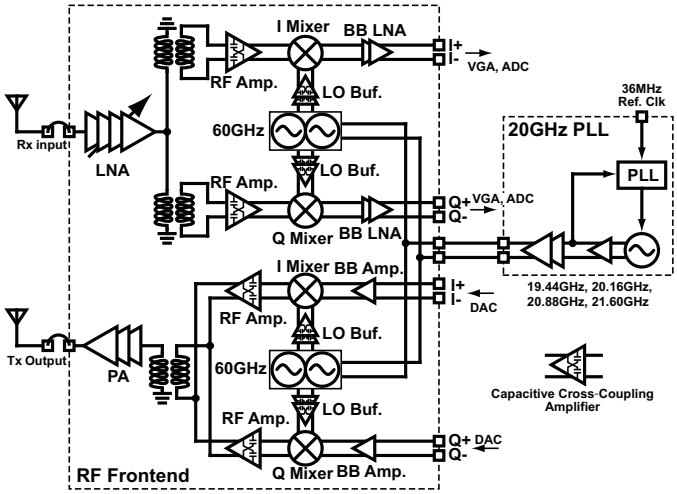


Fig. 1. Block diagram of the 60 GHz direct-conversion transceiver.

II. Transmitter

Fig. 1 shows the entire block diagram of the proposed 60-GHz transceiver, and it has a direct-conversion architecture due to energy and area efficiency. The transmitter consists of a 3-stage PA, I/Q active mixers and a quadrature oscillator. The 3-stage PA has a single-ended configuration, and other parts have fully differential configurations. A low-loss transmission line, which has a loss of 0.8 dB/mm, is used for matching network, and the de-coupling is implemented with MIM transmission line(MIM TL). Transistors in the 3-stage PA have a finger width of 2 μm, and the total gate width of the final stage is 80 μm. A double-balanced Gilbert mixer is used, and Fig. 2 shows a circuit schematic of the mixer. The output is connected to the 3-stage PA through a parallel-line transformer

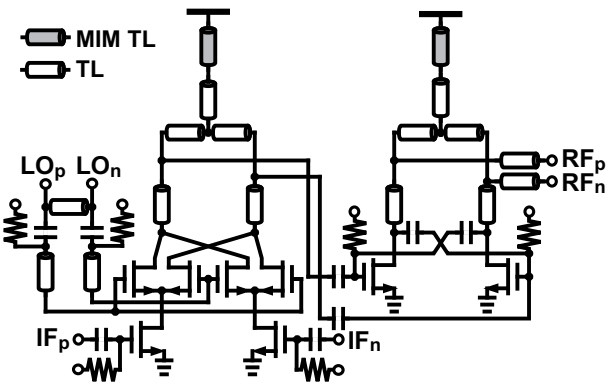


Fig. 2. Up-conversion mixer.

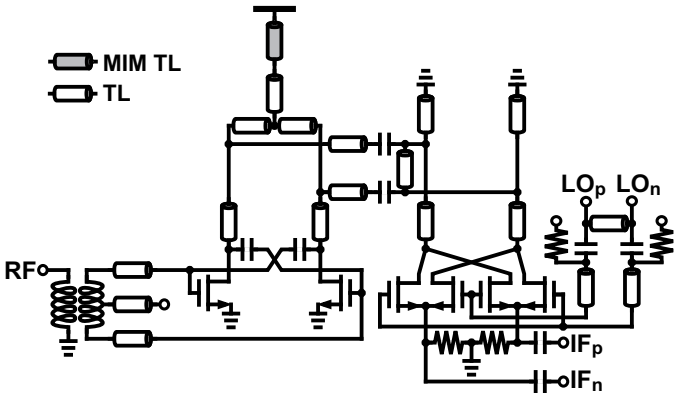


Fig. 3. Down-conversion mixer.

and a differential amplifier. The capacitive cross-coupling neutralization is applied to the differential amplifier. A cross-coupled capacitor between gate and drain of the opposite-side transistor cancels parasitic gate-to-drain capacitance and improves the reverse isolation. The high reverse isolation realizes high stability and gain enhancement. The common differential amplifier using a tail transistor cannot maintain a high CMRR at millimeter-wave frequency because of a parasitic capacitance at the drain of the tail transistor. Thus, the common-mode rejection is realized in the matching blocks of differential amplifiers. The shunt part in the matching block works as a short stub for a differential-mode signal because it forms a virtual ground. For a common-mode signal, it works as a open stub.

III. Receiver

The receiver design is shown in Figs. 3 and 4. The receiver consists of a 4-stage LNA, I/Q passive mixers, BB LNA, and a quadrature oscillator. The 4-stage LNA has a single-ended configuration and a CS-CS topology so that it improves the noise figure. Output of the LNA is connected to the passive mixer through the parallel-line transformer and a differential amplifier using the capacitive cross-coupling neutralization. A wideband low-noise BB LNA is used to compensate the conversion loss of the mixer, which is realized by a capacitive cross-coupled common-gate amplifier with a source-follower buffer.

IV. Local Oscillator

The LO consists of a quadrature injection-locked oscillator (QILO) and a 20 GHz PLL[6]. The QILO design is shown in Fig. 5. The QILO works as a frequency tripler with a 20 GHz injection-lock input, and it has a tail I/Q coupling, which is carefully designed to keep the I/Q balance robustly. Two quadrature oscillators are used, one for the transmitter and the other for the receiver, to maintain I/Q phase balance and avoid insertion loss in the 60 GHz LO distribution[7].

V. Experimental Results

The transceiver is fabricated in 65 nm CMOS technology. The die photo is shown in Fig. 6. The core areas of TX

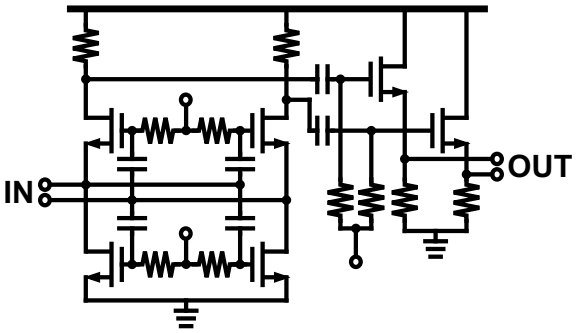


Fig. 4. BB LNA (capacitive cross-couple common-gate).

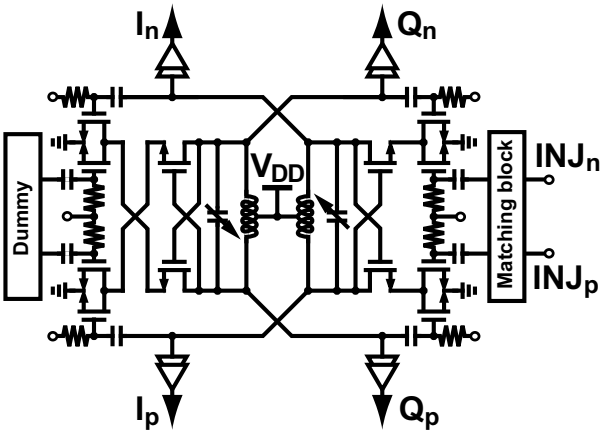


Fig. 5. Quadrature oscillator.

and RX are 2.5 mm^2 and 2.3 mm^2, respectively. A post-wall waveguide antenna[8] is implemented in a package. It is connected with the CMOS chip through a 270 μm bonding wire. The antenna in the BGA package has a 2dBi gain. Fig. 7 shows the measured spectrum in QPSK mode with the IEEE802.15.3c spectrum mask. The measured spectrum meets the IEEE802.15.3c standard. An arbitrary waveform generator (AWG) generates I/Q modulated signals, and an oscilloscope is used to evaluate the constellation, EVM, and BER with a built-in software. The measured EVM is from 3.87 % (-28.2 dB) for 16QAM mode, which uses decision feedback equalization (DFE) realized by the built-in software.

Fig. 8 shows the conversion gain of TX, which is 16 dB. The large-signal measurement is calibrated with the saturated output power, which is measured by a probe station. Fig. 9 shows the measured output power, which is 5.4 dBm at 1-dB compression. The transmitter consumes 181 mW from a 1.2 V supply. Fig. 10 shows the conversion gain of RX. The LNA realizes a gain control, and the conversion gain is 27 dB in high-gain mode and 17 dB in low-gain mode. The lower cut-off frequency of the BB amplifier is less than 4MHz. Fig. 11 shows the noise figure. The entire noise figure is less than 6.1 dB, and the measured IIP3 is -20 dBm. The receiver consumes 138 mW from a 1.2 V supply. The measured free-running frequency is from 55-63 GHz. The overall phase noise is -94.2 dBc/Hz@1MHz-offset at 60.48GHz, which is measured through the entire TX path.

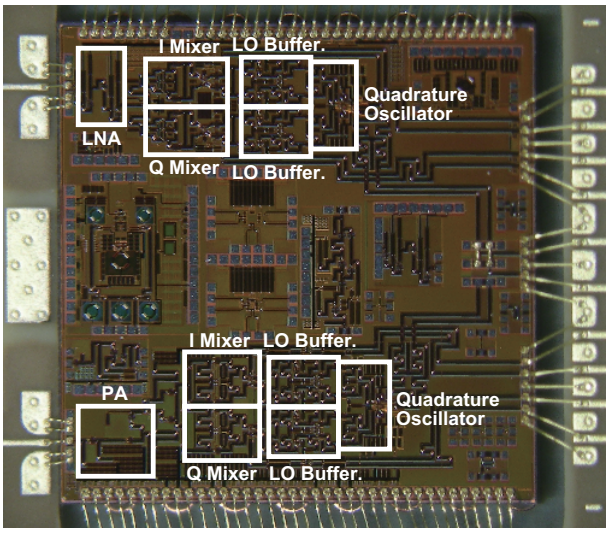


Fig. 6. Die micrograph.

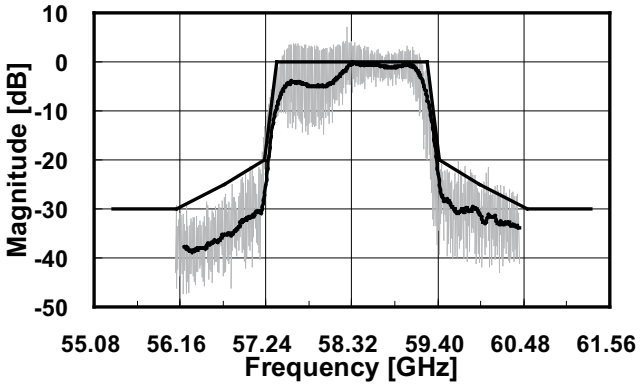


Fig. 7. Measured spectrum for QPSK at TX output.

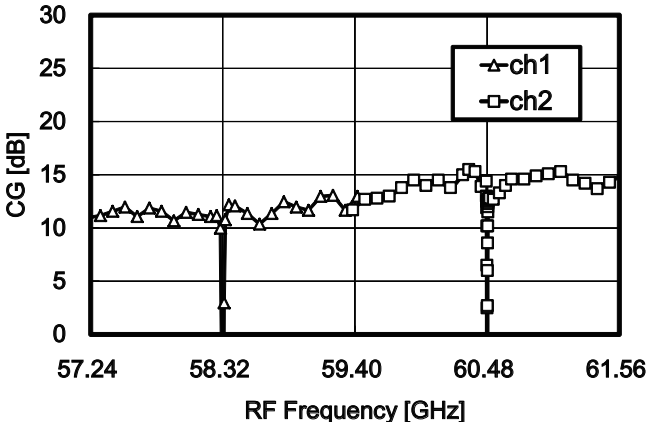


Fig. 8. Conversion gain of TX.

Table I shows the measured constellation. The symbol rate is 1.76 GS/s with a roll-off factor of 25 %, and the data rates with the 2.16 GHz bandwidth are 3.52 and 7.04 Gb/s for QPSK and 16QAM, respectively. The communication distances in QPSK and 16QAM modes are at least >100 cm

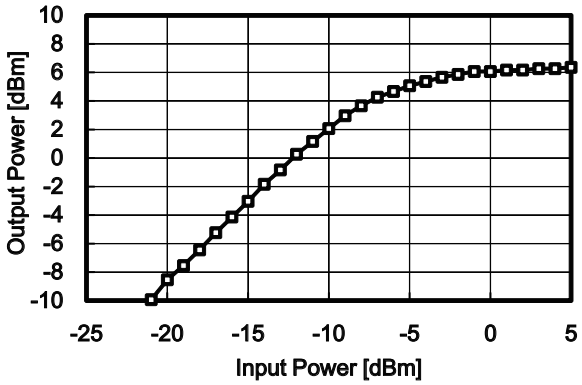


Fig. 9. Output power.

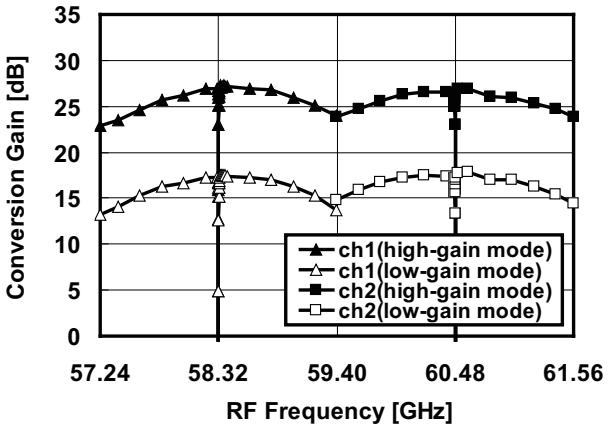


Fig. 10. Conversion gain of RX.

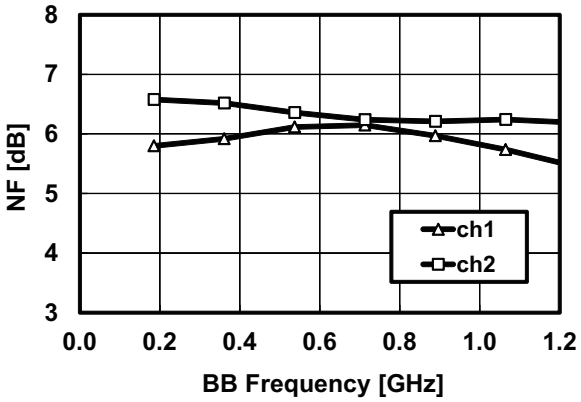
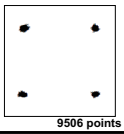
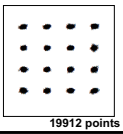
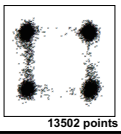
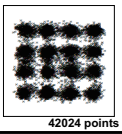


Fig. 11. Noise figure.

and >20 cm, respectively. The minimum BER in QPSK mode is also confirmed up to $<10^{-8}$ (limited by measurement time). Full-rate communication speed is possible for channel 1 (57.24 to 59.40 GHz) and channel 2 (59.40 to 61.56 GHz) of IEEE802.15.3c within a BER of $<10^{-3}$. The maximum data rates using wider bandwidth in QPSK and 16QAM with a 25 % roll-off are at least 10 Gb/s and 16 Gb/s within a BER of $<10^{-3}$. BPSK and 8PSK can also be realized with the full data rates.

TABLE I

MEASURED CONSTELLATION FOR QPSK AND 16QAM.

Constellation	 9506 points	 19912 points	 13502 points	 42024 points
Modulation	QPSK	16QAM	QPSK	16QAM
Symbol rate	1.76GS/s	1.76GS/s	5.0GS/s	4.0GS/s
Data rate	3.52Gb/s	7.04Gb/s	10.0Gb/s	16.0Gb/s
EVM (withDFE)	-30.5dB	-28.2dB	-15.2dB	-16.1dB

VI. CONCLUSION

This paper presents a 60 GHz direct-conversion transceiver using the capacitive cross-coupling neutralization in 65 nm CMOS. A fully-balanced mixer is used to reduce the local leakage, and the matching blocks of differential amplifiers realize the common-mode rejection. The proposed transceiver realizes the 60 GHz wireless communication for 16QAM/8PSK/QPSK/BPSK mode, which is capable of channel 1 and channel 2 operation for the IEEE 802.15.3c standard. The maximum data rate is at least 10 Gb/s in QPSK mode and 16 Gb/s in 16QAM mode within a BER of $<10^{-3}$, and the transmitter and the receiver consume 181 mW and 138 mW, respectively.

ACKNOWLEDGMENT

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TABLE III

PERFORMANCE SUMMARY.

Tx	
CG	16 dB
P_{1dB}	5.4 dBm
P_{sat}	6.5 dBm
P_{DC}	181 mW

Rx	
CG	17-27 dB
NF	$<$ 6.1 dB
IIP3	-20 dBm
P_{DC}	138 mW

PLL	
Frequency	17.9-21.2 GHz
Phase Noise @60.48GHz	-94.2 dBc/Hz @1MHz-offset
P_{out}	-2 dBm
P_{DC}	66 mW

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TABLE II

PERFORMANCE COMPARISON.

	Data rate/Modulation	EVM(16QAM)	Direct-Conversion	Integration	Power	Area
[1]U. Toronto	4 Gb/s(BPSK)	N/A	Yes	65 nm, single-chip TRx w/o LO	374 mW with 1.2 V (233 mW with 1.0 V)	1 mm^2
[2]UCB	4 Gb/s(QPSK)	N/A	Yes	90 nm, single-chip TRx inc. 30GHz PLL with 90° hybrid and BB	170 mW(Tx mode) 138 mW(Rx mode)	6.8 mm^2
[7]Tokyo Tech	8 Gb/s(QPSK) 11 Gb/s(16QAM)	-17 dB (Tx→Rx)	Yes	65 nm, single-chip TRx with 60 GHz quad. osc.	186 mW(Tx mode) 106 mW(Rx mode)	7.3 mm^2(TRx) 1.2 mm^2(PLL)
[3]CEA-LETI	3.8 Gb/s(16QAM)	-20.7 dB (Tx) -19.2 dB (Rx)	No	65 nm, single-chip TRx with a HTCC package	1.357 W(Tx mode) 454 mW(Rx mode)	9.3 mm^2(TRx) 0.46 mm^2(PLL)
[4]SiBeam	7.14 Gb/s(16QAM) 3.8 Gb/s(16QAM)	-19.2 dB (Tx→Rx)	No	65 nm, Tx/Rx with BB, maximum 32 sink/source phased-arrays	1.82 W(Tx mode) 1.25 W(Rx mode)	77.2 mm^2(Tx) 72.7 mm^2(Rx)
This work	**10 Gb/s(QPSK) 16 Gb/s(16QAM)**	**-28.2 dB (Tx→Rx)**	Yes	65 nm, single-chip, capacitive cross-coupled TRx with 60 GHz quad. osc.	**181 mW(Tx mode) 138 mW(Rx mode)**	**4.8 mm^2(TRx) 1.2 mm^2(PLL)**