A 20GHz ILFD with Locking Range of 31% for Divide-by-4 and 15% for Divide-by-8 Using Progressive Mixing

Ahmed Musa, Kenichi Okada, Akira Matsuzawa

Tokyo Institute of Technology, Japan

TOKYO TECH Pursuing Excellence

Matsuzawa & Okada Lab.

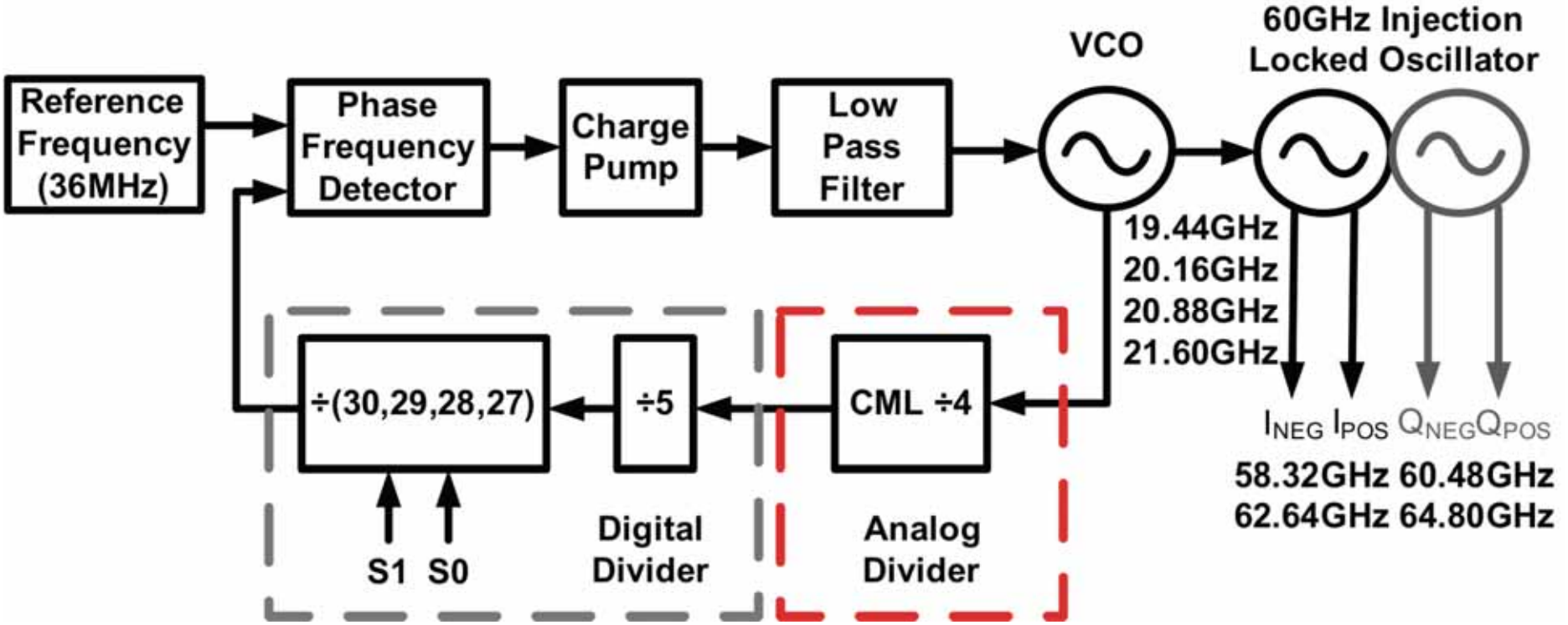
Outline

- Motivation
- Conventional ILFD
- Proposed ILFD
- Measurement Results
- Performance Comparison
- Conclusion

Outline

- **Motivation**
- Conventional ILFD
- Proposed ILFD
- Measurement Results
- Performance Comparison
- Conclusion

High Frequency PLLs



- **High Frequency PLLs are becoming more popular**
- **Static prescalers consume considerable power**
  - **40% of PLL total power consumption [1].**

[1] A. Musa et. al, JSSC 2011

High Speed Frequency Dividers

- **Static Frequency Dividers:**
  - **Operate up to several tens of GHz**
  - **Wide locking range**
  - **Consume considerable current to operate**
  - **Conventionally only divides by 2**

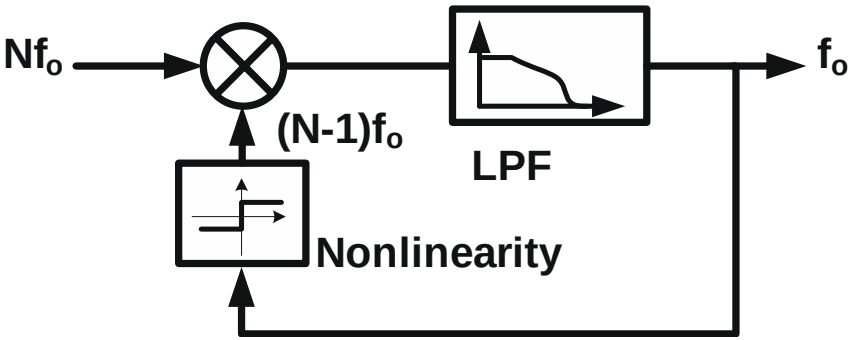
- **Injection Locked Frequency Dividers (ILFDs)**
  - **Operate higher than 100GHz**
  - **Limited locking range**
  - **Low power consumption**
  - **Can divide by higher than 2**

Outline

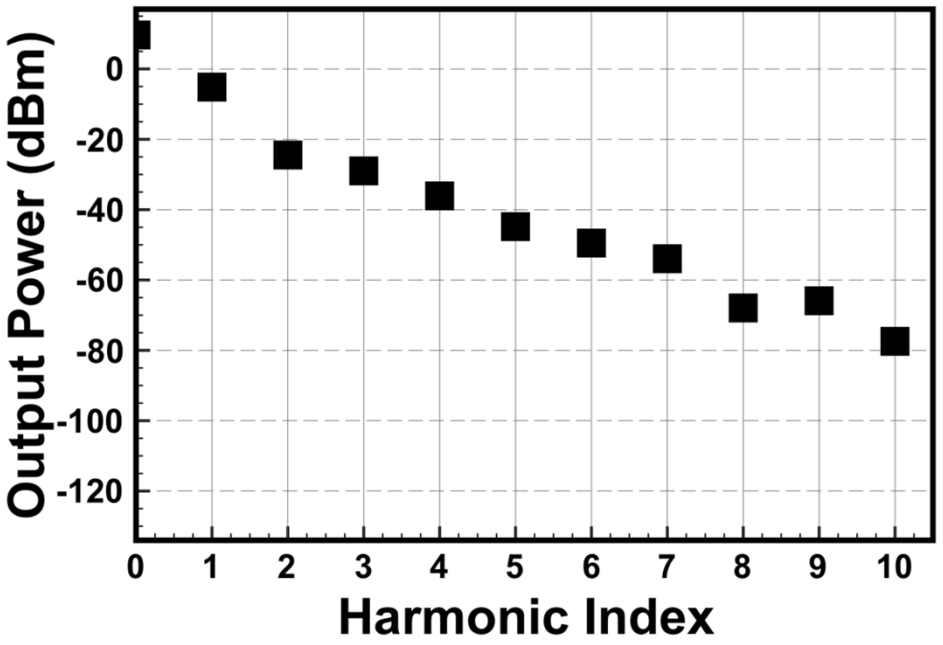
- Motivation
- **Conventional ILFD**
- Proposed ILFD
- Measurement Results
- Performance Comparison
- Conclusion

Conventional ILFD (Direct)

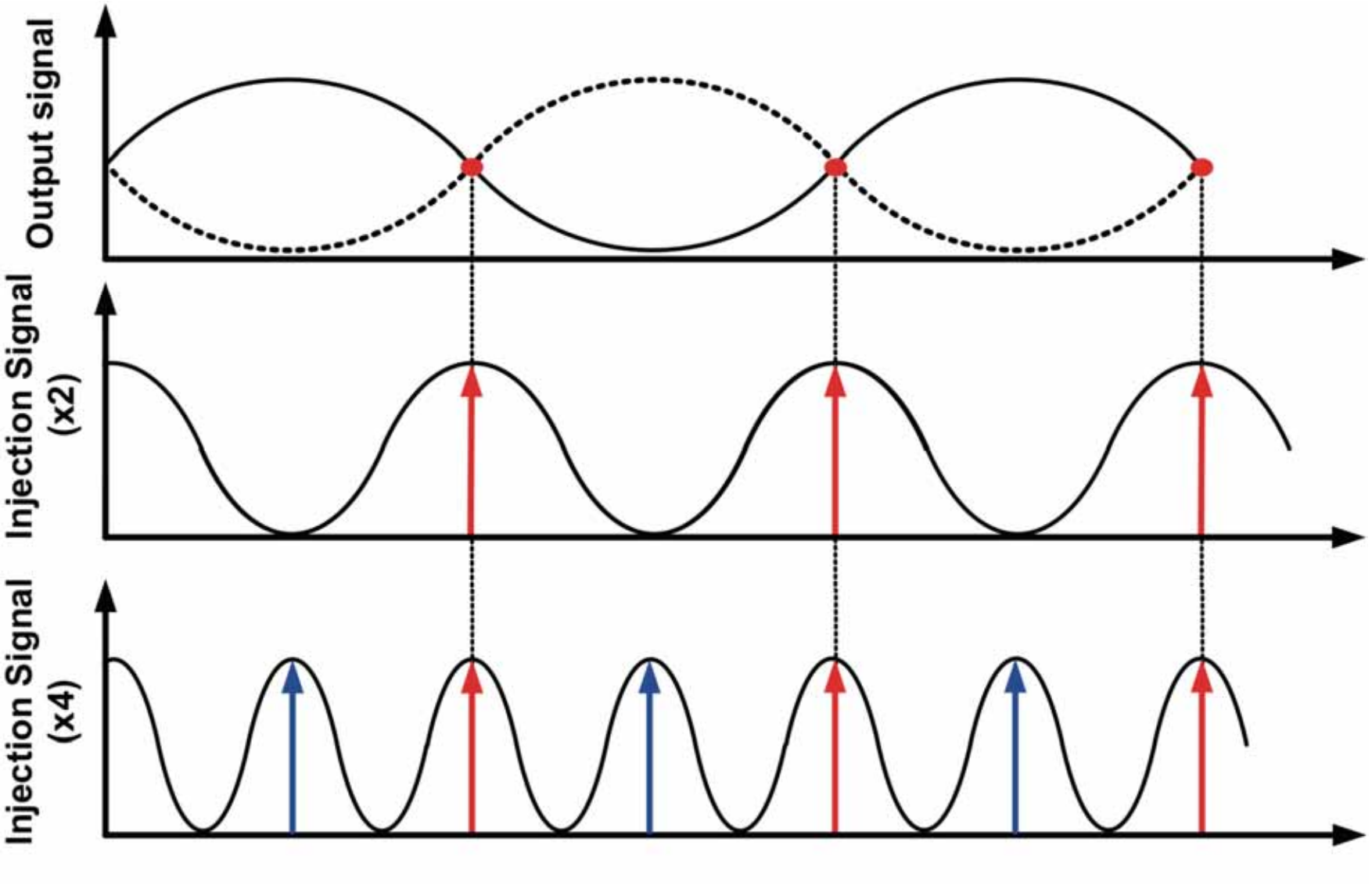
- **Input signal is divided directly by *N*:**
  - **Low power consumption**
  - **Narrow Locking range**
  - **False Locking**



Divide by *N* directly in one step



Conventional ILFD

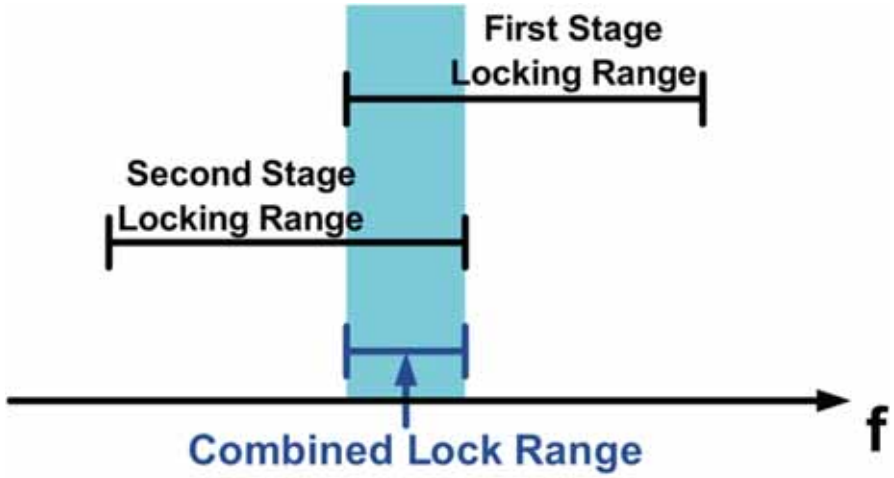


Red arrows indicate <u>desired</u> injection

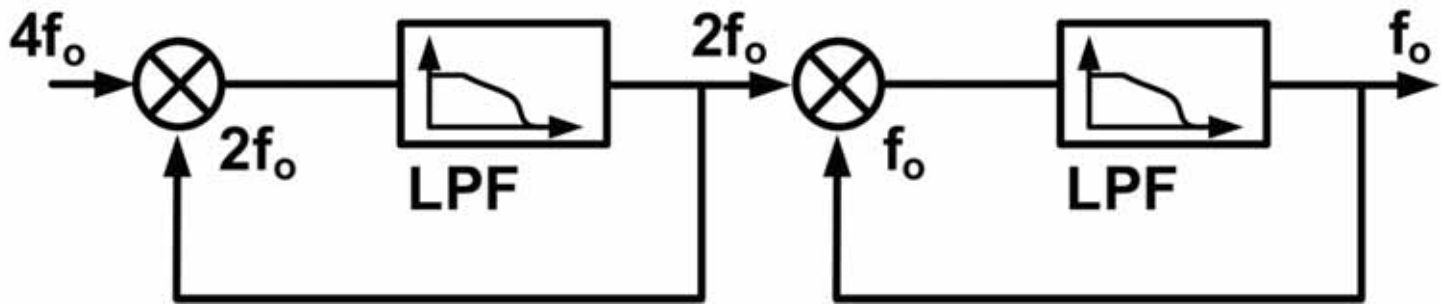
Blue arrows indicate <u>harmful</u> injection

Conventional ILFD (Cascade)

- **Cascading two ÷2 ILFDs to achieve ÷4:**
  - **Wider locking range**
  - **Locking range mismatch**
    - **15%@÷2 → 2.4%@÷4 [2]**
  - **Independent tuning**



Lock range mismatch



Divide by 4 in multistep by cascading 2 divide-by-2 circuits

[2] P. Mayr et. al, ISSCC 2007

ILFD Topology Summary

	Direct	Cascade
Lock range higher than 2	Narrow	Wide
False locking	Yes	No
Locking range mismatch	No	Yes
Power consumption	Low	High

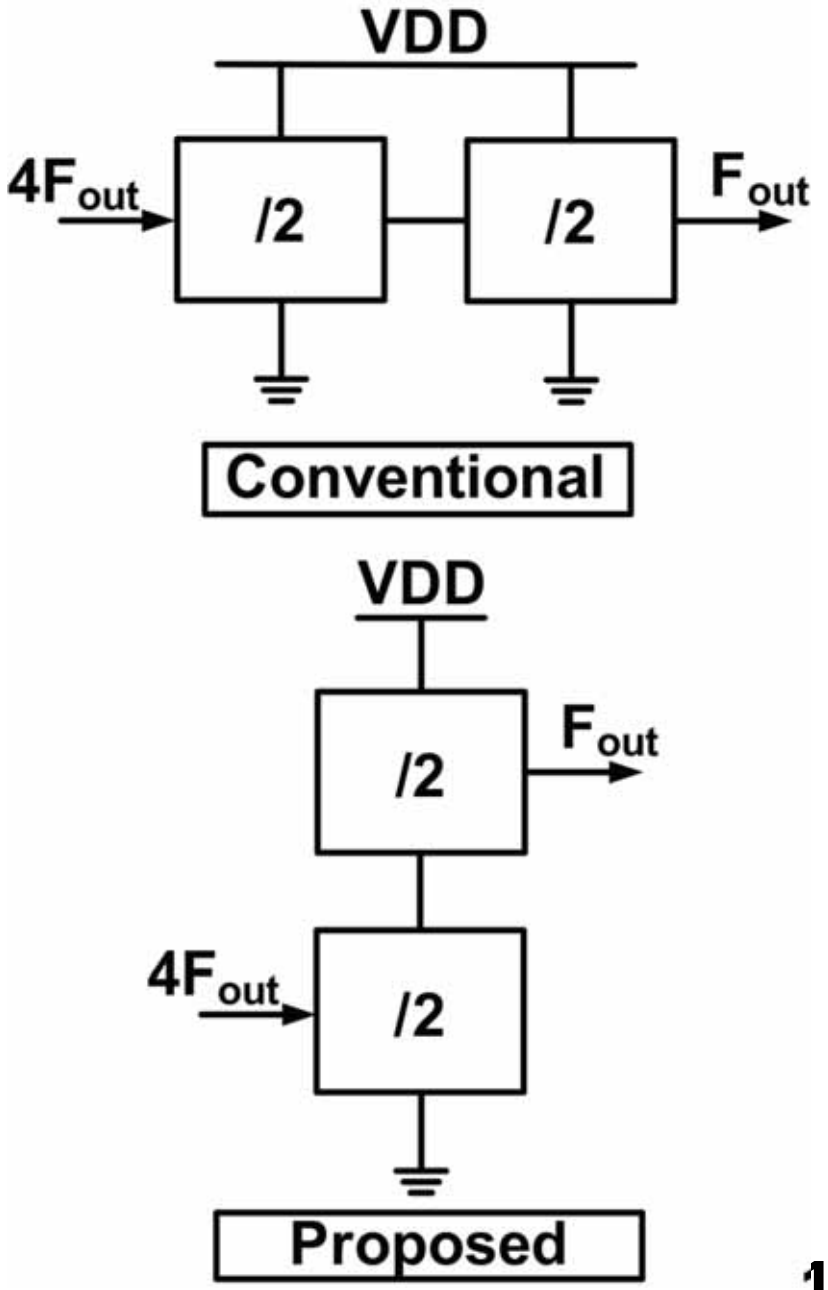
A topology that combines the advantages of both is needed

Outline

- Motivation
- Conventional ILFD
- **Proposed ILFD**
- Measurement Results
- Performance Comparison
- Conclusion

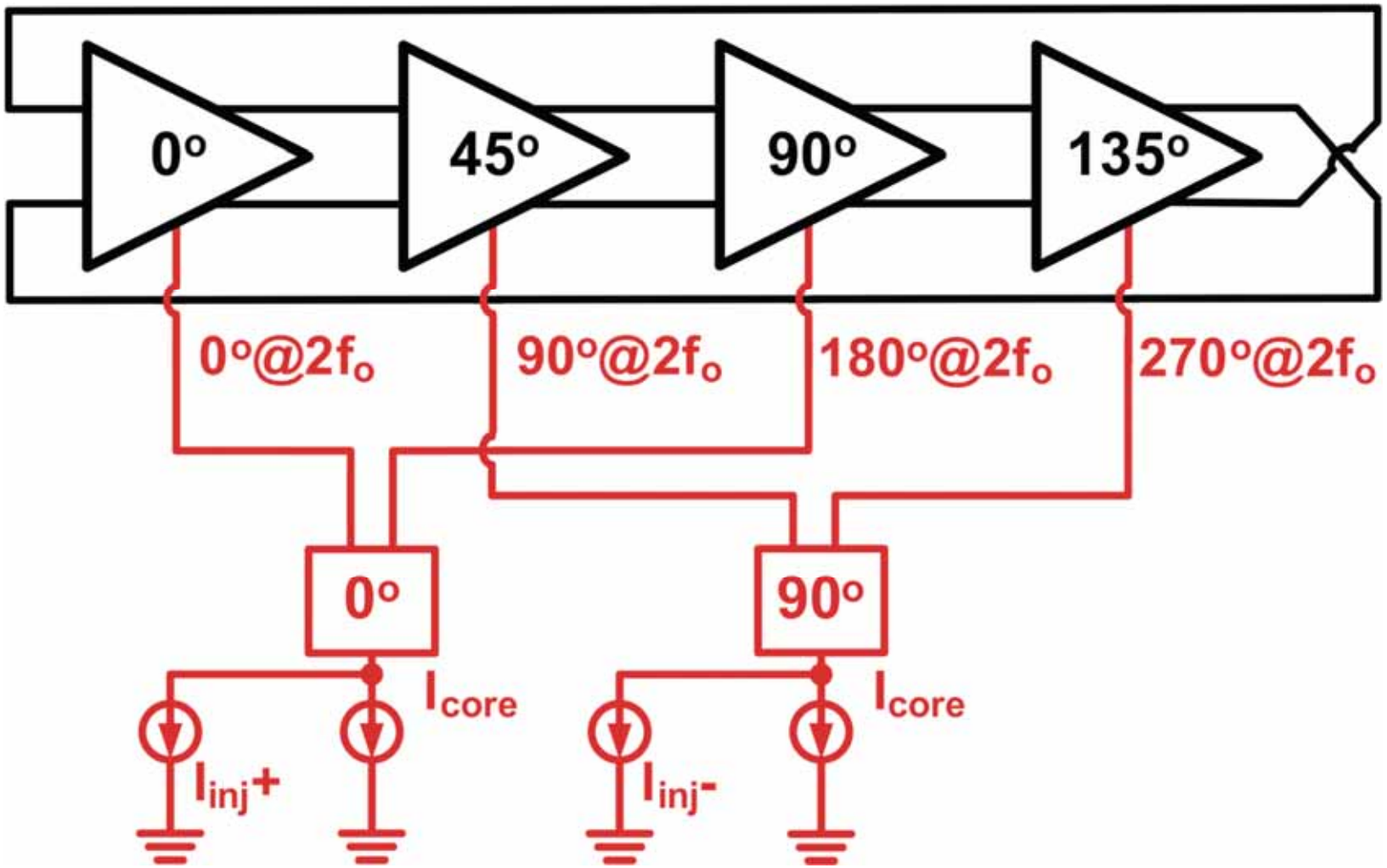
Proposed ILFD Configuration

- One oscillator
  - Direct division power consumption
- Reuse fundamental higher harmonics
  - Cascaded wider locking range
- Vertical configuration
- Extendable

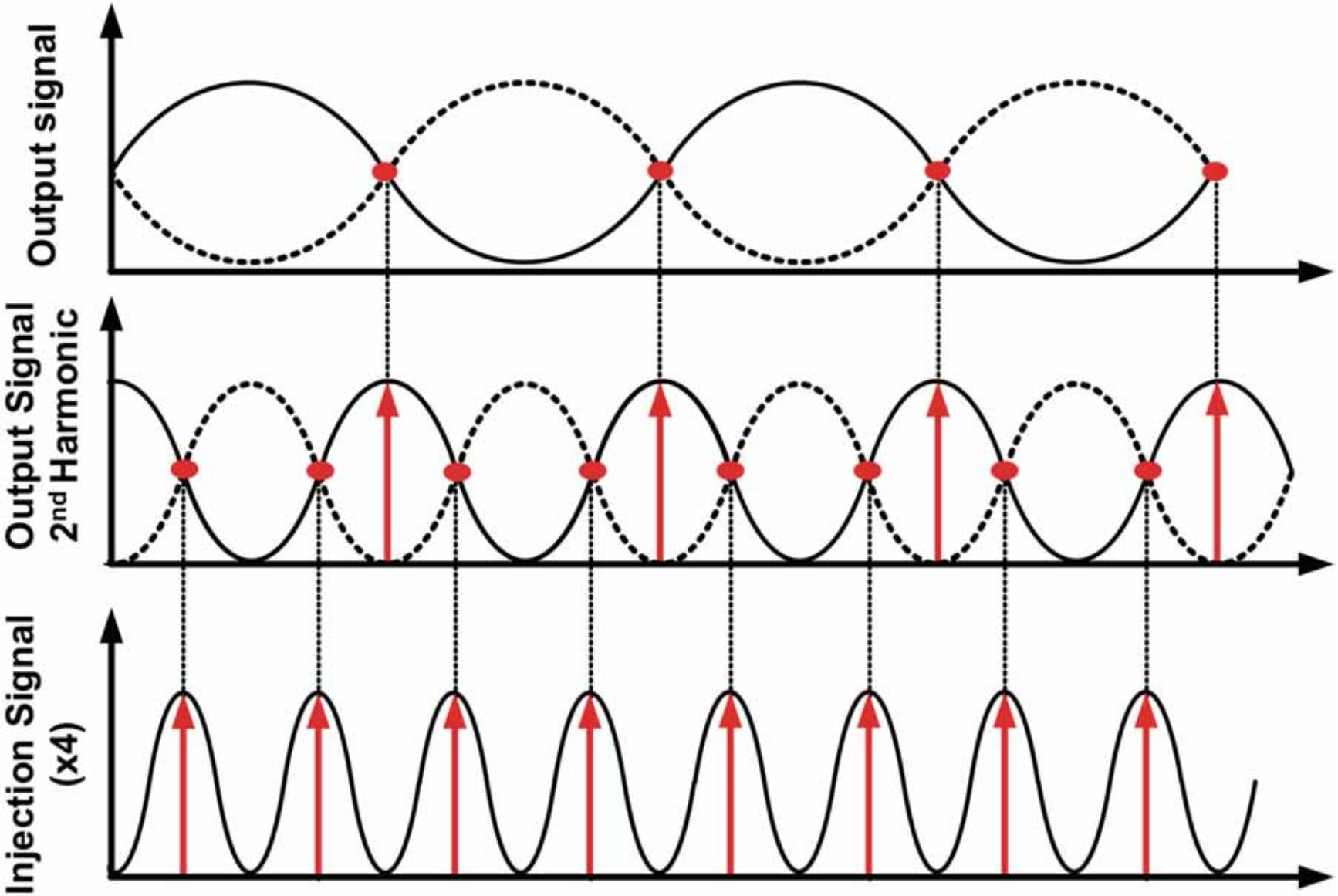


Proposed ILFD Configuration

- **For a divide-by-4 Configuration:**



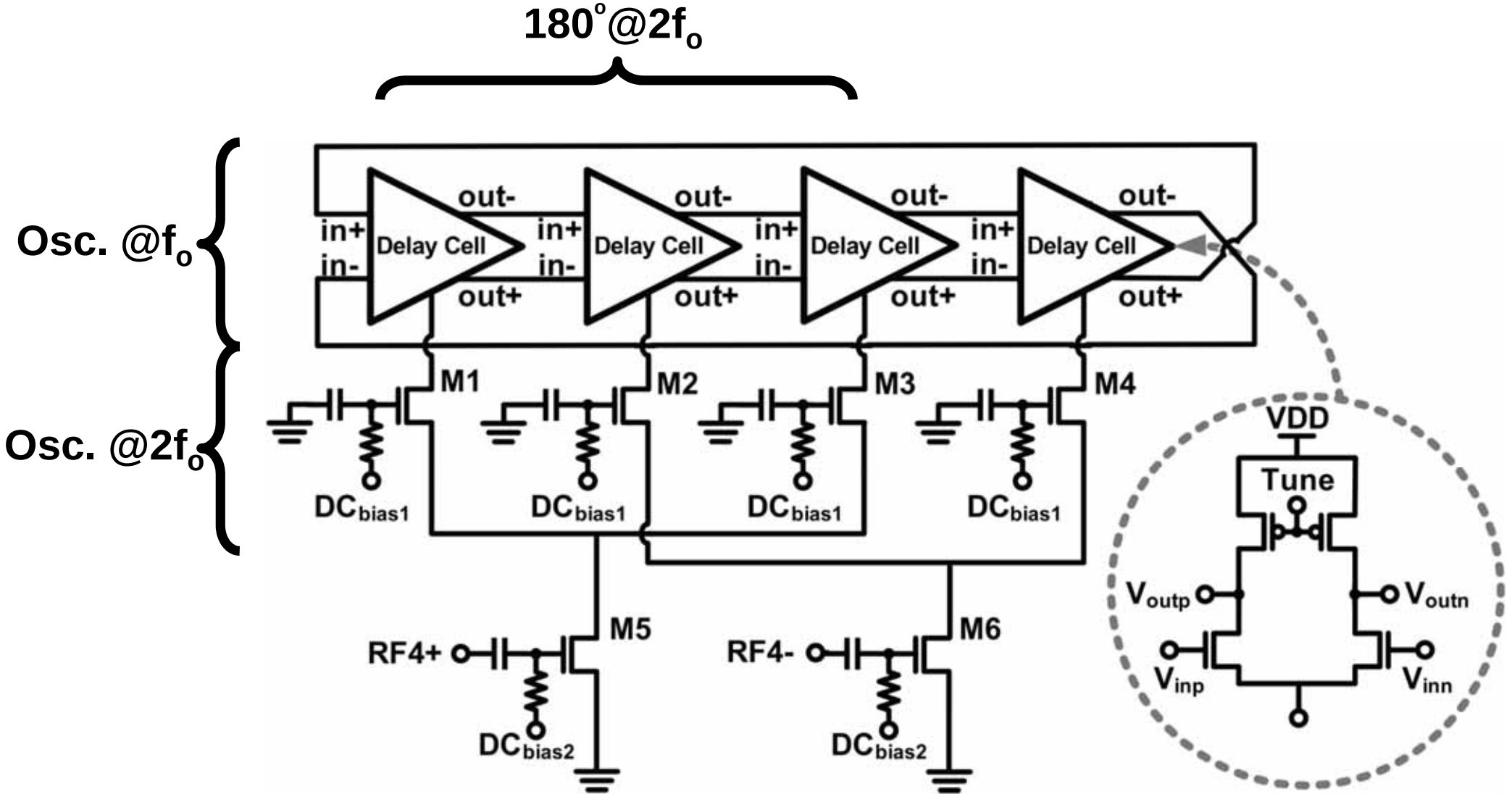
Proposed ÷4 ILFD Timing Waveform



Red arrows indicate <u>desired</u> injection

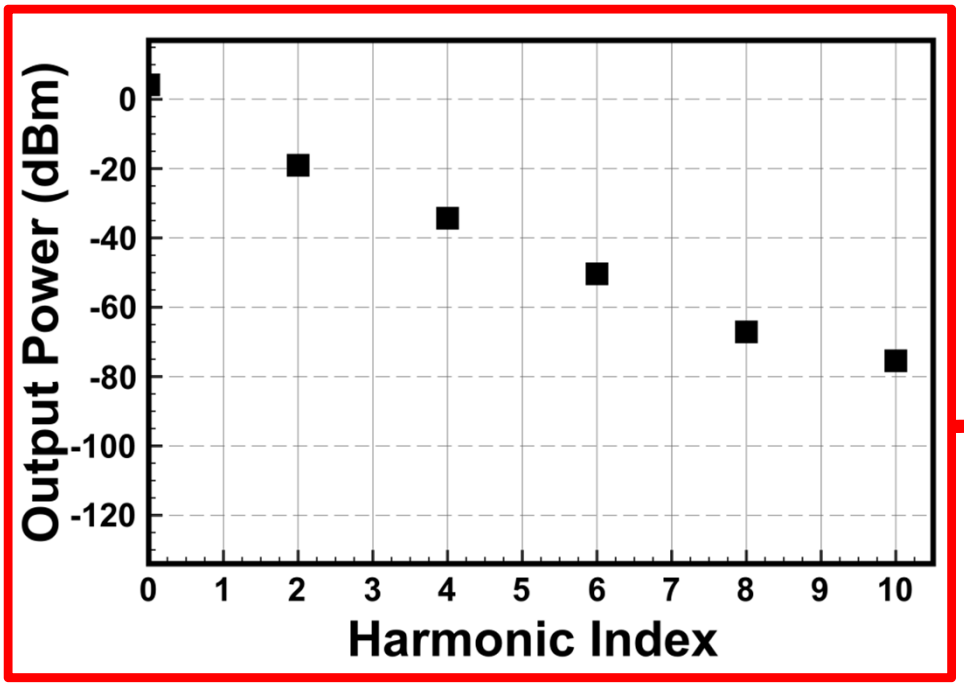
Blue arrows indicate <u>harmful</u> injection **(Not there anymore)**

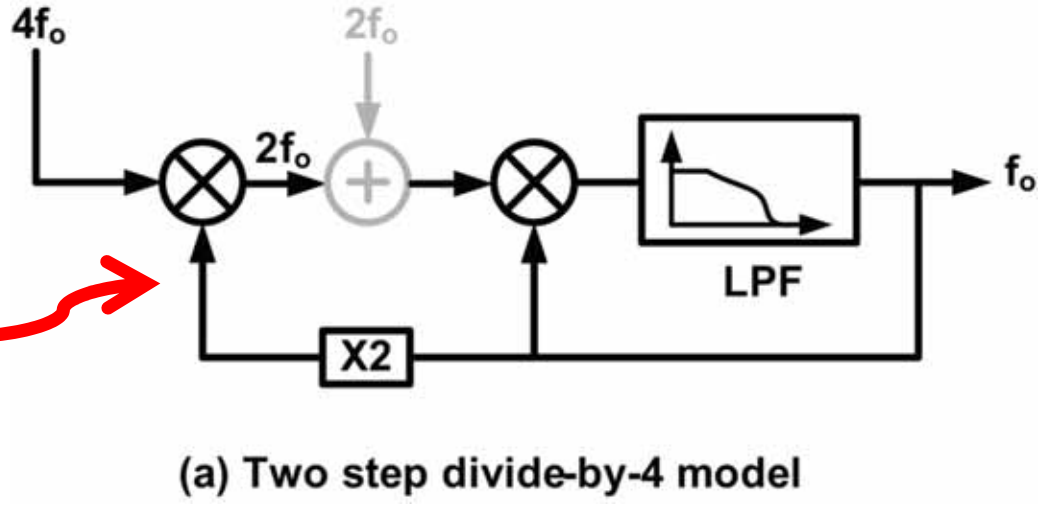
Proposed ÷4 ILFD Schematic



Schematic of the Proposed Progressive Mixing ILFD

Proposed ÷4 ILFD Model





(a) Two step divide-by-4 model

- Multistep conversion
- Strongest harmonics in mixing
- Intermediate points can be used to inject points for lower division ratios

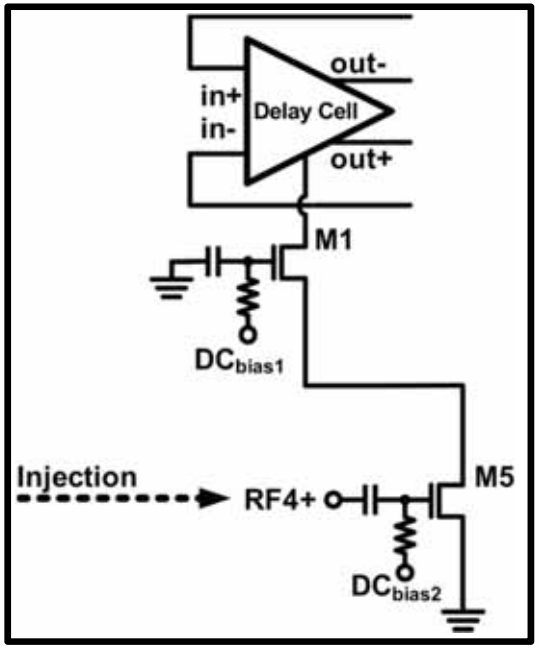
Proposed ILFD Topology Summary

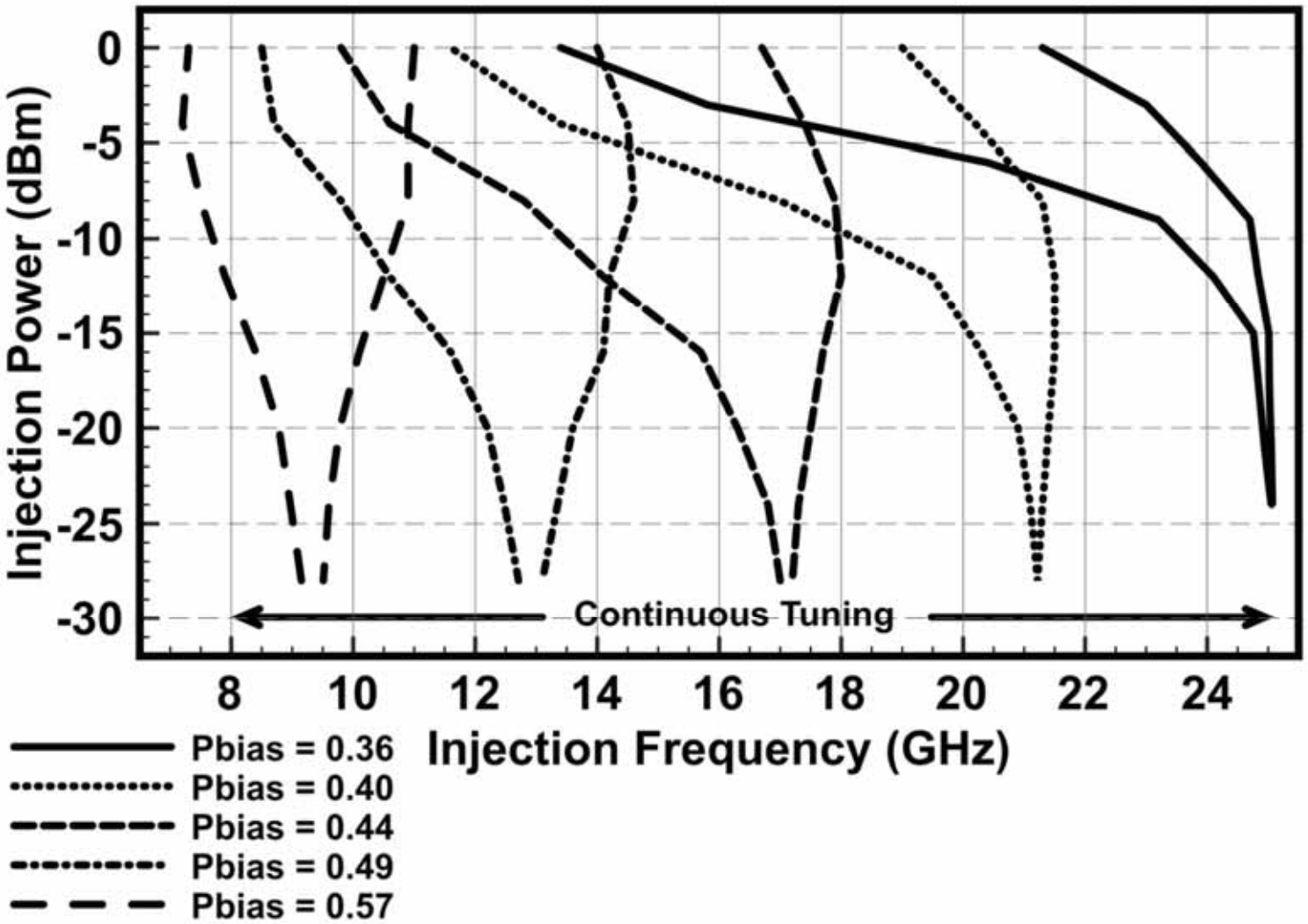
- **Inherent cascade topology for wide locking range.**
- **One oscillator is used for low power consumption.**
- **Strongest harmonic is used at each step to avoid false locking.**
- **Higher harmonics of the fundamental are used which avoids locking range mismatch.**

Outline

- Motivation
- Conventional ILFD
- Proposed ILFD
- **Measurement Results**
- Performance Comparison
- Conclusion

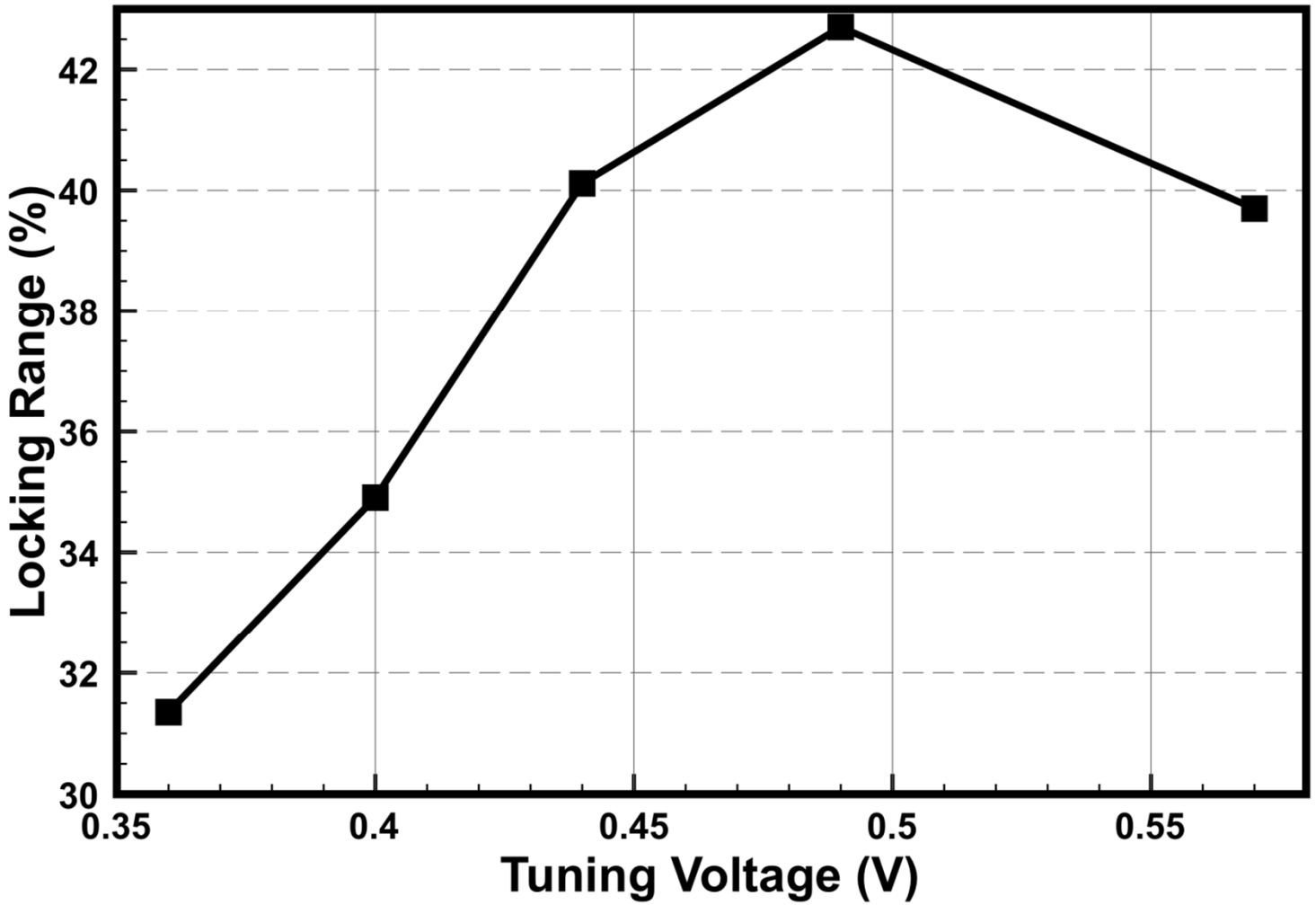
Sensitivity Curve ÷4 (Measured)





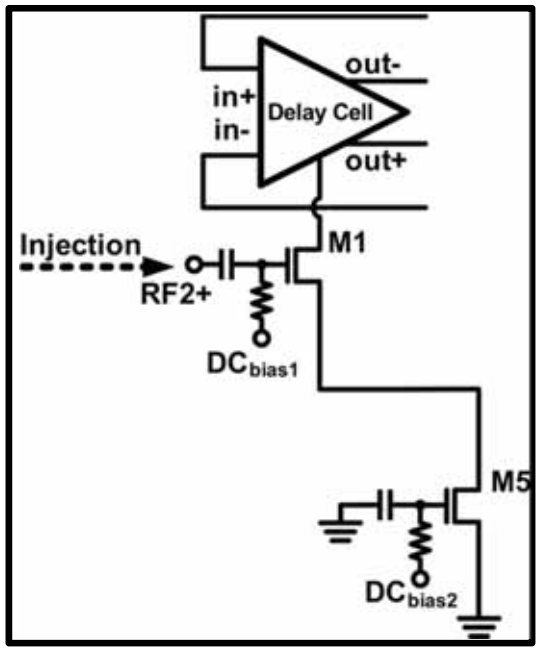
31.4% Locking range@20GHz

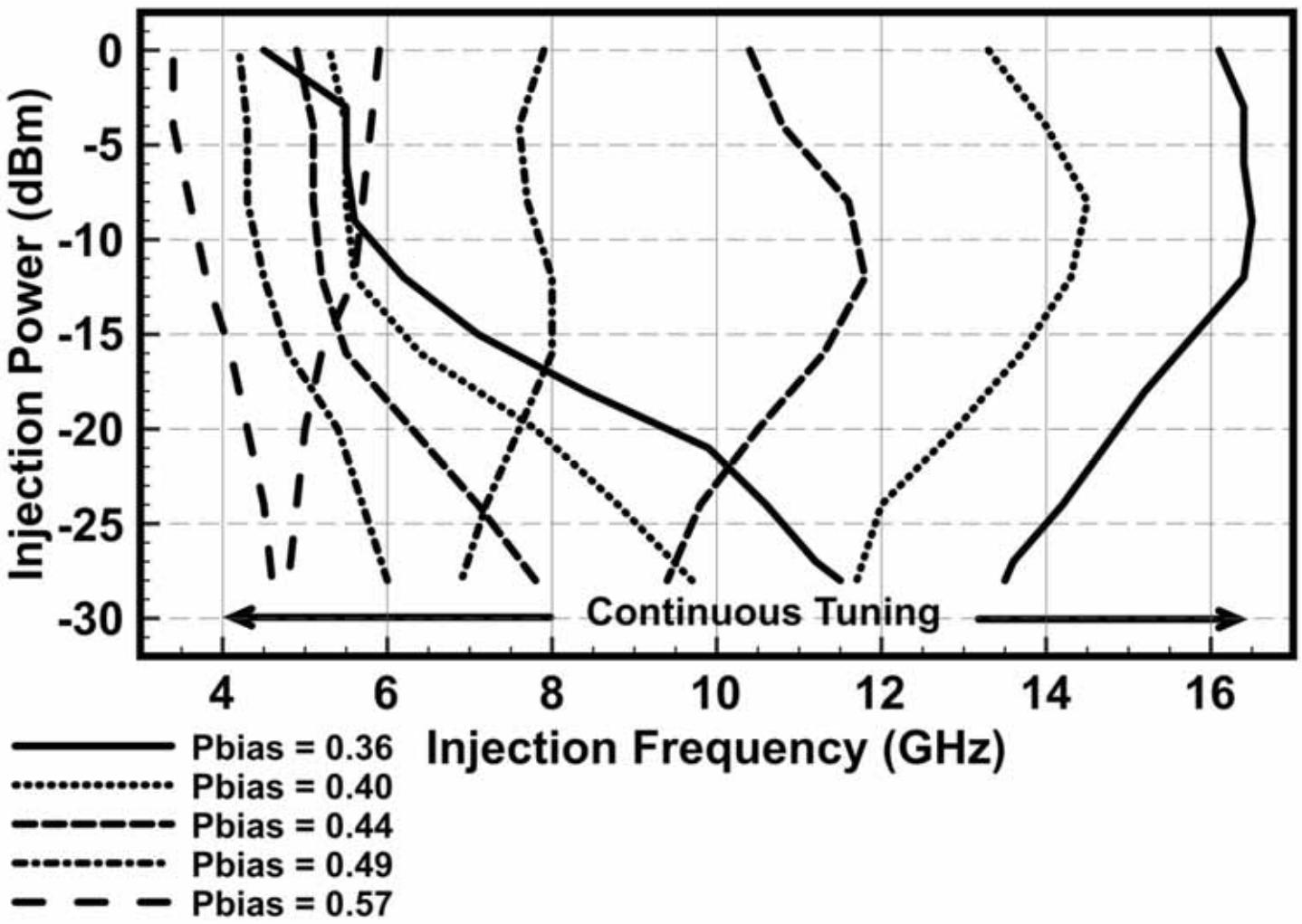
Locking Range Vs Tuning (Measured)



42.7% Maximum Locking Range

Sensitivity Curve ÷2 (Measured)



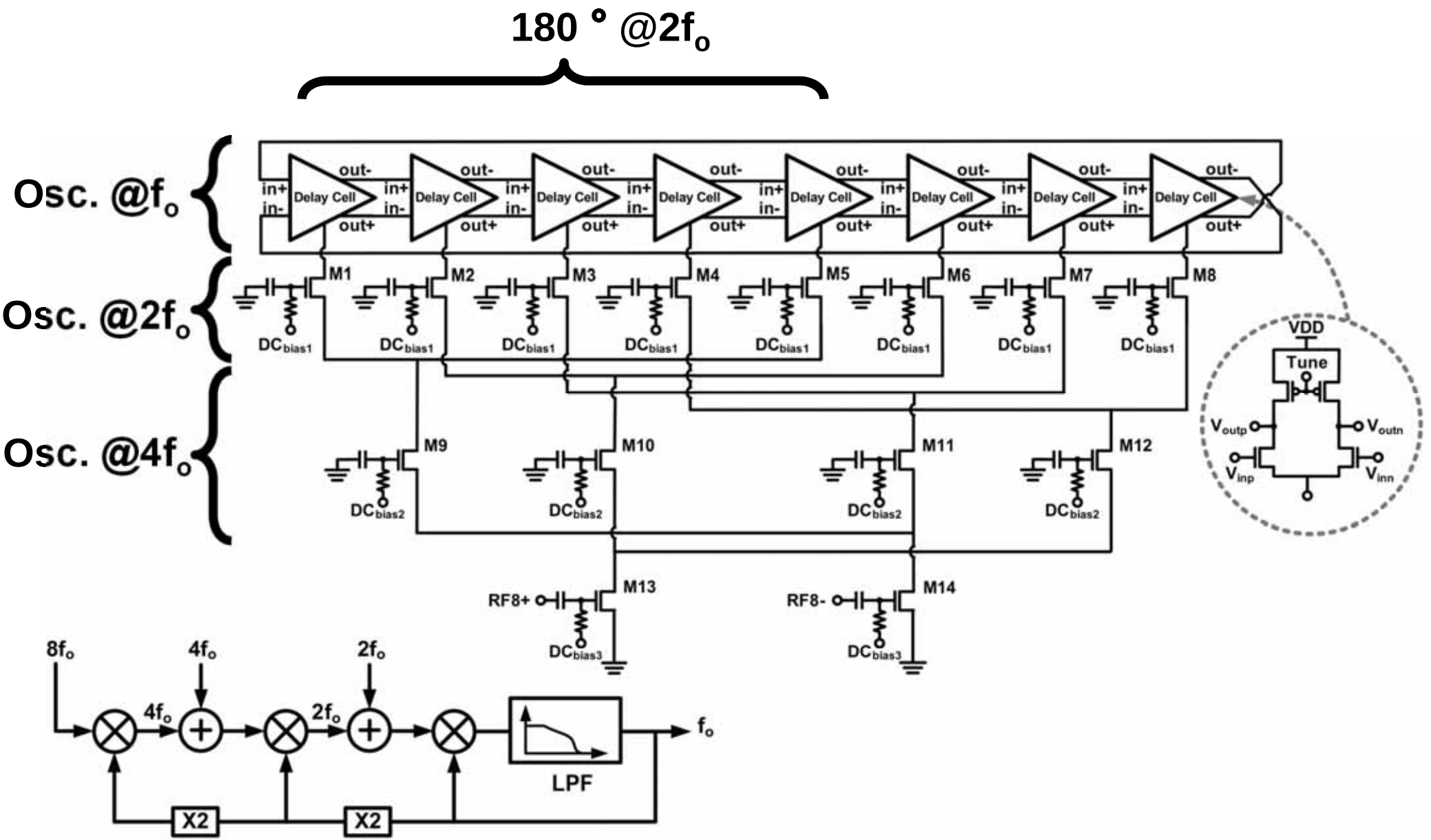


92.1% Maximum Locking range

Performance Summary ÷4

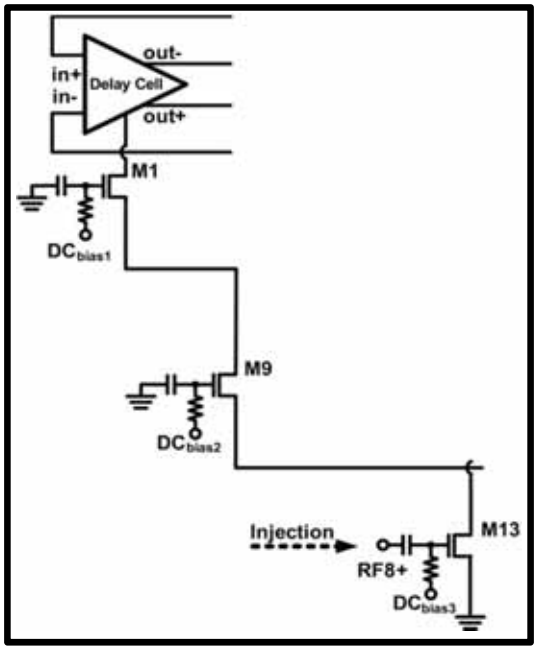
	Measurement
Process	65nm CMOS
Supply	1.2V
Free-run Frequency Range	2 ~ 8GHz
Lock range (÷4)	31.5 ~ 42.7%
Lock range (÷2)	53.7 ~ 92.6%
Power Consumption	3.9mW

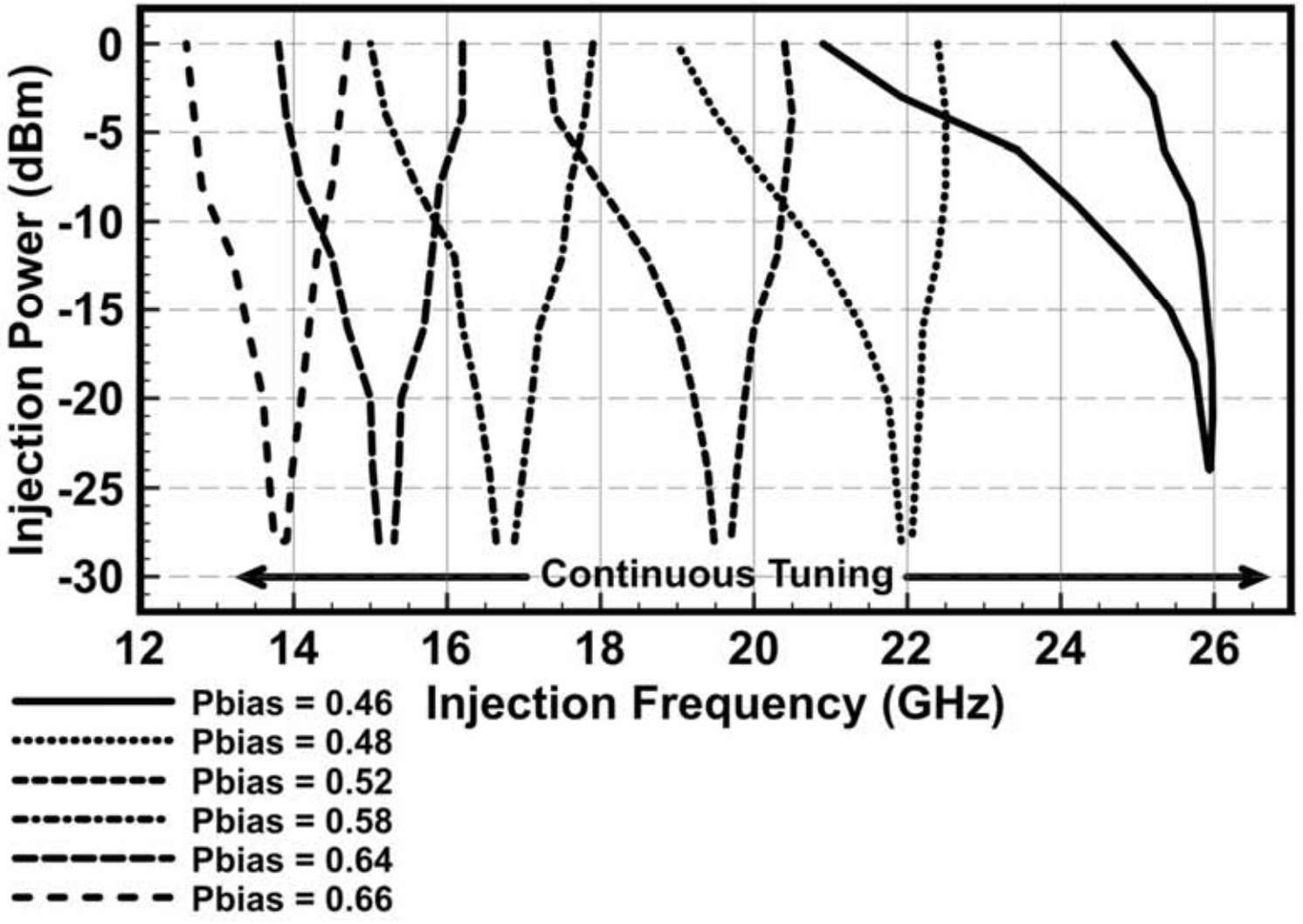
Proposed ÷8 ILFD



Three step divide-by-8 model

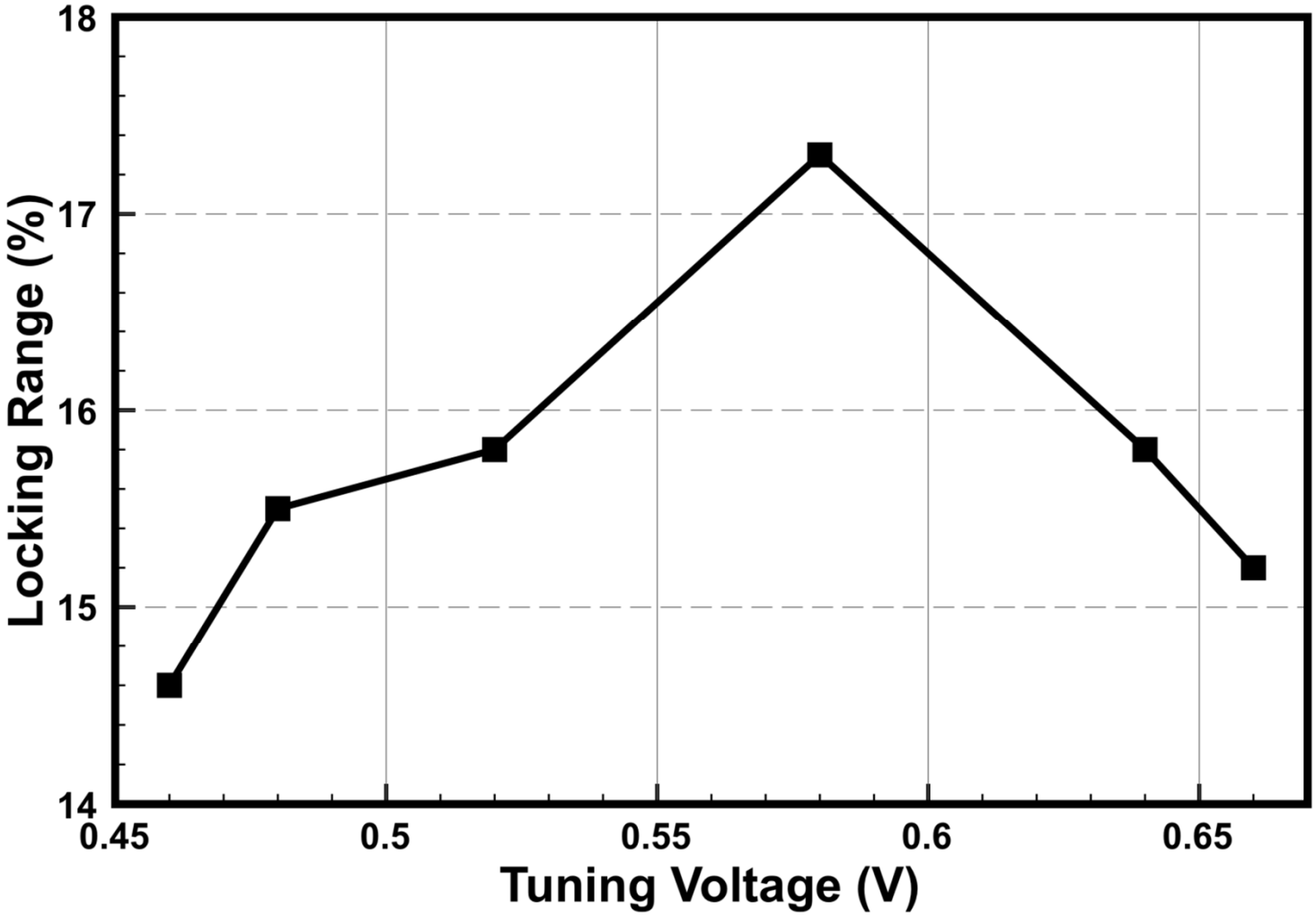
Sensitivity Curve ÷8 (Measured)





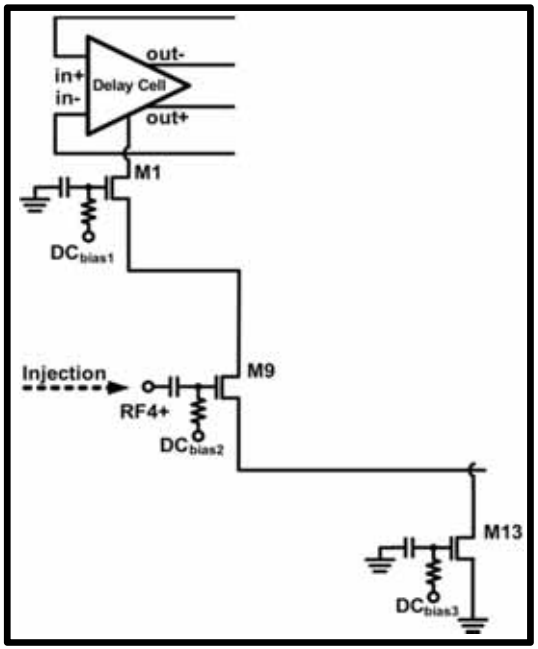
14.6% Locking range@20GHz

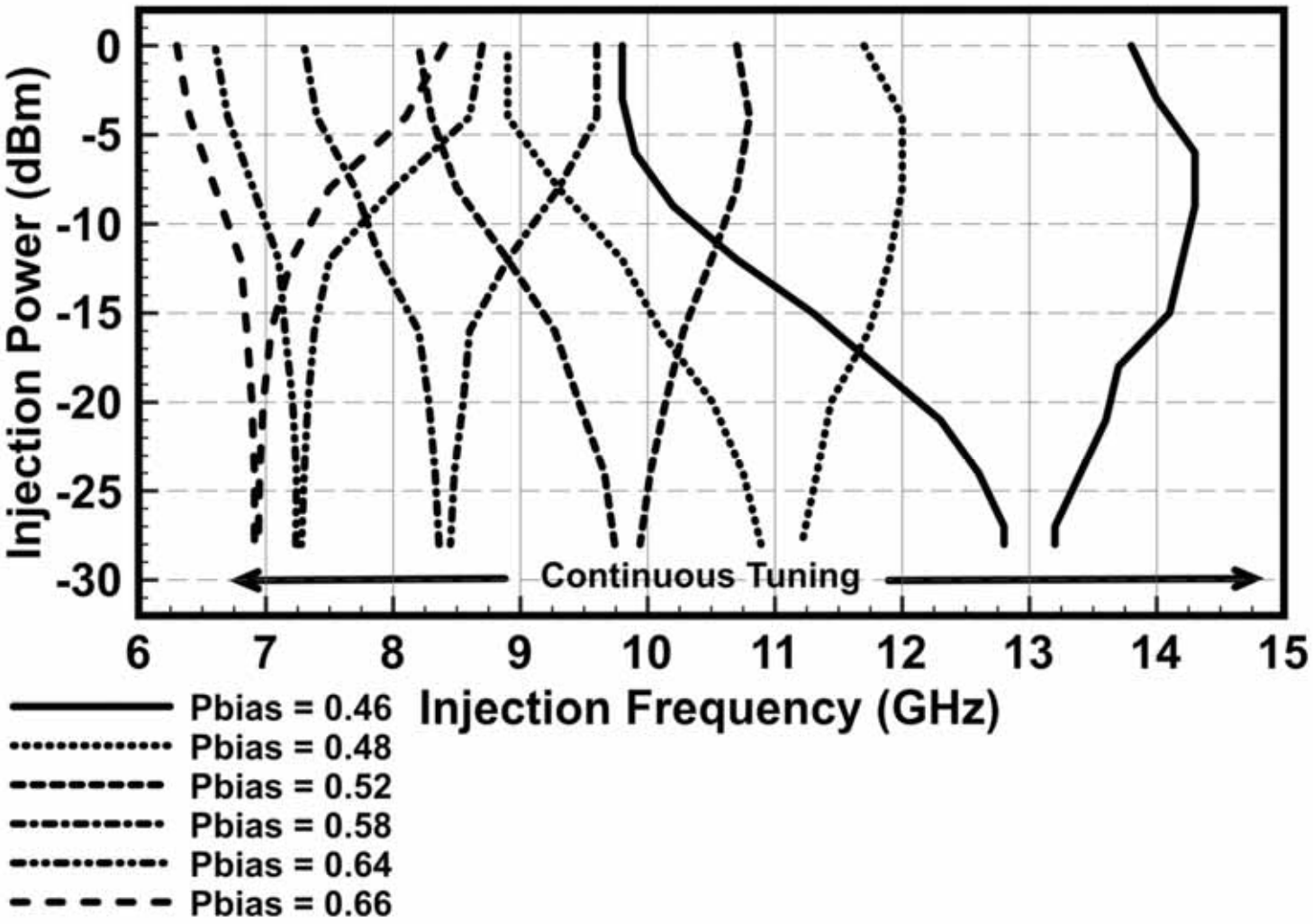
Locking Range Vs Tuning (Measured)



17.3% Maximum Locking Range

Sensitivity Curve ÷4 (Measured)





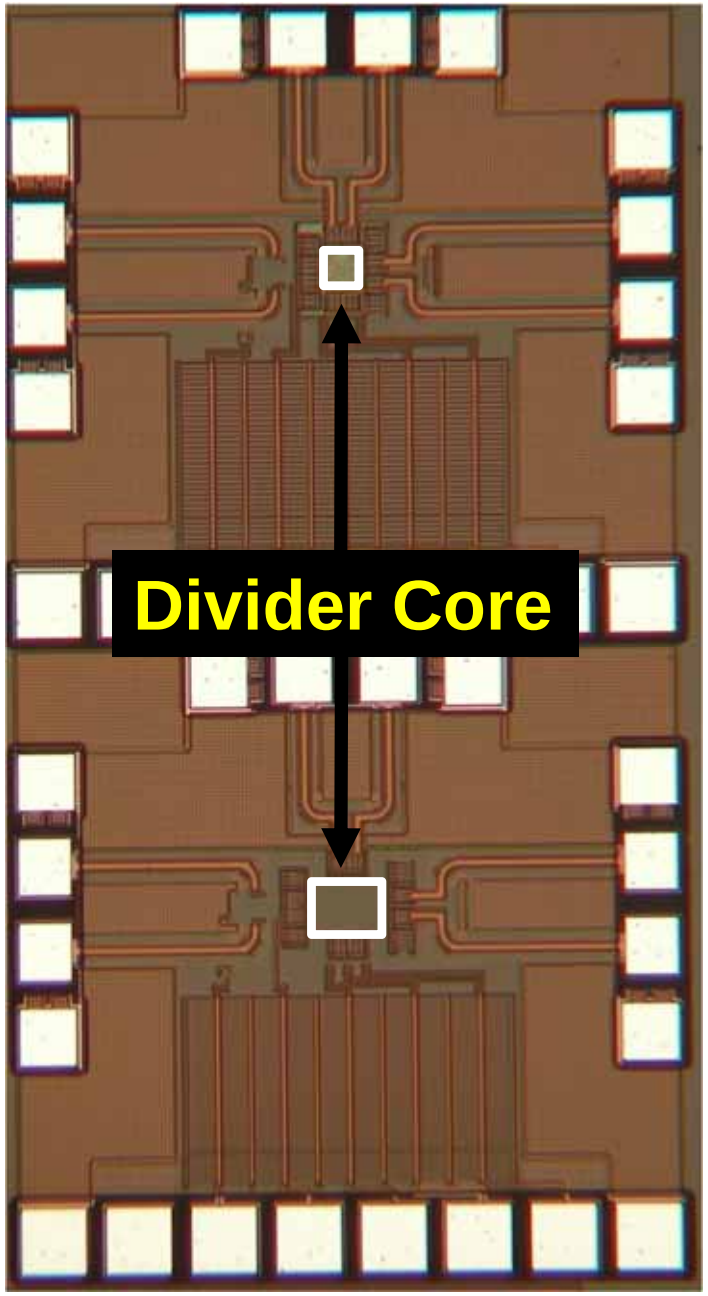
31.8% Maximum Locking range

Performance Summary ÷8

	Measurement
Process	65nm CMOS
Supply	1.2V
Free-run Frequency Range	1.6 ~ 5.3GHz
Lock range (÷8)	14.6 ~ 17.3%
Lock range (÷4)	25.5 ~ 31.8%
Power Consumption	7.1mW

Chip Micropraph

- **Chip Area:**
  - **÷4**
    - **750µm x 810µm**
    - **Divider**
      - **52µm X 48µm**
  - **÷8**
    - **750µm x 810µm**
    - **Divider**
      - **66µm x 86µm**



Outline

- Motivation
- Conventional ILFD
- Proposed ILFD
- Measurement Results
- **Performance Comparison**
- Conclusion

Performance Comparison

		TEG 1	TEG 2	[3]	[2]	[5]	[6]
Division Ratio(s)		2, 4	4, 8	2, 4	2, 4	4	2, 4, 6, 8
Power (mW)		3.9	7.1	3.0	12.4	2.8	6.8
Lock Range (GHz)	/2	11.6 (92%)	-	23 (34%)	12.1 (15%)	-	2 (56%)
	/4	7.9 (31%)	4 (32%)	6.5 (7.3%)	1.9 (2.4%)	1.6 (2.3%)	1.6 (22%)
	/8	-	3.8 (15%)	-	-	-	0.25 (1.7%)

[3] C.C. Chen et. al, MTT 2009

[2] P. Mayr et. al, ISSCC 2007

[5] K. Yamamoto et. al, ISSCC 2006

[6] M. Acar et. al, RFIC 2004

Outline

- Motivation
- Conventional ILFD
- Proposed ILFD
- Measurement Results
- Performance Comparison
- **Conclusion**

Conclusion

- A new injection locked frequency divider (ILFD) is proposed.
- The divider uses progressive mixing (multistep mixing) to allow injection at higher harmonics of the fundamental.
- Uses separate inputs for different division ratios to avoid false locking
- The widest locking range has been achieved especially for higher division ratios.
  - ÷2 (93%)
  - ÷4 (43%)
  - ÷8 (17%)