An Ultra-Low-Voltage LC-VCO with a Frequency Extension Circuit for Future 0.5-V Clock Generation

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Abstract - This paper proposes a 0.5-V LC-VCO with a frequency extension circuit to replace ring oscillators for ultra-low-voltage sub-1ps-jitter clock generation. Significant performances, in terms of 0.6-ps jitter, 50MHz-to-6.4GHz frequency tuning range with 2 bands and sub-1mW P_{DC}, indicates the successful replacement of ring VCO for the future 0.5-V LSIs and power aware LSIs.

I Introduction

Conventionally, ring oscillators are wide used due to small area, less power consumption and reasonable jitter, compared with LC-VCO. However, as the scaling-down of CMOS technology continues, the maximum power supply voltages have been steadily decreasing [1]. Thus, as illustrated in table 1, ring VCOs become infeasible due to too large jitter and unbelievable power consumption, which highlights the necessity of adopting LC-VCOs for ultra-low-voltage sub-picosecond-jitter clock generation applications [2].

Recently, active researches have been contributed to implement ultra-low-voltage LC-based VCOs [5][6][7][8]. Although these publications successfully achieve low power consumption and low jitter, however, they still suffer from narrow frequency tuning range which makes them infeasible for adoption in practical clock generation circuits [3], where wide frequency tuning range is strongly required to deal with different computing complexity applications and compensate the fluctuation in supply voltage, temperature and process (PVT). In this paper, a 0.5-V LC-VCO with a frequency extension circuit is proposed to overcome the issues.

II. Analysis and design of VCO architecture

As shown in Fig.1, the proposed circuit consists of a core VCO, divider stage 1 and stage 2. The fundamental frequency f_0 is output of core VCO. 1/2 f_0 and 1/3 f_0 are generated by the switchable divider stage 1. Lower frequency range can be produced by the divider stage 2. More specifically, the core VCO can be tune from 4.1-to-6.4GHz, the continuous tuning range of 2.05-to-3.2GHz and 1.36-to-2.13GHz can be generated with the divider-by-2 and divider-by-3, respectively. Lower frequency range from several MHz to 1.6-GHz can be obtained by divider stage 2. As a result, the LC-VCO with frequency extension circuit generates two bands distributed from 0.05-to-3.2GHz (band I) and 4.1-to-6.4GHz (band II).

A. 0.5-V divider stage design

Three strict requirements for divider stage 1 make it extremely difficult to design such kind of divider:
1.) Operate under the power supply as low as 0.5-V. 2.) Operate at the output frequency of core VCO (higher than 7GHz). 3.) Possess wide operation frequency range as wide as the tuning range of core-VCO (more than 3GHz).

This paper proposes E-TSPC frequency dividers [4] using forward body bias technique for 0.5-V divider stage design. The main consideration is conventional frequency dividers (CML dividers, injection lock dividers) could not fulfill the requirements for divider stage 1. By applying forward body bias, the maximum operating frequency and minimum supply voltage for E-TSPC divider could be significantly improved. The schematic of the divider stage 1 and divider stage 2 based on E-TSPC logic are shown in Fig.2 and Fig.3

B. 0.5-V Core-VCO design

There are three main design issues for core-VCO design. First of all, forward body bias technique is employed to decrease the threshold voltage for transistors of core-VCO and switch transistors of capacitor bank. For transistors in the core-VCO, the decreasing of threshold voltage directly leads to the increasing of transconductance of the cross-coupled transistors. Then, the startup constraint at 0.5-V could be fulfilled. For switch transistors of capacitor bank, the decreasing of threshold voltage brings the increasing of Vgs. Thus, the turn-on resistance would be reduced, which in turn, decrease the parasitic capacitance and enlarge the frequency tuning range. The second consideration is gate-bias technique. As depicted in Fig.4, gate bias voltage V_{b1} and V_{b2} are added to gate nodes to guarantee the transistors operated at moderate or strong inversion region. Finally, tail-feedback technique [10][11] is applied to the core-VCO to improve the phase noise with the reduction of 1/f noise.

III. Measurement results

Fig.5 shows the chip microphoto of proposed design. Phase noise characteristics for each divide ratio of stage 1 are illustrated in Fig.6. Table II summarizes the performances comparison to other ultra-low-voltage VCOs in literature. FOM_T [12] is defined by the following equation.

$$\mathrm{FOM_T} = \mathrm{L}(f_{\mathrm{offset}}) - 20\log\left(\frac{f_0}{f_{\mathrm{offset}}}\cdot\frac{\mathrm{FTR}}{10}\right) + 10\log\left(\frac{\mathrm{P_{DC}}}{1\mathrm{mW}}\right) \qquad (1)$$

Fig.7 compares FOM_T and frequency tuning range of published ultra-low-voltage LC-VCOs [5][6][7][8][9]. To the best knowledge, this design has achieved the first wide tuning range in ultra-low-voltage VCOs.

IV. Conclusion

As addressed in this paper, the inevitable necessity of LC VCOs to replace ring VCOs for sub-picosecond-jitter clock generation is investigated [13]. With careful design, the proposed ultra-low-voltage frequency-extended LC-VCO can be well suited for sub-picosecond-jitter clock generation circuits in future 0.5-V LSI and power aware LSI.

ACKNOWLEDGEMENT

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TABLE I Scaling of jitter between LC and ring VCO

V_{DD}	Type	P_{DC}	Phase Noise @ 1MHz	Jitter
1.2V	LC	1mW	-121.6 dBc/Hz	0.16ps
	Ring	1mW	-91.6 dBc/Hz	5.0ps
0.5V	LC	0.17mW	-114.0 dBc/Hz	0.38ps
	Ring	0.17mW	-84.0 dBc/Hz	**12.0ps**
		174mW	-114.0 dBc/Hz	0.38ps

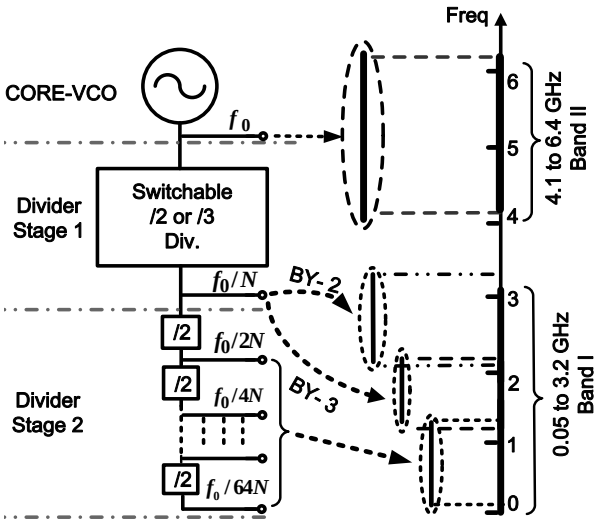

Fig.1 Frequency plan and proposed architecture

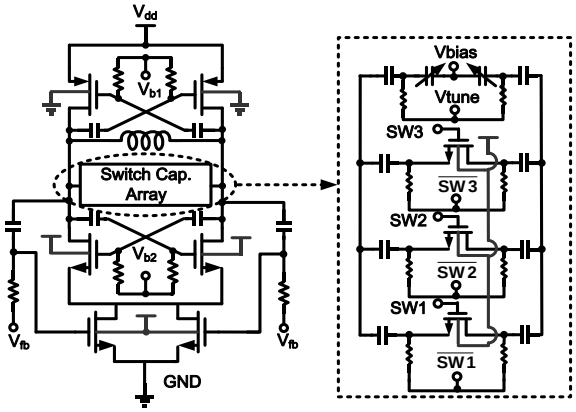

Fig.4 Schematic of 0.5-V core-VCO

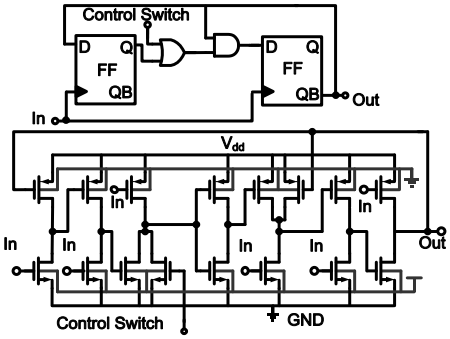

Fig.2 Proposed 0.5-V div-by-2/3 divider stage 1

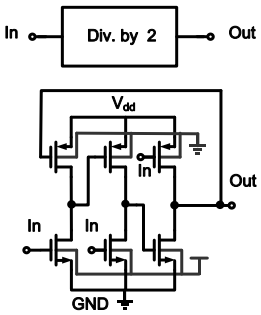

Fig.3 Proposed 0.5-V divider stage 2

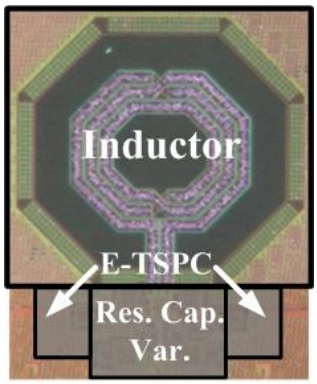

Fig.5 Chip microphotograph

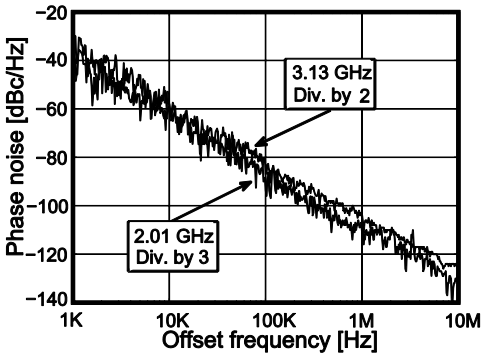

Fig.6 Measurement results of phase noise

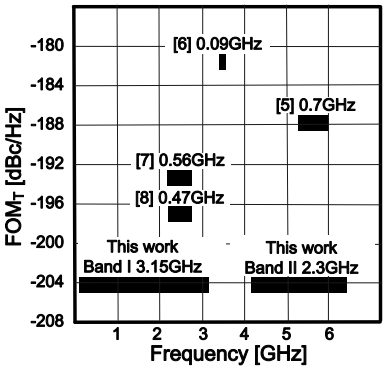

Fig.7 Comparison of FOM_T and tuning range

TABLE II Comparison of published ultra-low-voltage VCOs

-	Unit	[5]	[6]	[7]	[8]		[9]	This work	
Topology	-	LC	LC	LC	LC		Ring	LC with frequency extension	
V_{DD}	V	0.6	0.5	0.9	0.5	0.43	0.5	0.5	
Frequency	GHz	5.3~6	3.65~3.76	2.17~2.73	2.15~2.62		0.12 ~1.3	4.1 ~ 6.4	0.05 ~ 3.2
Jitter	ps	<1	<1	<1	<1		>15	<1	
Tuning range	MHz	700	90	560	470		1180	**5450**	
FTR	%	8.1	3	22.8	20		83	44	194
FOM_T	dBc/Hz	-188	-183	-193	-196	-197	-164	-198	**-204**