Area Reduction of Millimeter-Wave CMOS Amplifier Using Narrow Transmission Line

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Outline

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- Background
- Transmission line
  - Structure
  - Characterization
- Power amplifier
  - Schematic
  - Die micrograph
  - Simulation
- Conclusion

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Background

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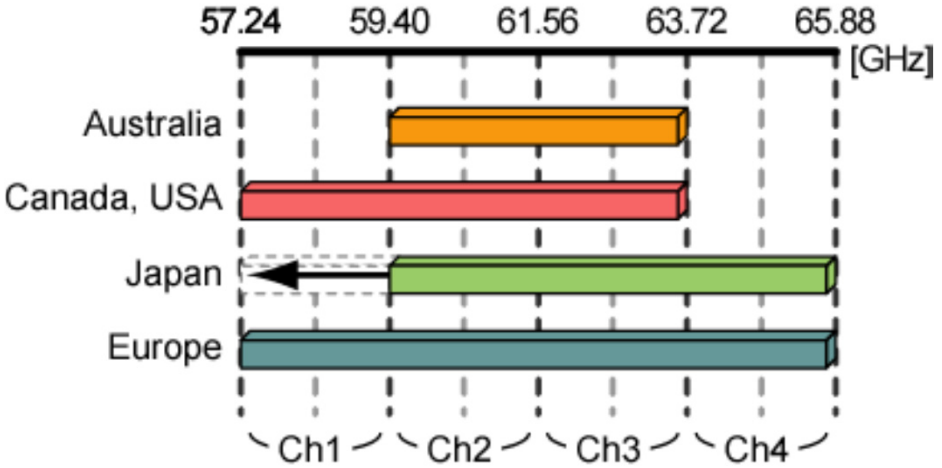
Characterization of 60GHz

☹ Attenuation is large.

☺ Wide bandwidth can be used without license.

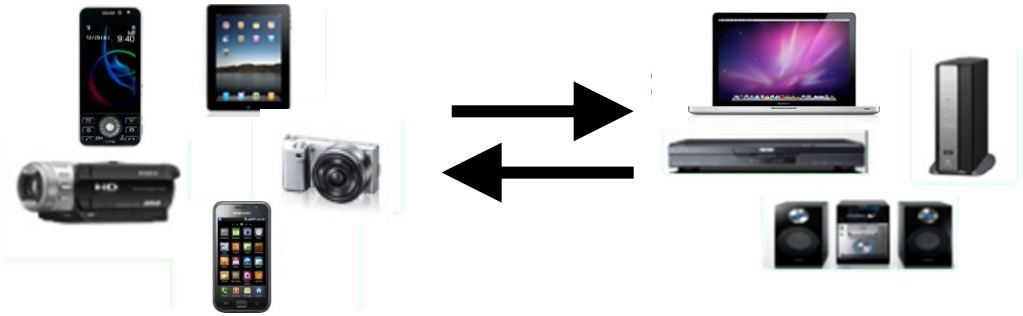
Suitable for short range and very high-speed wireless communication



MIC The radio use web site:

http://www.tele.soumu.go.jp/index.htm

Application



High-speed file/data transfer

3.5Gbps(QPSK)

7Gbps(16QAM)

（IEEE802.15.3c ）

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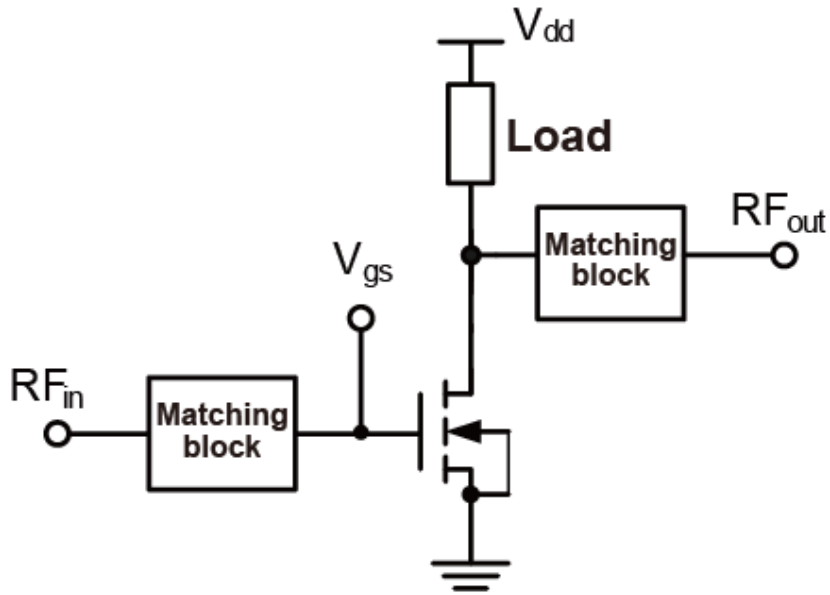
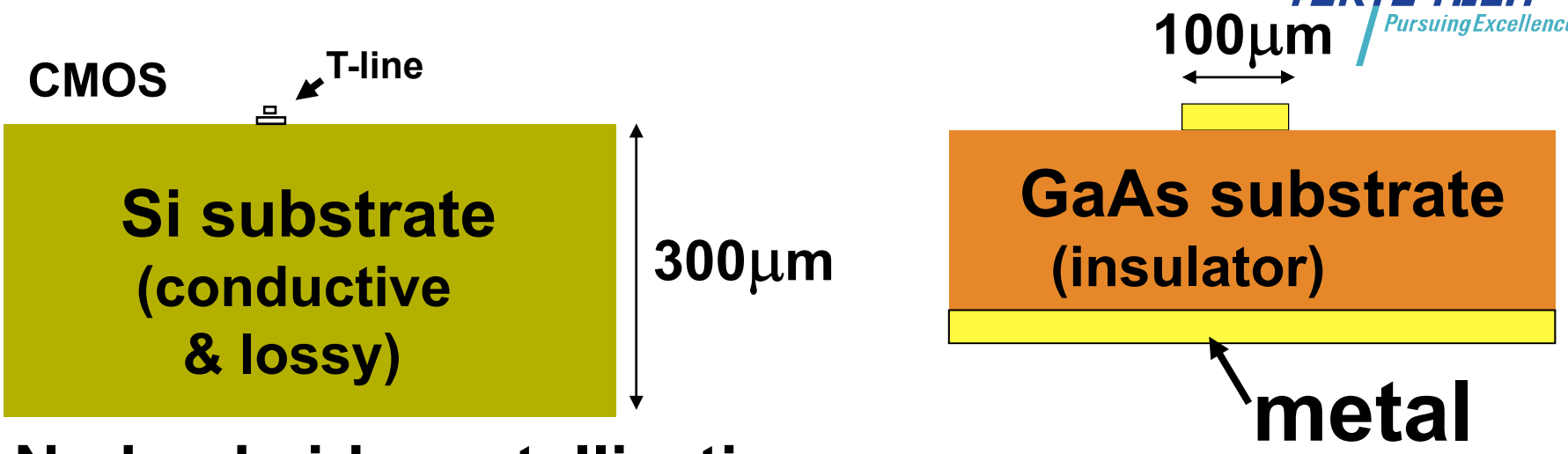
60GHz power amplifier



Matching block

- Lumped-element component
  - ☹Very widely
  - ☹Scalable model is difficult to be built.
- Transmission line(TL)
  - ☺Scalable

Loss of passive devices



No backside metallization

Conductor loss + Substrate eddy-current loss

50Ω T-line loss: 0.5 – 1.5dB/mm @60GHz

	Si CMOS	GaAs
Wire width	10μm	100μm
Wire thickness	1 – 2μm	10μm
Dielectric thickness	< 5μm	100μm

The structure of TL

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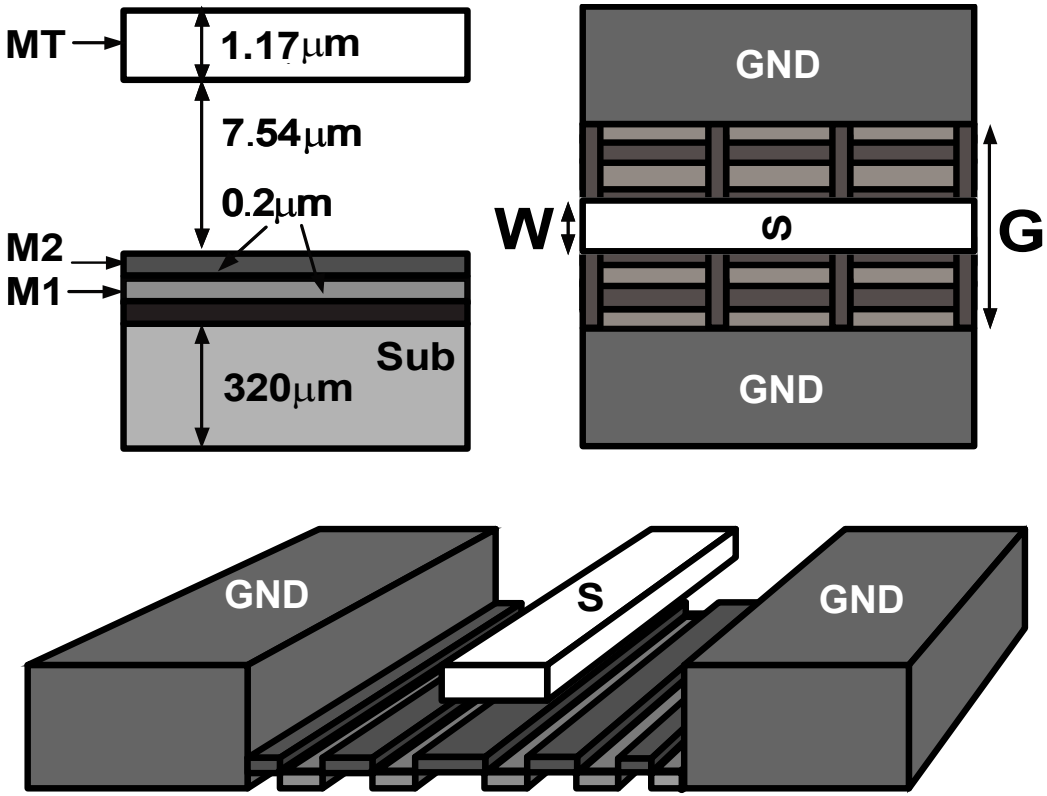

W: The width of signal line

G : The distance between the side grounds

The optimization of TL by W and G

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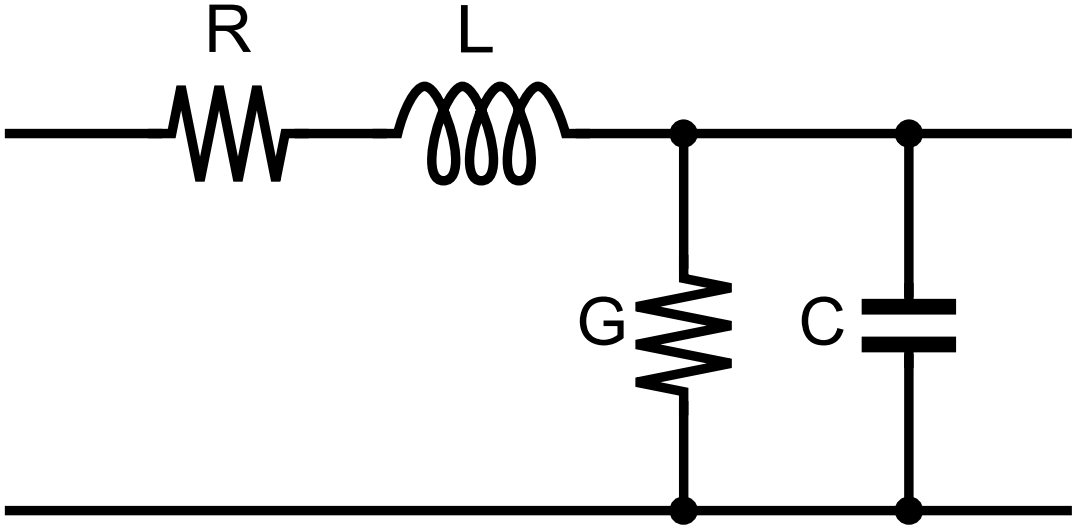
TL at 60GHz



Equivalent circuit

$$\alpha \approx \frac{R}{2Z} = \frac{R}{2}\sqrt{\frac{C}{L}}$$

$$\beta \approx \omega\sqrt{LC}$$

$$Q = \frac{\beta}{2\alpha}$$

G is not so large in CMOS.

Larger R, L

Larger α, β

Wavelength

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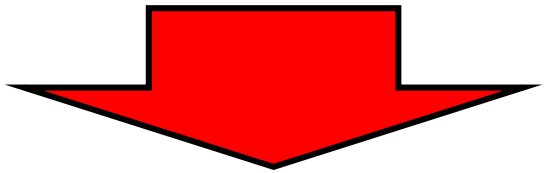
Wavelength of transmission line:

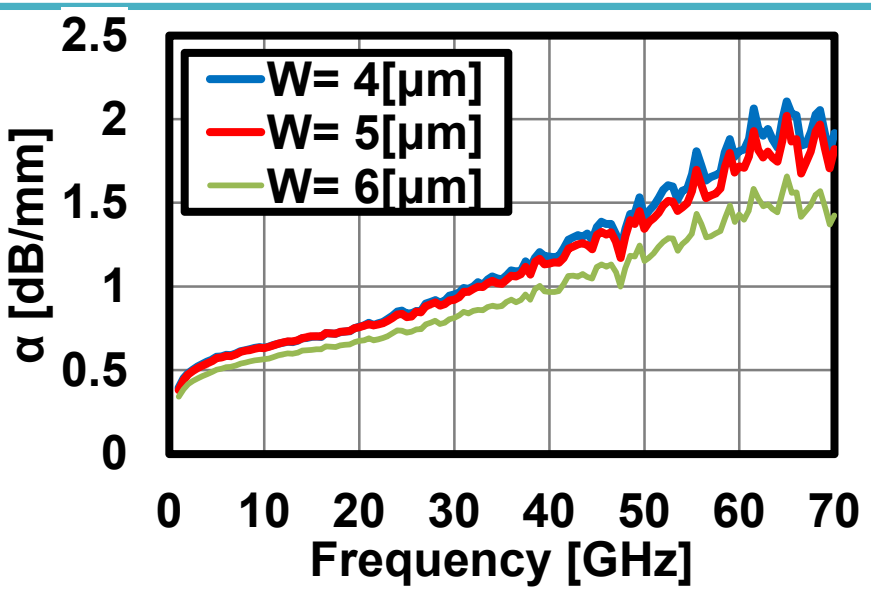
$$\lambda = \frac{2\pi}{\beta}$$

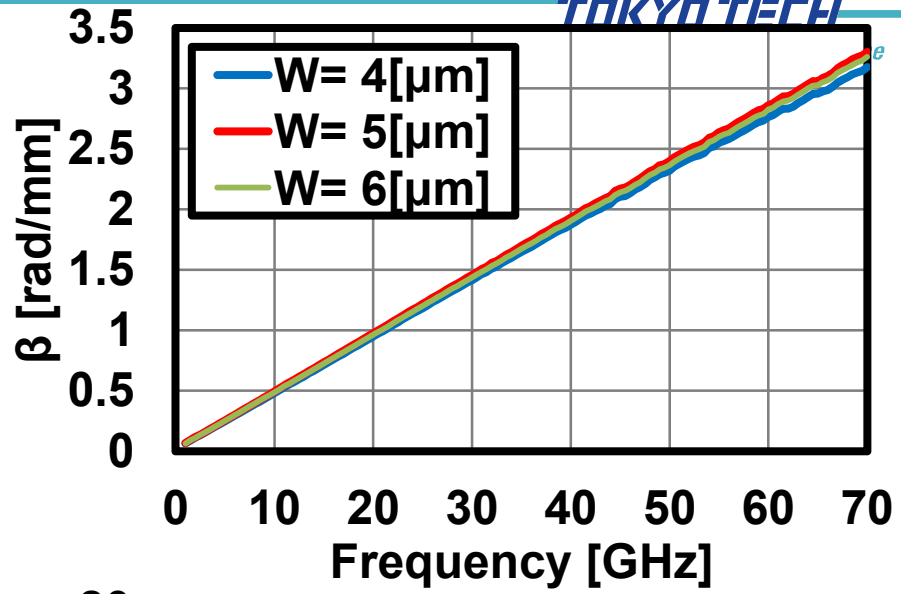
Larger β ⇒ **Smaller wavelength**

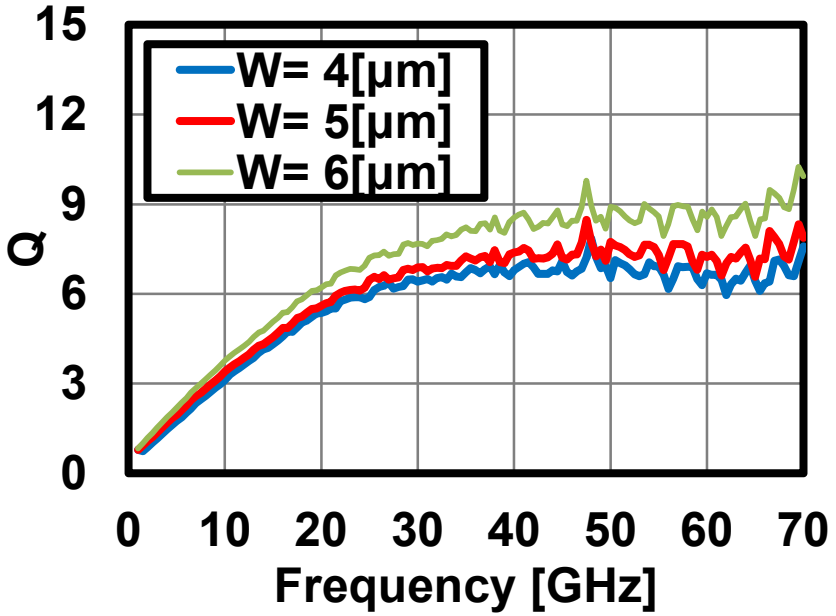


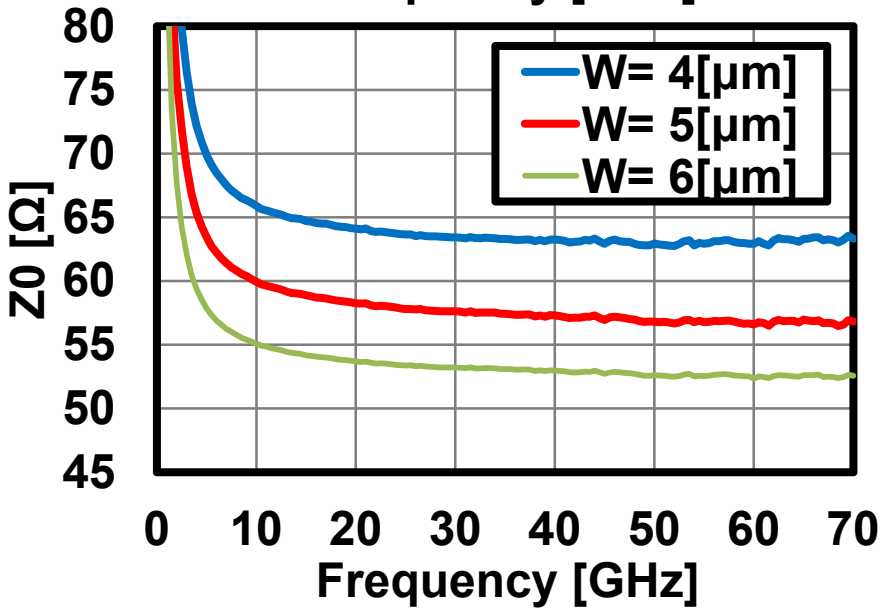
Narrow TLs lead to shorter matching blocks.

The characterizations of TL









G=20μm is fixed and W is varied.

The characterizations of TL

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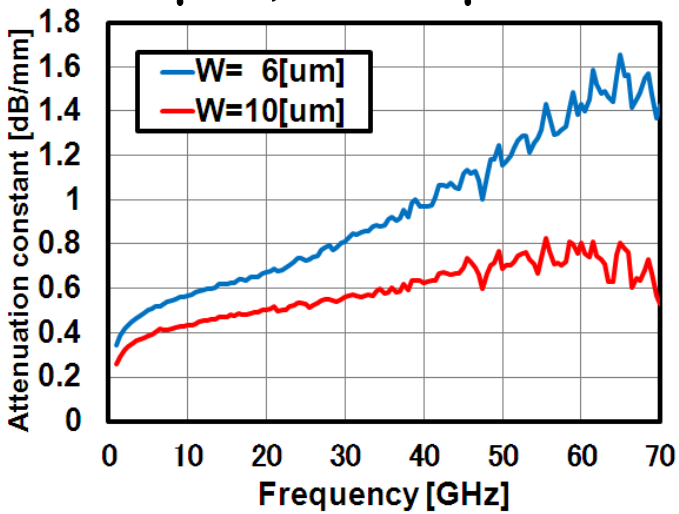
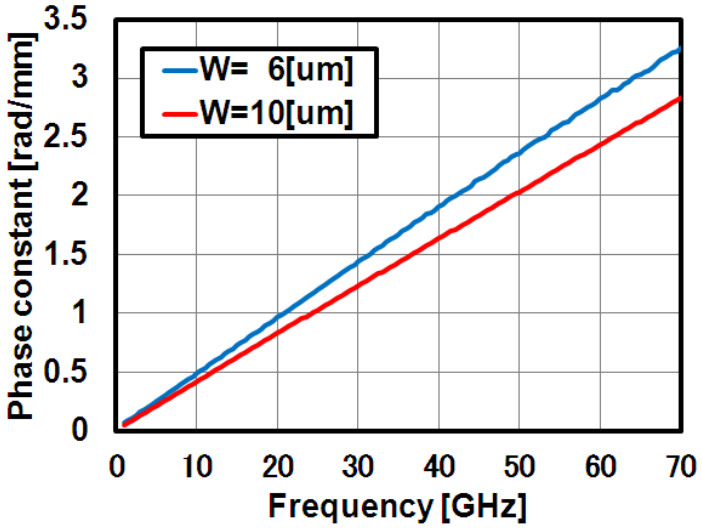
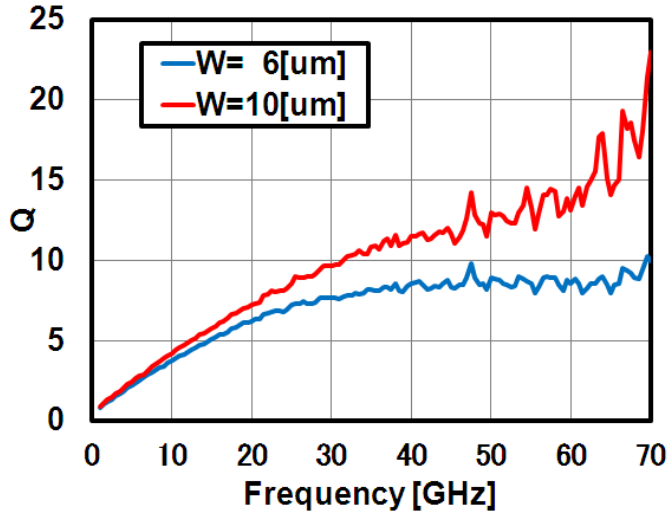
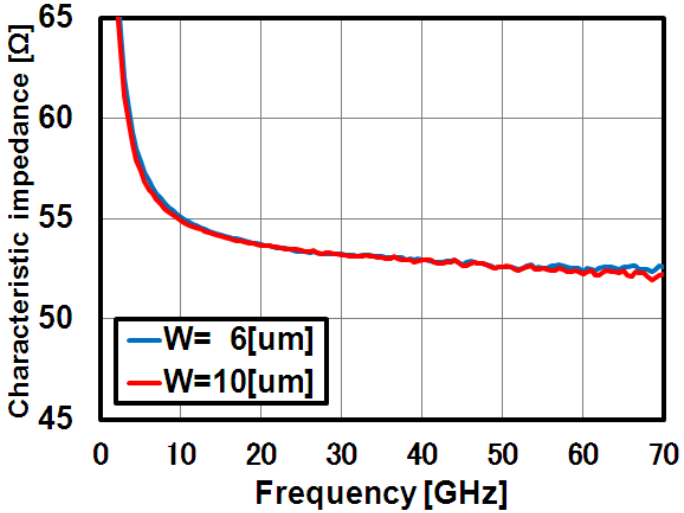
- W= 6μm, G=20μm
- W=10μm, G=40μm

Comparison









Schematic

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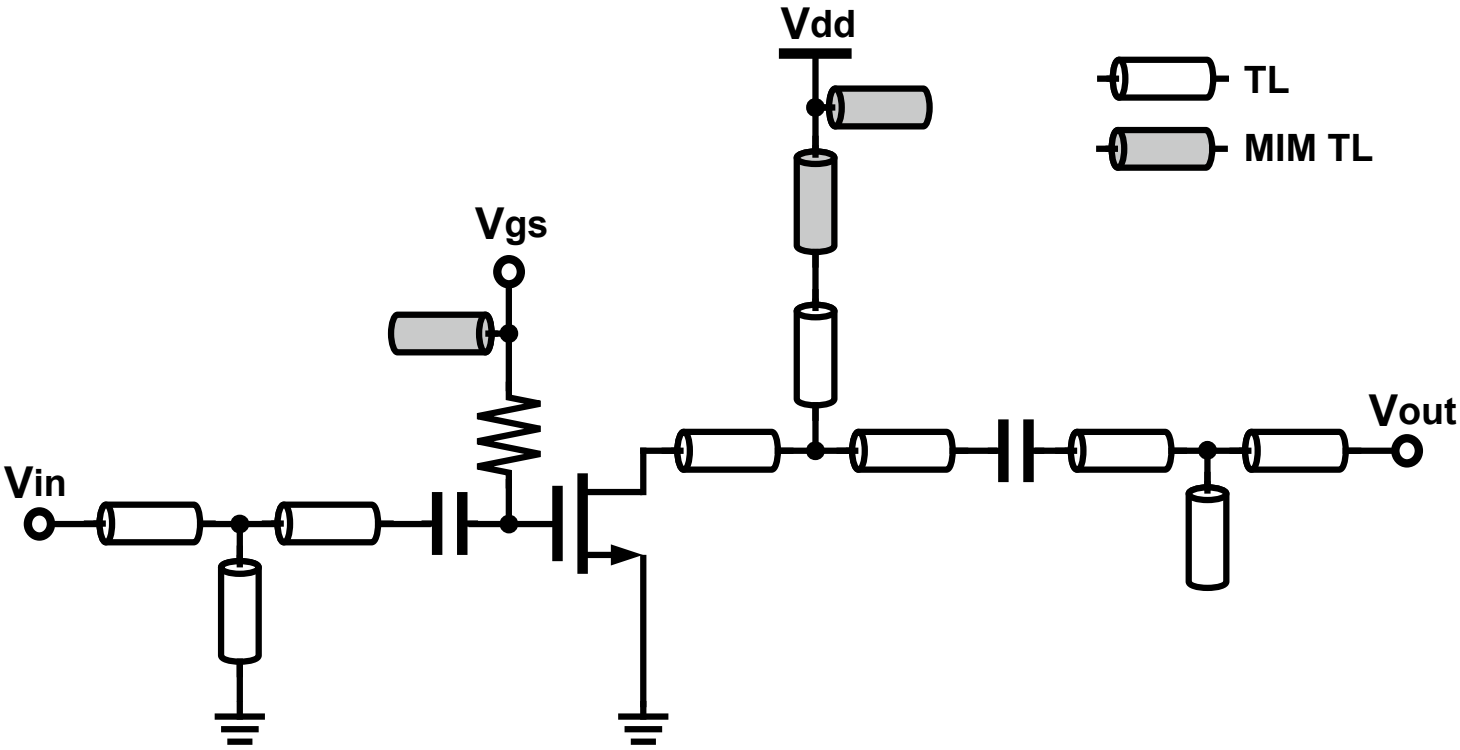
- 1-stage amplifiers are designed by using the TLs of W=6 and 10μm for matching blocks.



- 65nm CMOS process
- Transistor size: 2×20μm

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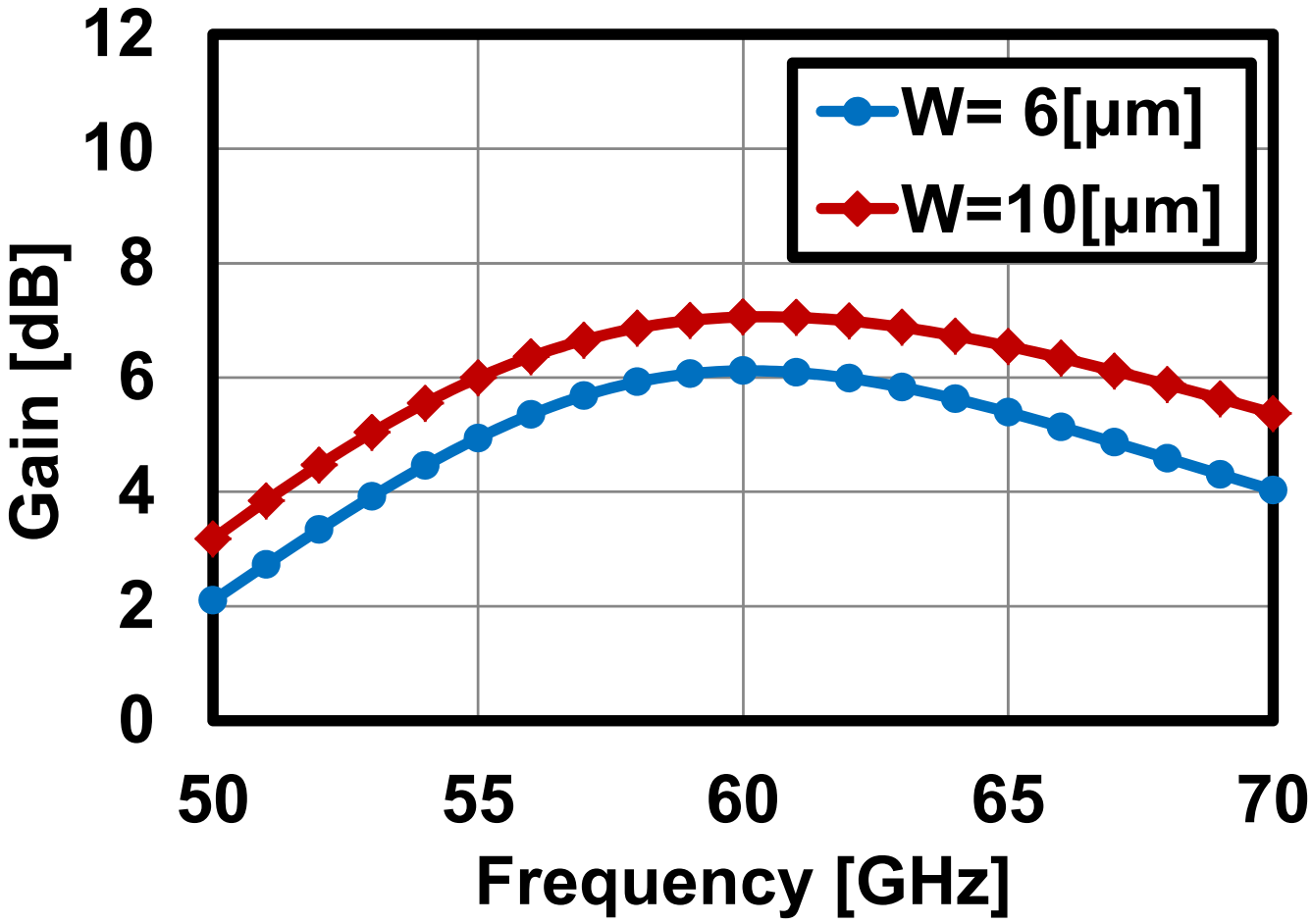
Simulation (Power gain)



- W= 6μm : 6.1dB
- W=10μm : 7.1dB

Loss per wavelength

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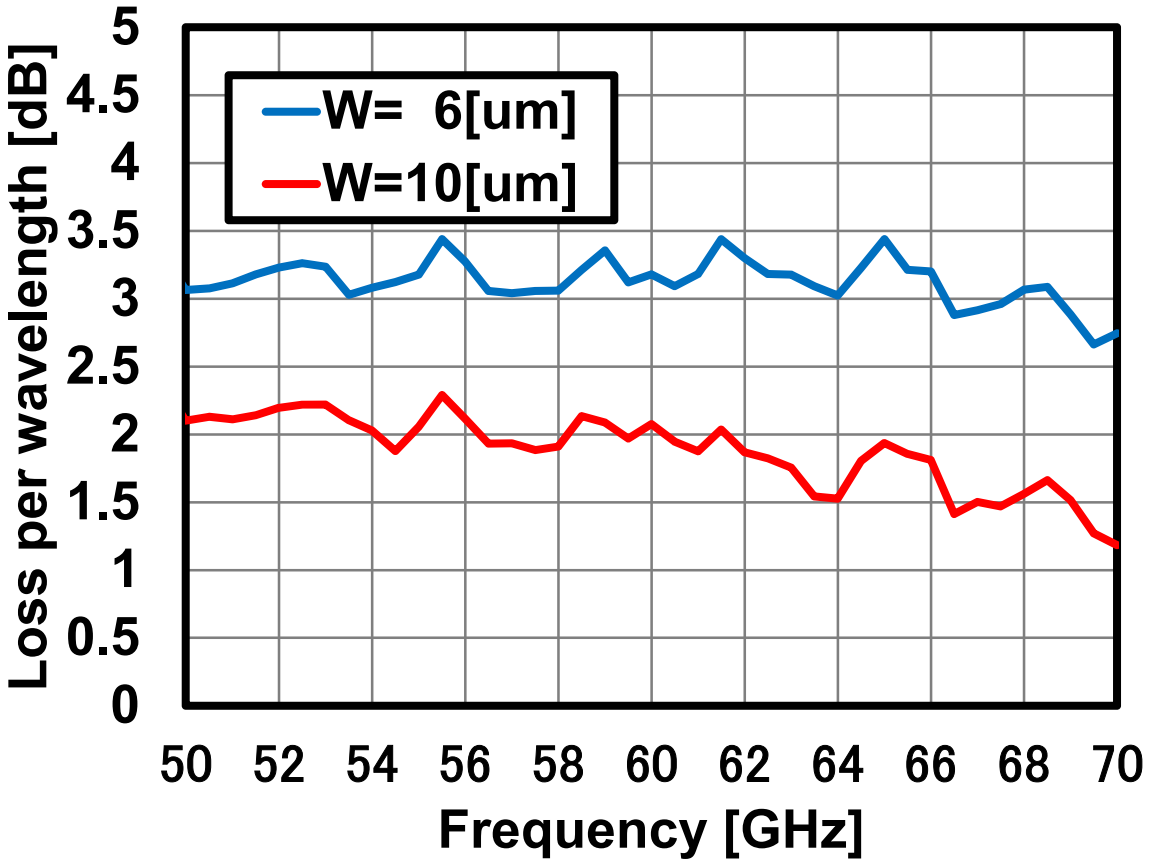

- **W= 6μm : 3.2dB**
- **W=10μm : 2.1dB**

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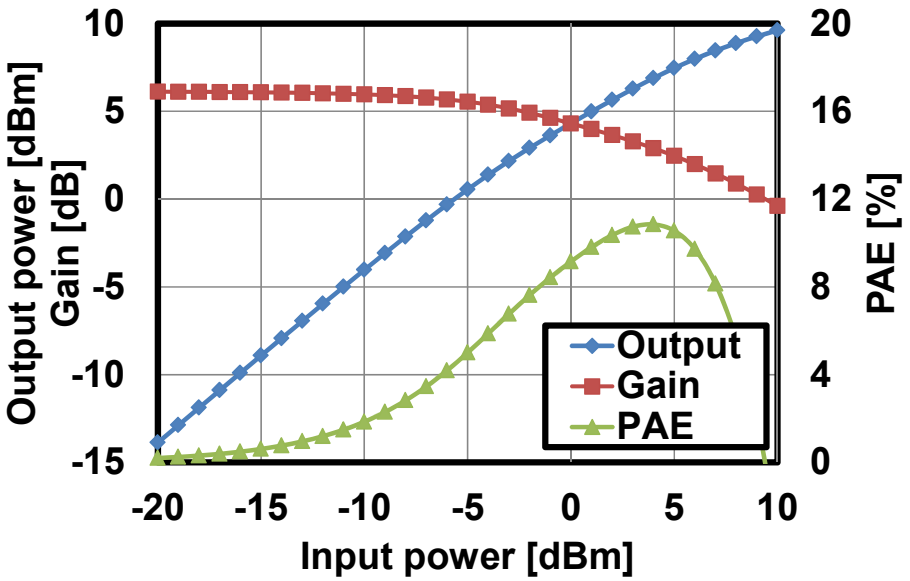
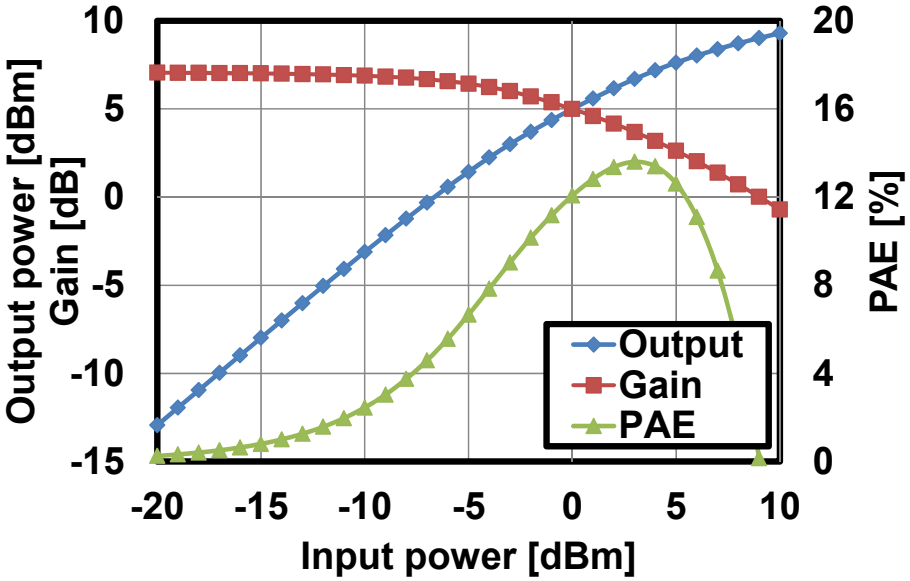
Simulation (Power sweep)





(a)W = 6μm

- P_{1dB}=2.2 dBm
- P_{sat}=9.6dBm
- PAE@P_{1dB}=6.8%

(b) W = 10μm

- P_{1dB}=3.0dBm
- P_{sat}=9.3dBm
- PAE@P_{1dB}=9.0%

The die micrograph

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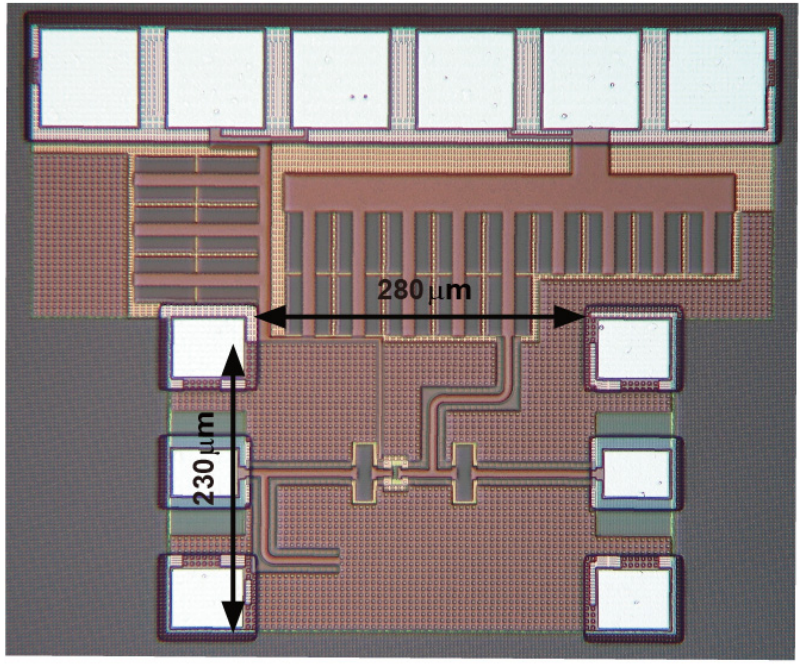
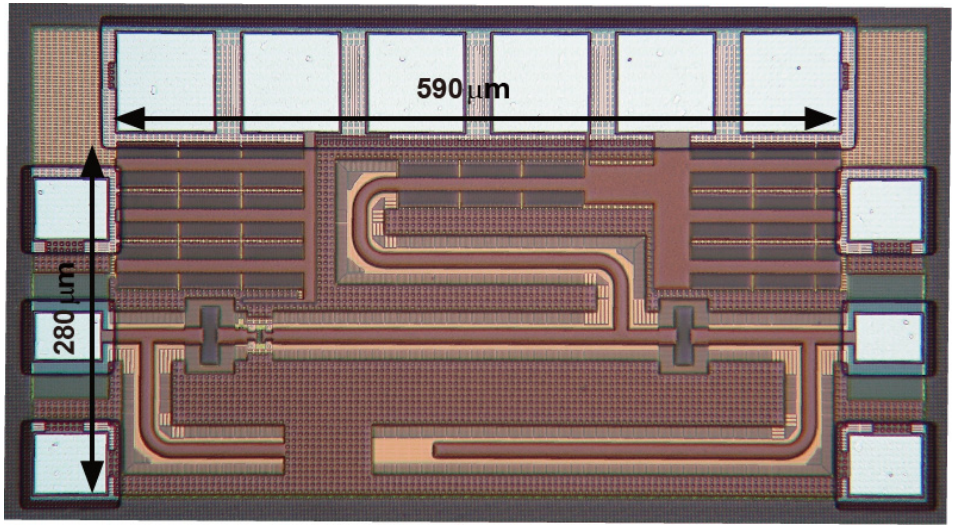


(a) W = 6μm



(b) W = 10μm

- W= 6μm : 230μm × 280μm
- W=10μm : 280μm × 590μm

Using narrow TLs reduced chip area by 60%.

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Conclusion

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- **Transmission line with 6μm signal line width is used to investigate area reduction of mmW amplifiers.**
- **The core size of the amplifier is reduced by 60% while achieving the standard performance.**