A 60GHz CMOS Power Amplifier Using Varactor Cross-Coupling Neutralization with Adaptive Bias

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Outline

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- Background
- Capacitor cross-coupling method
- Proposed varactor cross-coupling method
  - Applied capacitor cross-coupling
  - The optimal capacitance is designed by using adaptive bias
- Measurement result
  - Power gain
  - Power added efficiency (PAE)
  - Power consumption
- Performance comparison
- Conclusion

Background

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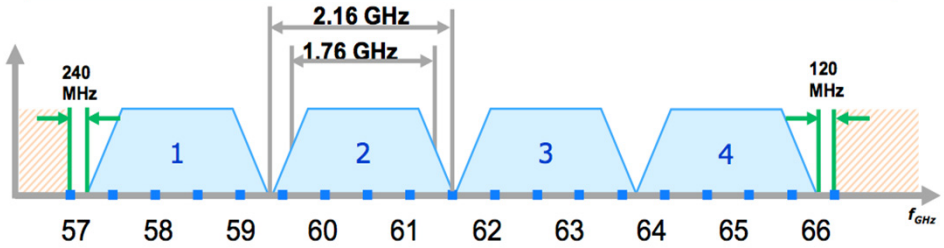
Advantage of 60GHz

- ☹ Enable communication distance is short.
- ☺ High speed wireless communication can be realized without lisence.

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (GHz)	Roll-Off Factor
A1	57.24	58.32	59.40	1.76	0.227
A2	59.40	60.48	61.56	1.76	0.227
A3	61.56	62.64	63.72	1.76	0.227
A4	63.72	64.80	65.88	1.76	0.227



IEEE 802.15.3c

・QPSK

⇒ 3.5Gbps/ch

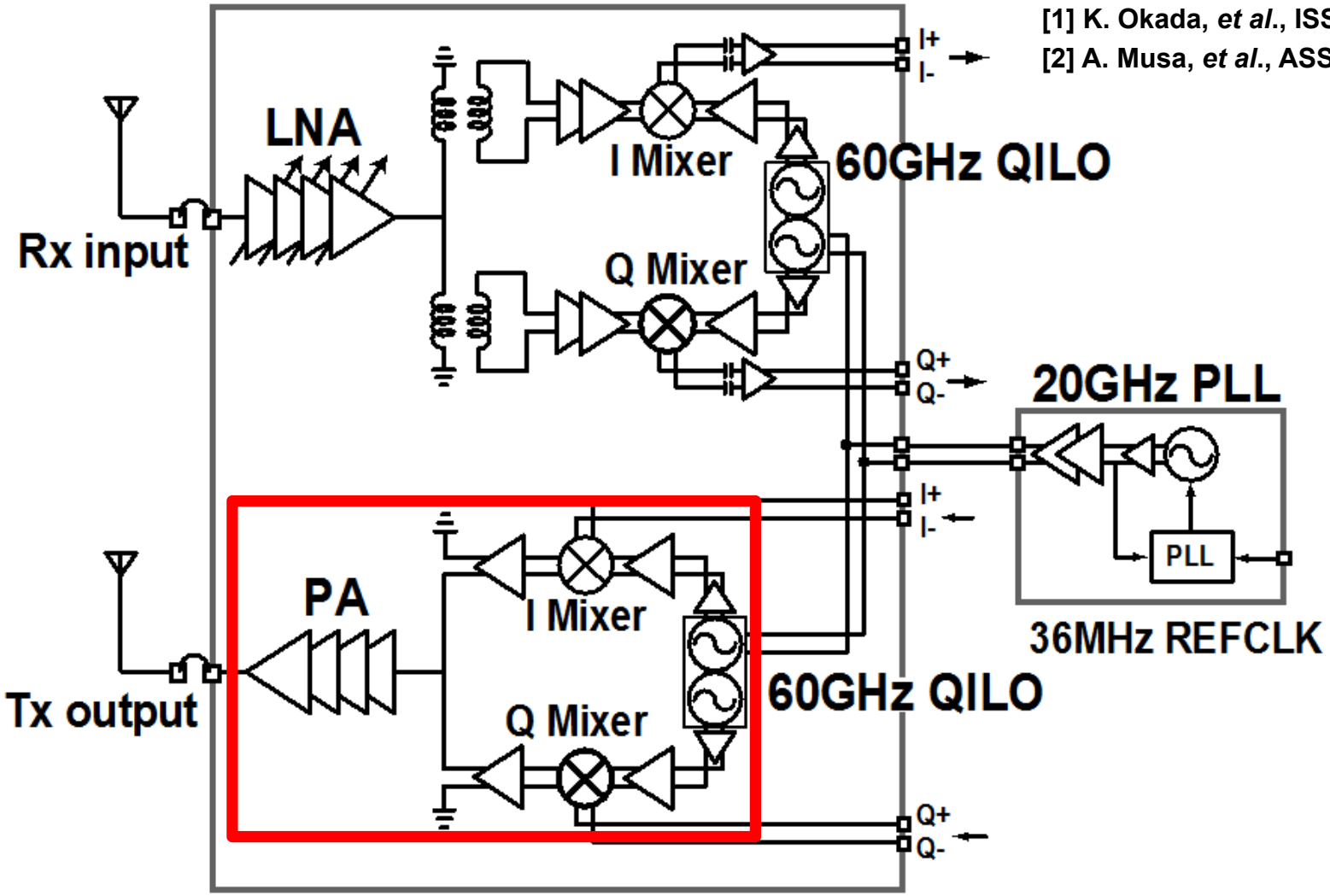
・16QAM

⇒ 7.0Gbps/ch

Gbps Wireless Communication

A 60GHz wireless transceiver[1], [2]

[1] K. Okada, *et al.*, ISSCC 2011
[2] A. Musa, *et al.*, ASSCC 2010



At 60GHz wireless communication

- **High output power**
- **High efficiency**

Transmission Line

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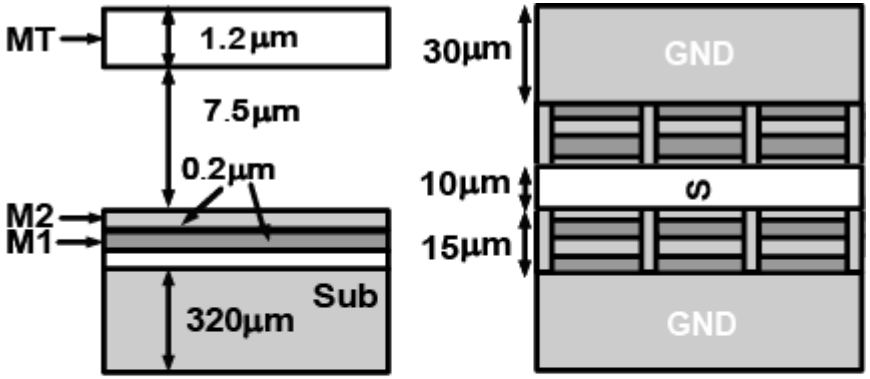
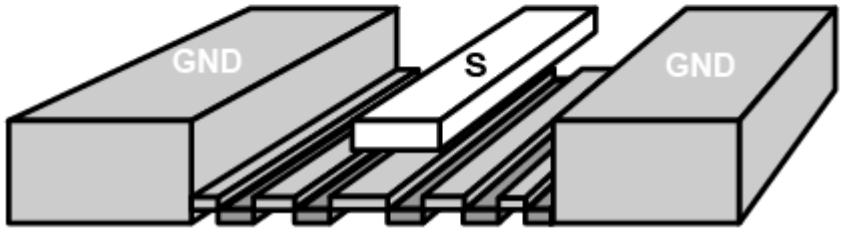
At 60GHz, the size of component is not negligible comparing the wavelength.

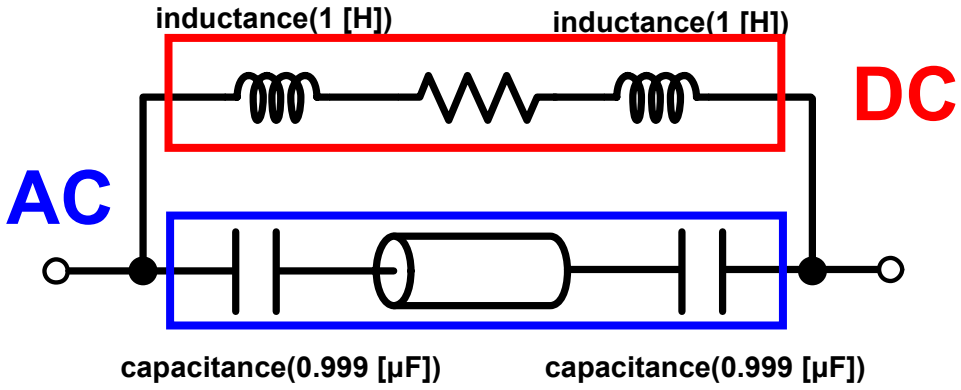
☹ **lumped constant**

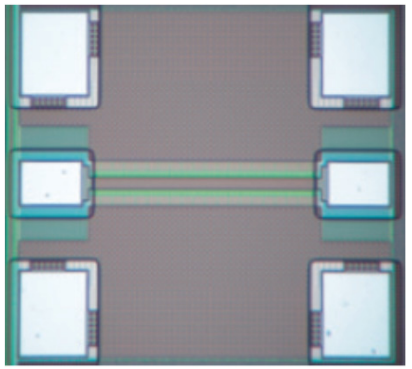
☺ **distributed constant ➡ transmission line is used.**





The structure of TL.





Model and photo.

Matsuzawa & Okada Lab.

MIM Transmission Line

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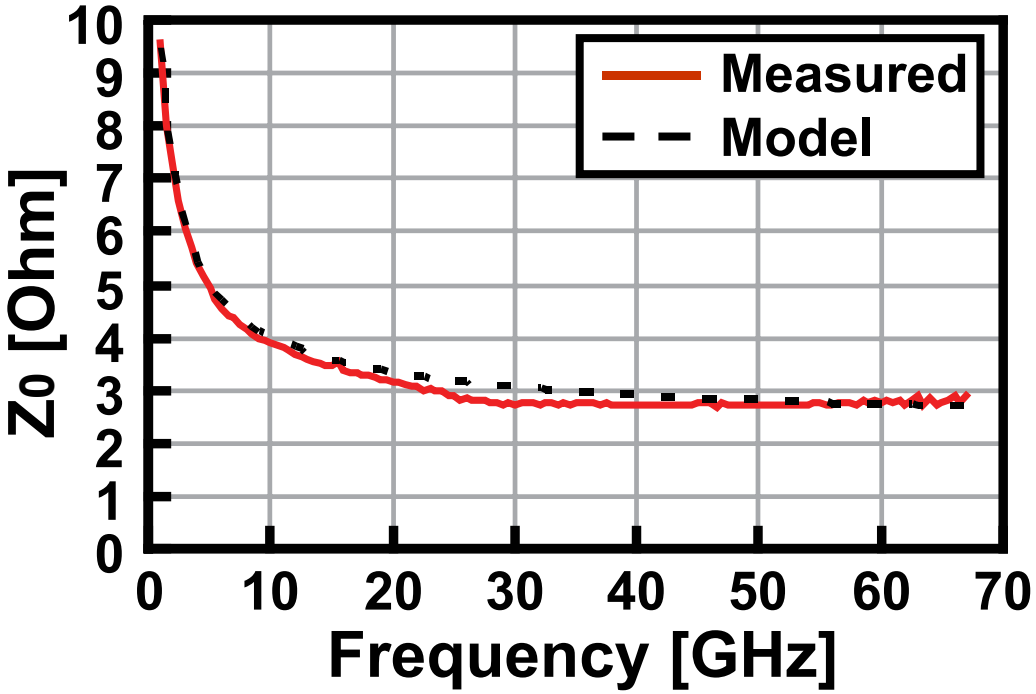
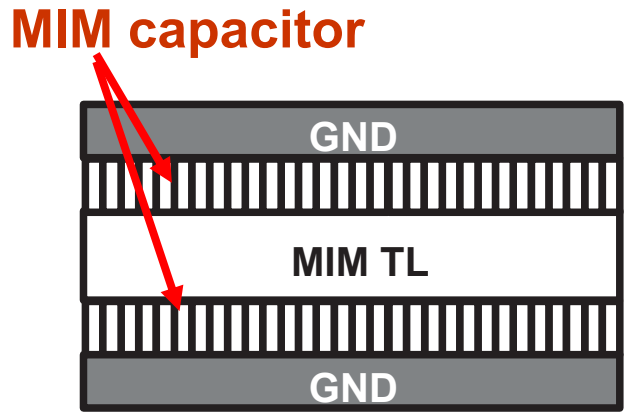
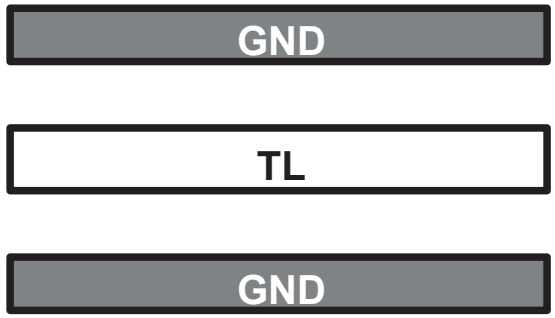
- De-coupling use
- Modeling accuracy
- Avoiding self-resonance of parallel-plate capacitors





MIM transmission line



50Ω transmission line

[3] T. Suzuki, *et al.*, ISSCC 2008

Parasitic capacitance between gate and drain

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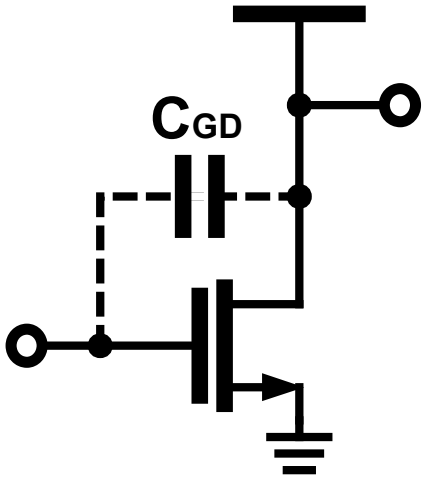
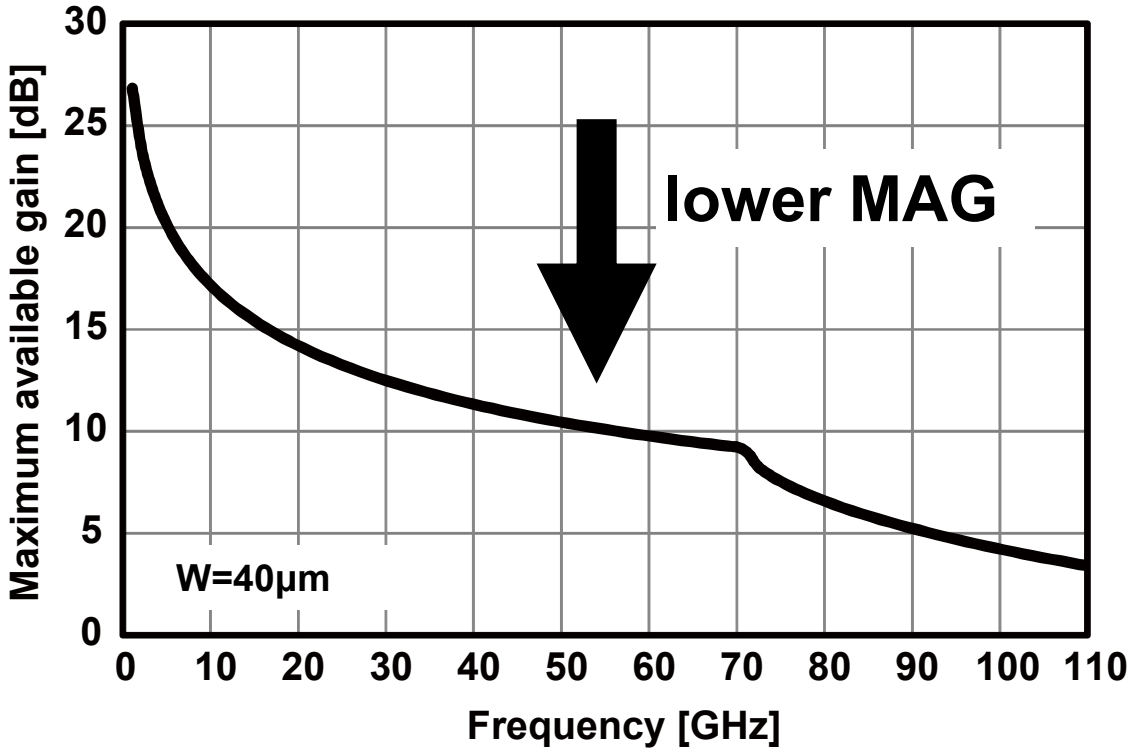
Parasitic Capacitance



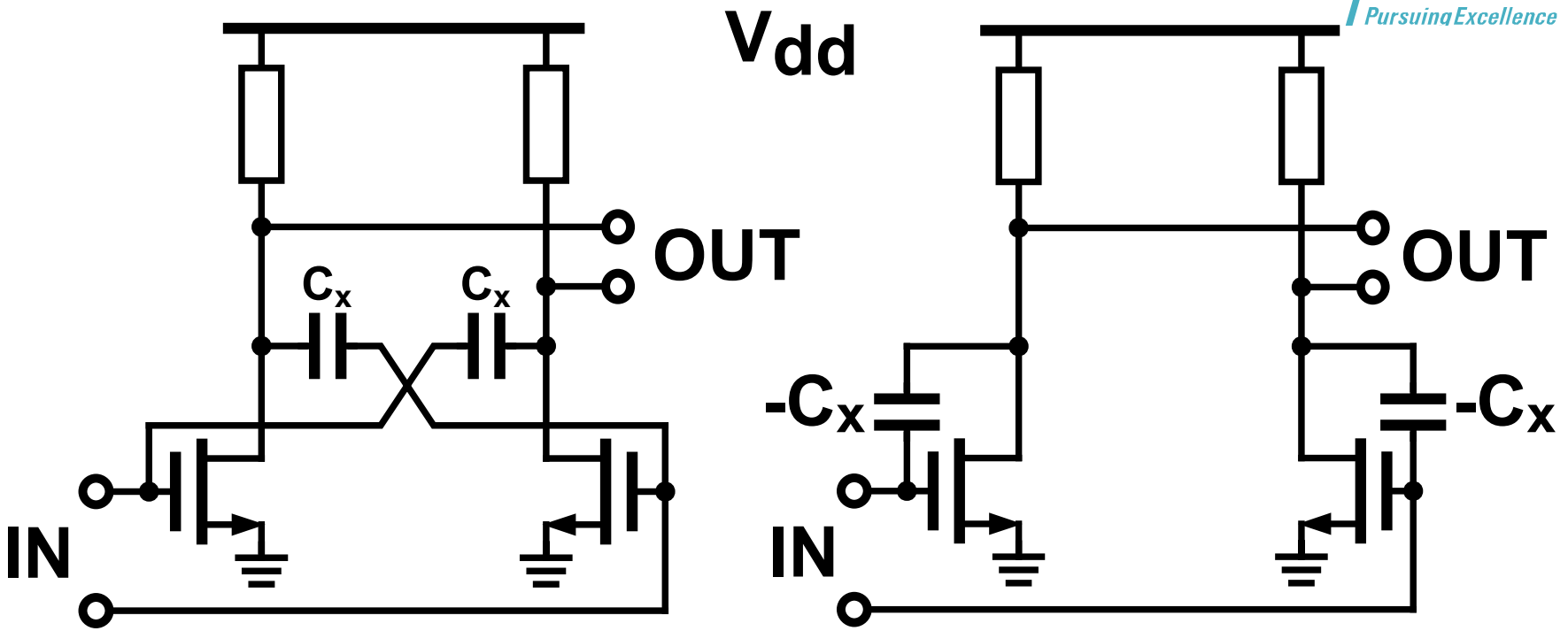
$$C_{GD} = -\frac{\mathrm{Im}[Y_{12}]}{j\omega}$$



Parasitic capacitances causes low reverse isolation and low gain.

Matsuzawa & Okada Lab.

Capacitor cross-coupling[3]

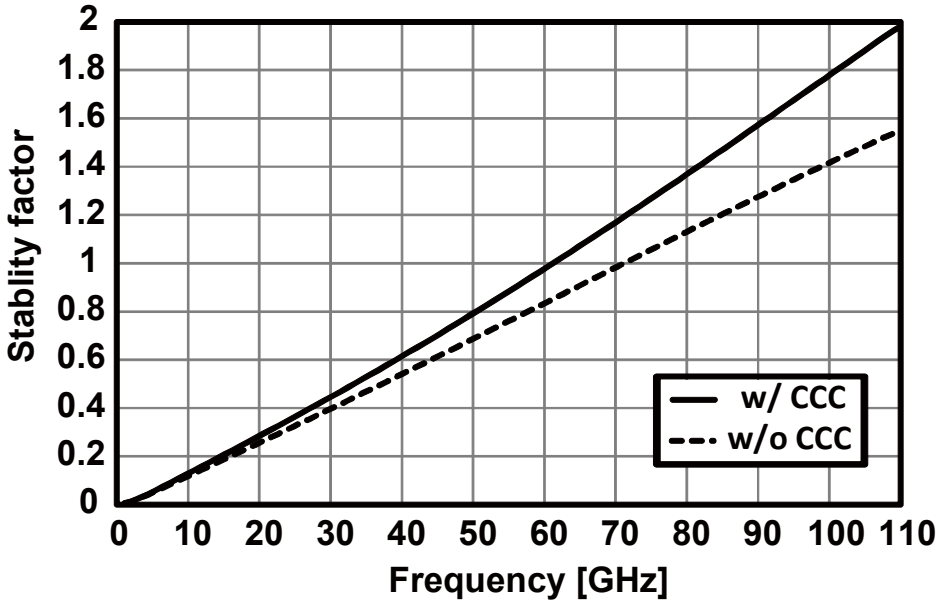


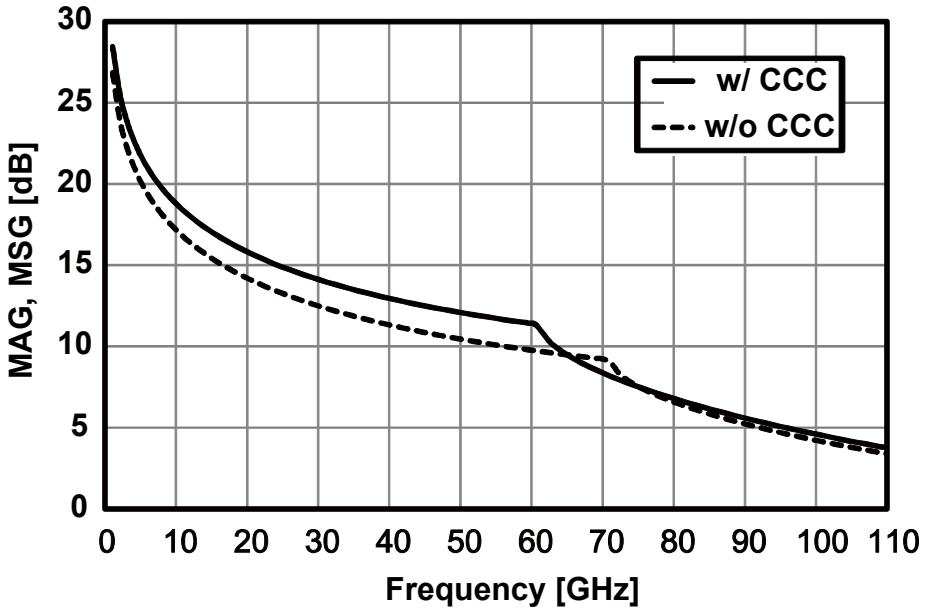
A cross-coupled capacitor between gate and drain of the opposite-side transistor works as negative capacitor.

– The reverse isolation is improved.

[4] W. L. Chan, *et al.*, ISSCC 2009

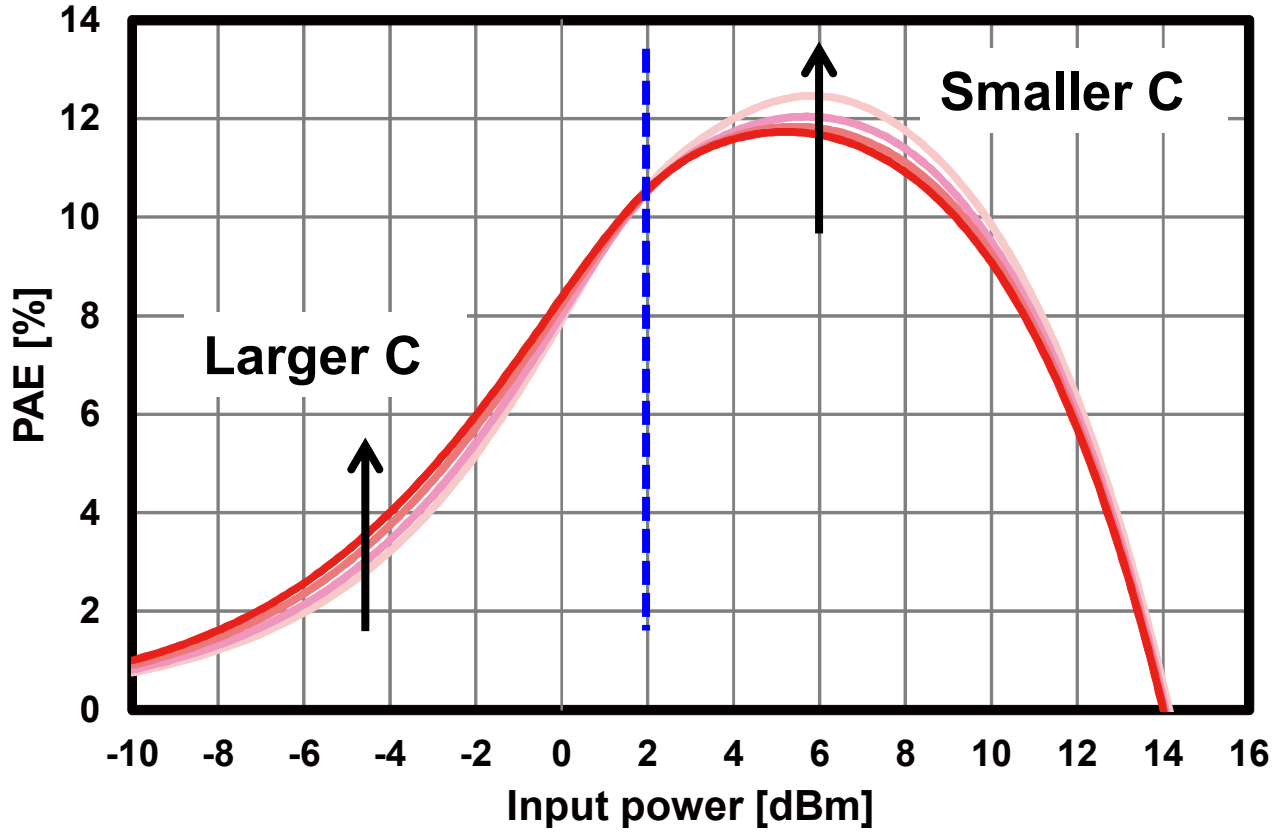
Simulation result of CCC





- **Stability Factor is improved across entire frequency.**
- **The maximum available gain is improved about 2dB at 60GHz.**

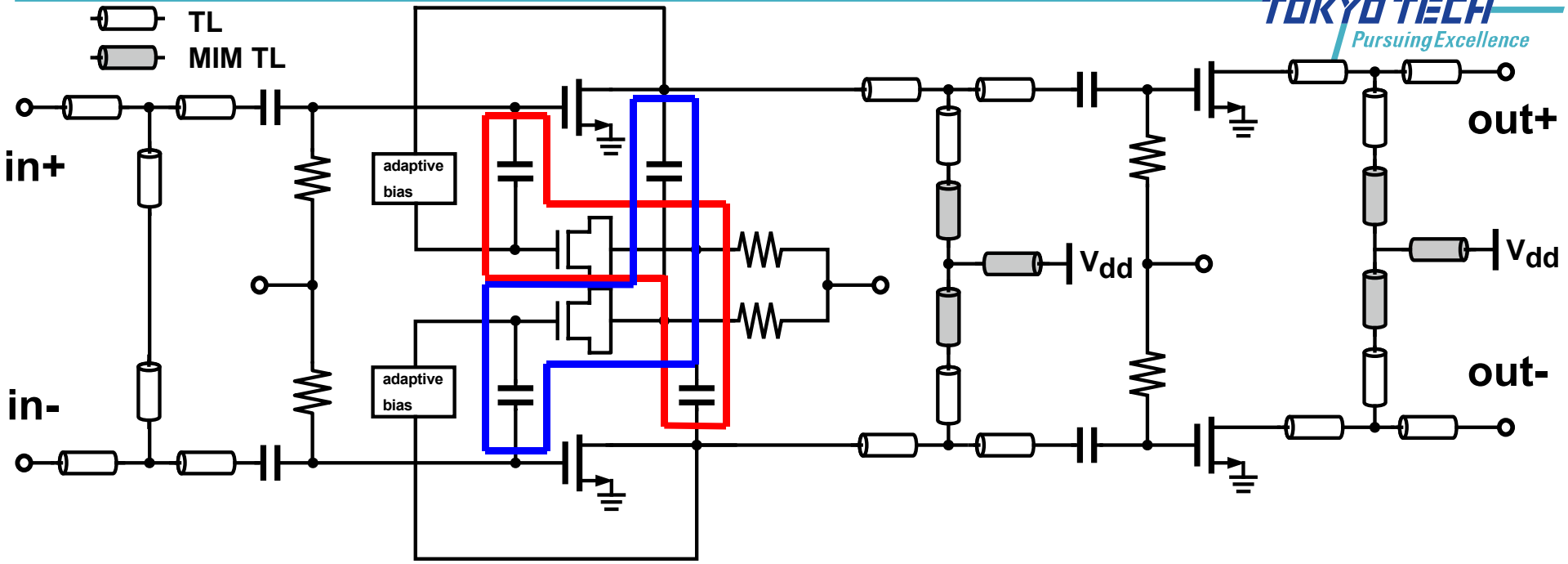
Simulation result of PAE

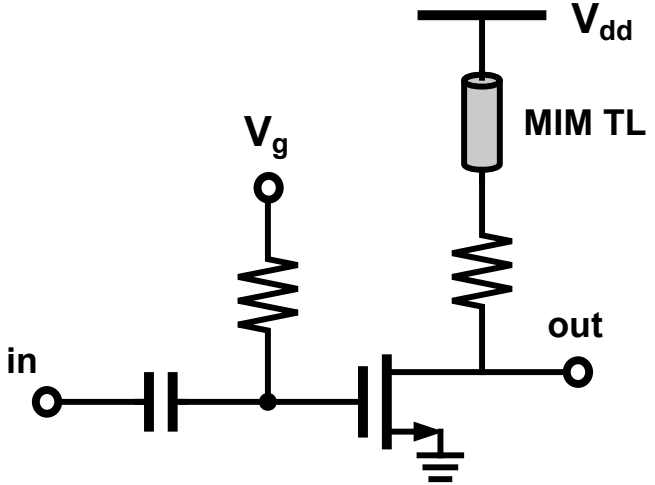


- The optimal capacitance is depended on the input power.
- Smaller input power → Larger C than C_x is better
- Larger input power → Smaller C than C_x is better

→ Varactor is used as a cross coupled capacitor

Varactor cross coupling differential PA

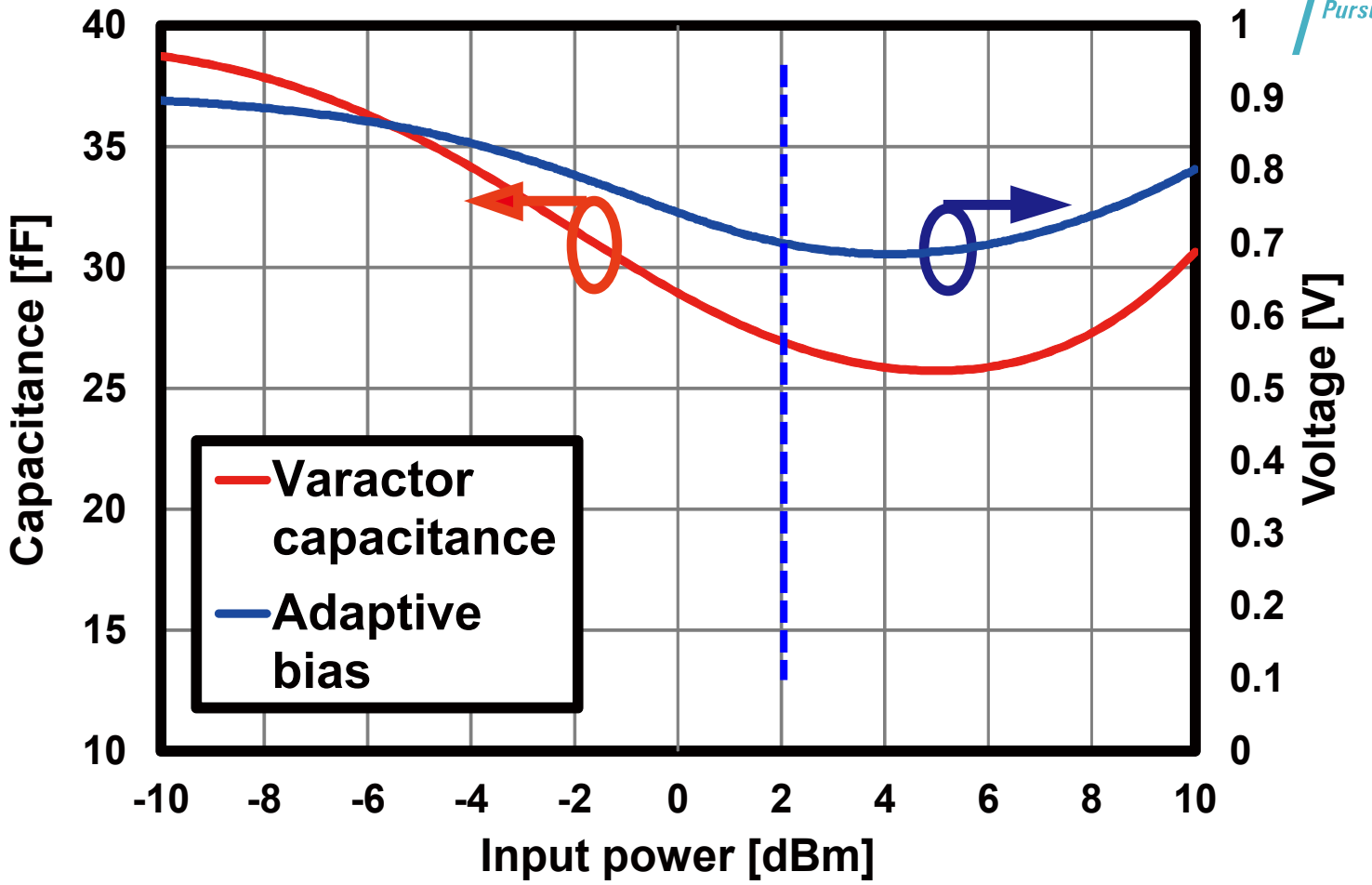




Adaptive bias circuit

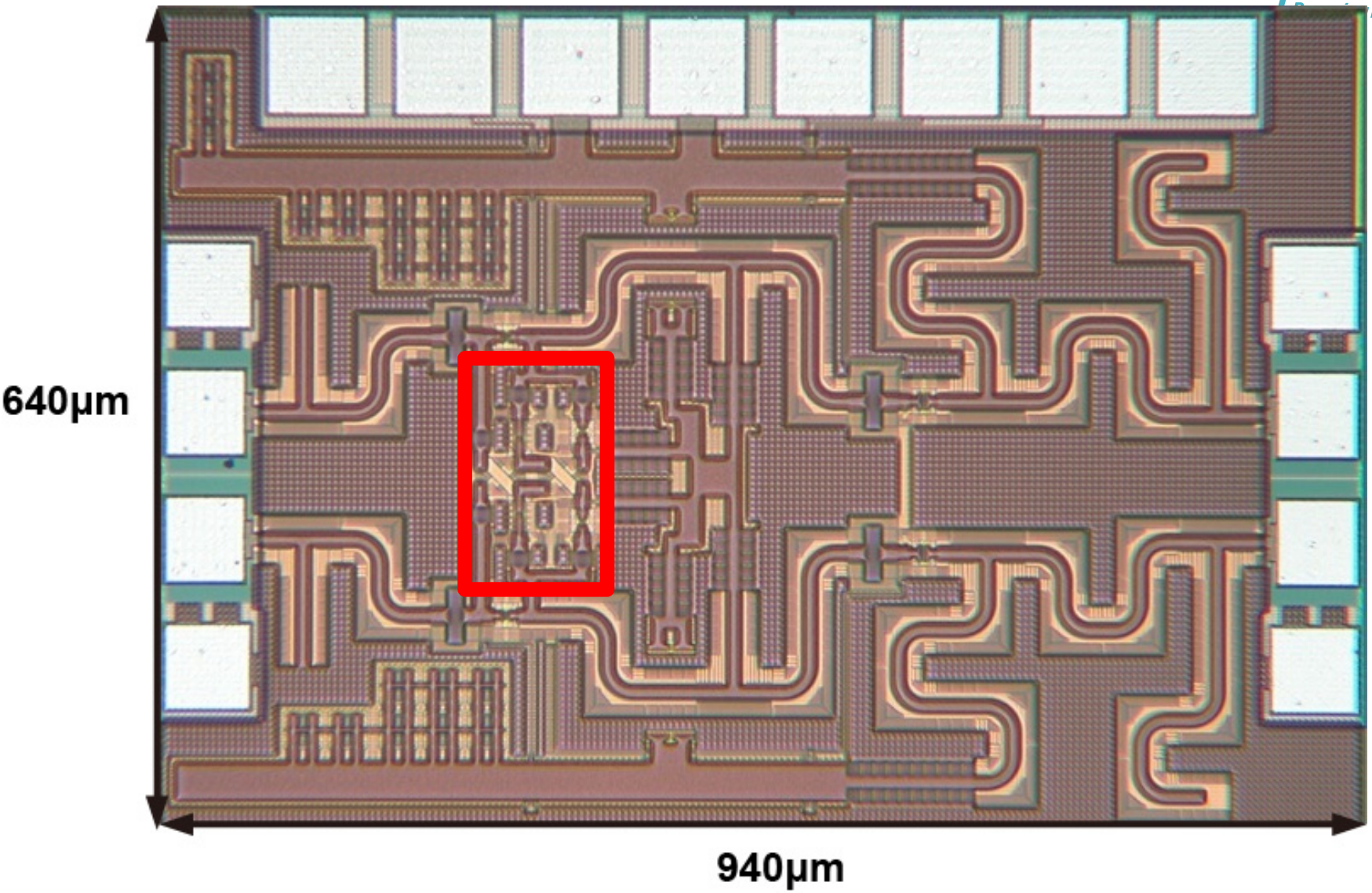
- CMOS 65nm process
- Two-stage differential PA
- Low loss transmission line
- 1.2V power supply

Simulation result of varactor

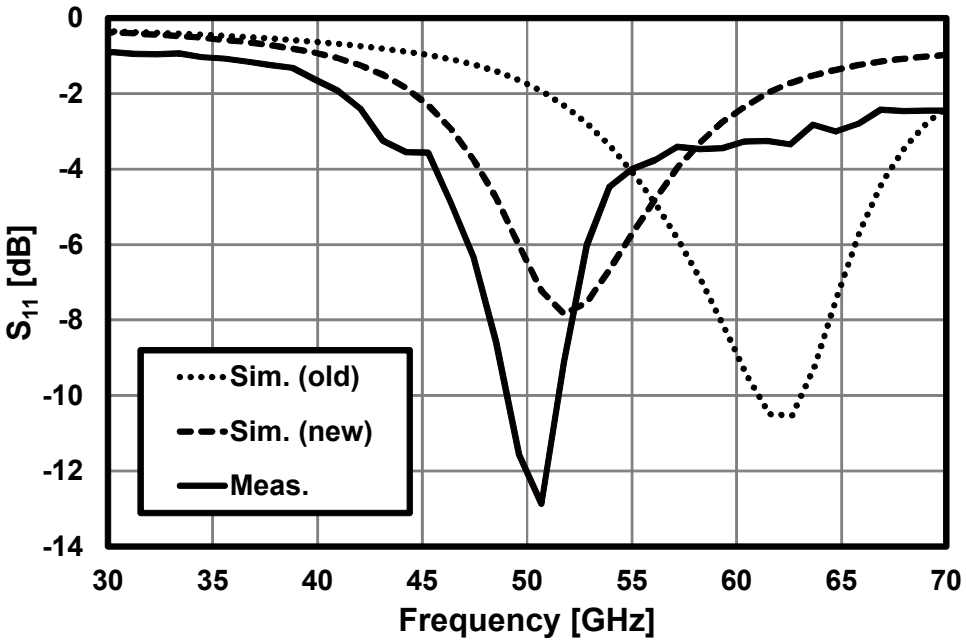


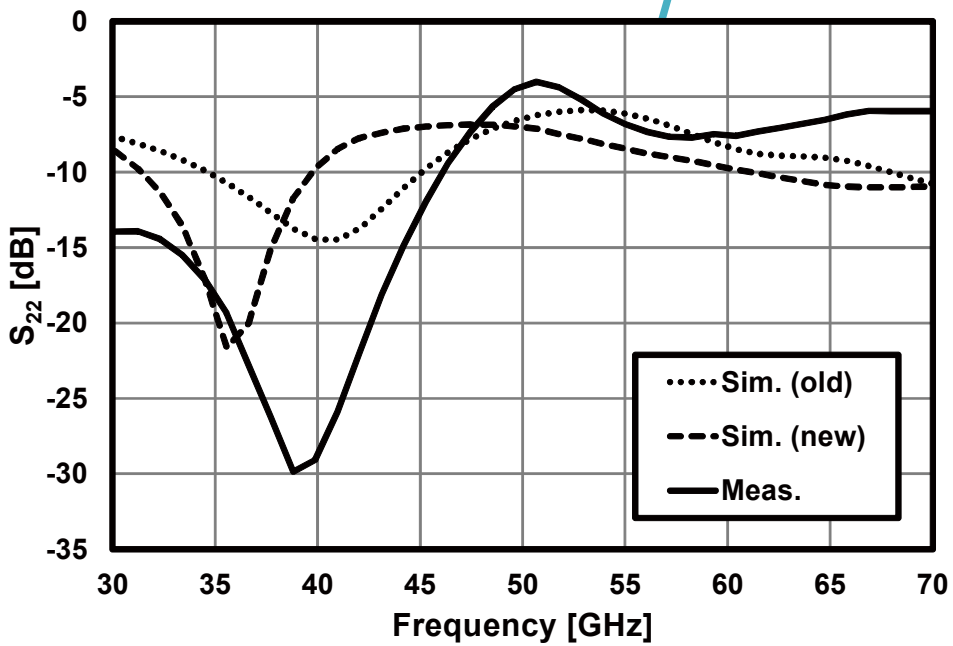
- **Optimal capacitance is realized by varying the bias of varactor using feedback of input power.**

Die photo



Measurement result (small signal)



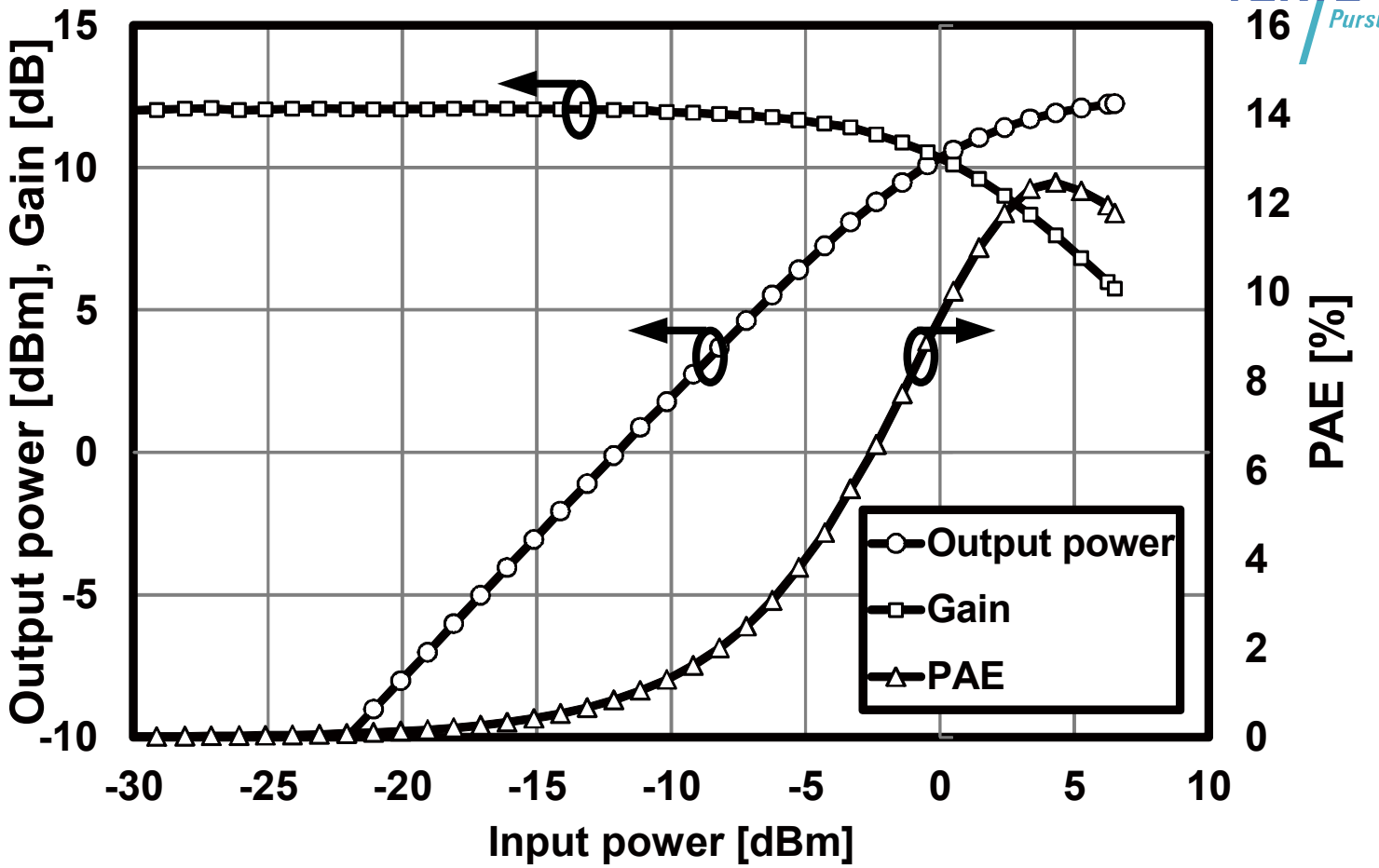


- Sim.(old) shows the result of using old models.
- Sim.(new) shows the result of using update models.

About 10GHz frequency error is generated between simulation and measurement.

➡ The accuracy of models were not good.

Measurement result (large signal)



Gain: 12.1dB **P_{sat}: 12.2dBm**

PAE at P_{1dB}: 7.7% **P_{DC}: 86mW**

Peak PAE: 12.5% **V_{DD}: 1.2V**

Performance comparison

	Tech.	Gain [dB]	P_{1dB} [dBm]	P_{sat} [dBm]	PAE@P_{1dB} [dBm]	Power [mW]	V_{DD}[V]
ISSCC 2008[5]	65nm	5.5	9	12.3	6	—	1.0
ISSCC 2009[4]	65nm	16	2.5	11.5	4.5	43.5	1.0
ISSCC 2010[6]	65nm	14.3	11	16.6	1.3	732	1.2
ISSCC 2010[7]	65nm	19.2	15.4	17.7	7	480	1.0
ISSCC 2011[8]	65nm	20.3	15	18.6	6.3	72	1.0
This Work	65nm	12.1	9.5	12.2	7.7	86	1.2

Very good PAE at P_{1dB} is realized.

[4] W. L. Chan, *et al.*, ISSCC 2009
[5] D. Chowdhury, *et al.*, ISSCC 2008
[6] B. Martineau, *et al.*, ISSCC 2010
[7] J. Lai, *et al.*, ISSCC 2010
[8] J. Chen, *et al.*, ISSCC 2011

Conclusion

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- **A 60GHz varactor cross coupled 2-stage differential power amplifier is implemented by using CMOS 65nm process.**

- **Very good power added efficiency (PAE) at 1-dB power compression point is realized in proposed CMOS power amplifier.**