A 60 GHz CMOS Power Amplifier Using Varactor Cross-Coupling Neutralization with Adaptive Bias

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***Abstract*—This paper proposes the method of varactor cross-couplng with adaptive bias. The capacitive cross-coupling neutralization contributes to improve power gain and reverse isolation. The optimized capacitance of cross-coupled PA depends heavily on the input power. Thus, the varacter is used and adaptive bias is obtained by the feedback of the input power. The 2-stage differential power amplifier is fabricated in a 65 nm CMOS process. It achieves the PAE at P_{1dB} of 7.7 % and peak PAE of 12.5 % from a 1.2 V power supply. The effect of varactor cross-coupling neutralization with adaptive bias is validated.**

***Index Terms*—Power amplifiers, CMOS, varactor, Cross-Coupling.**

I. Introduction

Recently, high-speed wireless communication at 60 GHz is attracted. This is because the very wide bandwidth around 60 GHz can be used without license in many countries, and high speed wireless communications can be realized. Moreover, the cut-off frequency of CMOS transistors are increased recently. Thus we can use the CMOS technology instead of compound semiconductors for 60 GHz RF front-end[1]. To perform the wireless communication at 60 GHz, each RF component has to be high performance. Especially, Power Amplifier (PA) is required to have high output power and efficiency.

In this work, varactor cross-coupling is used for a mmW PA, which contributes to increase the power gain and stability factor. Moreover, Power Added Efficiency (PAE) is also optimized by using adaptive bias obtained from the feedback of input power.

Section II describes the technique of capacitor cross-coupling neutralization, section III shows the method of varactor cross-coupling with adaptive bias, and section IV presents the measurement result of the PA and performance comparison.

II. Capacitive Cross-Coupling Neutralization

The challenge of designing circuit at 60 GHz is that the performance of each circuit component is decreased by parasitic capacitance. Especially, the increasing of capacitance between gate and drain lower reverse isolation, power gain and stability factor. To decrease the gate-drain capacitance(C_{GD}), the technique of capacitor cross-coupling has been used so far. This technique can be used only for differential circuit.

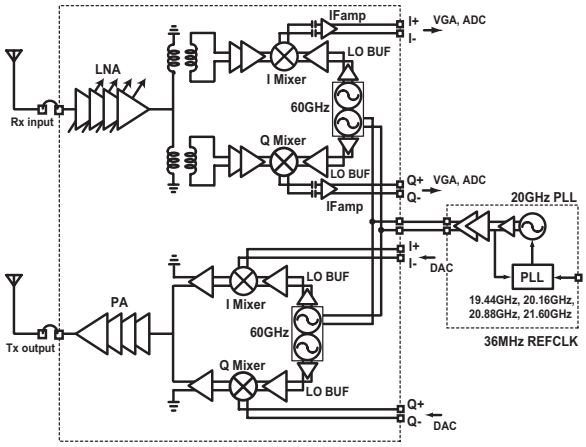

Fig. 1. Block diagram of the 60 GHz transceiver[1].

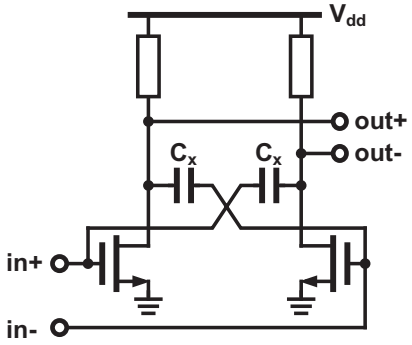

Fig. 2. Capacitive cross-coupling neutralization.

Fig. 2 shows the simplified differential circuit to explain the capacitive cross-coupling neutralization. It achieves a $-C$ by connecting the gate of one transistor and the drain of another transistor[2]. Moreover, refer to [3], the Maximum power gain (MAG), the Maximum stable gain (MSG) and the stability

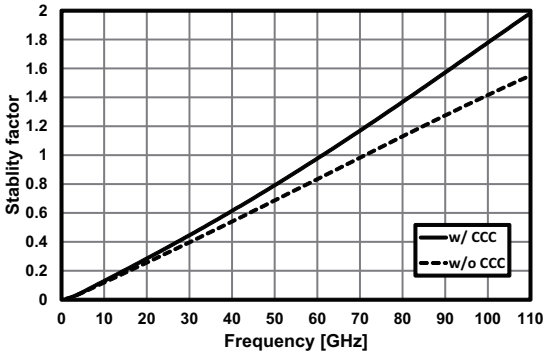

Fig. 3. Simulated stability factor.

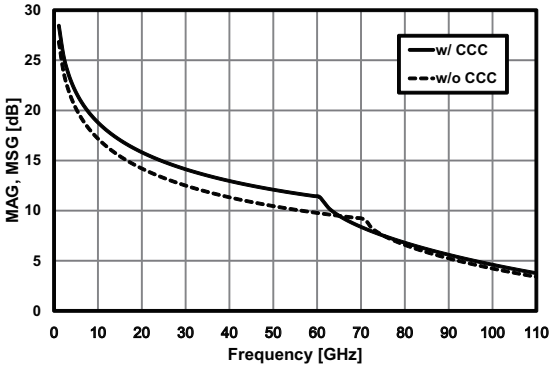

Fig. 4. Simulated maximum available gain.

factor (k) of Fig. 2 are given by Eqs.(1), (2), and (3). When the stability factor is less than one, the maximum stable gain is defined as the maximum available gain with k=1. According to Eqs. (1), (2), and (3), when $C_{\rm X}$ equals to $C_{\rm GD}$, these values are greatly improved. Furthermore, it is obvious that these values get worse when $C_{\rm GD}$ is increased.

$$k = \frac{2 + \omega^2 (C_{\rm GD} - C_{\rm x})^2 R_{\rm G} R_{\rm D}}{\omega |C_{\rm GD} - C_{\rm x}| R_{\rm G} R_{\rm D} \sqrt{\omega^2 (C_{\rm GD} - C_{\rm x})^2 + {g_{\rm m}}^2}}, \qquad (1)$$

$$MAG = \frac{\sqrt{\omega^2 (C_{\rm GD} - C_{\rm x})^2 + {g_{\rm m}}^2}}{\omega |C_{\rm GD} - C_{\rm x}|} (k - \sqrt{k^2 - 1}), \qquad (2)$$

$$MSG = \frac{\sqrt{\omega^2 (C_{\rm GD} - C_{\rm x})^2 + {g_{\rm m}}^2}}{\omega |C_{\rm GD} - C_{\rm x}|}. \qquad (3)$$

where $C_{\rm x}$ is the cross-coupled capacitance, $C_{\rm GD}$ is the gate-to-drain capacitance, $C_{\rm GS}$ is the gate-to-source capacitance, $C_{\rm DB}$ is the drain-to-bulk capacitance, $R_{\rm G}$ is the gate resistance, $R_{\rm D}$ is the drain resistance, and $g_{\rm m}$ is the transconductance.

Fig. 3 shows the simulated k, and Fig. 4 shows the MAG and MSG with or without capacitor cross-coupling. In these figures, it is obvious that these values are improved by using the technique of capacitor cross-coupling.

However the PAE using this topology depends on the value of cross-coupled capacitance. Fig. 5 shows the simulation result of the PAE when the size of cross-coupled capacitance and input power of differential PA are swept. This figure shows that PAE can be optimized by changing the value of cross-coupled capacitance depending on the input power.

III. Varactor Cross-Coupling Neutralization with Adaptive Bias

This paper proposes the circuit of varactor cross-coupling using adaptive bias depending on the input power. Fig. 6 shows the simulation result of adaptive bias voltage and the capacitance value of the varactor. Fig. 7 shows the schematic of varactor cross coupling PA. Moreover, Fig. 8 shows the schematic of adaptive bias. This differential power amplifier

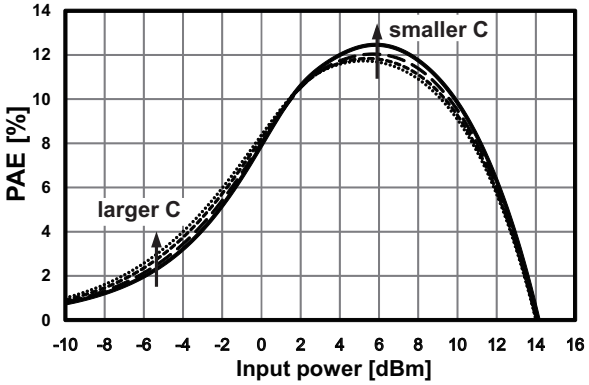

Fig. 5. The simulation result of PAE.

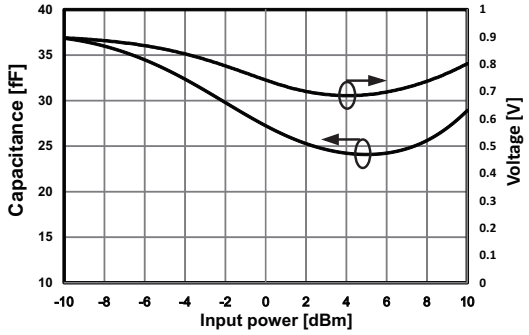

Fig. 6. The capacitance value of varactor and adaptive bias voltage.

consists of two amplifier stages. According to Fig. 6, it is obvious that the value of cross-coupled capacitance becomes smaller if the input power is over 2 dBm, and it becomes larger if the input power is under 2 dBm. Therefore, the PAE is optimized by using varactor and adaptive bias circuit.

It is essential to consider the circuit by using distributed constant not lumped constant at 60 GHz. Thus the guided micro-strip line, which is low-loss transmission line, is used. It has a loss of 0.8 dB/mm.

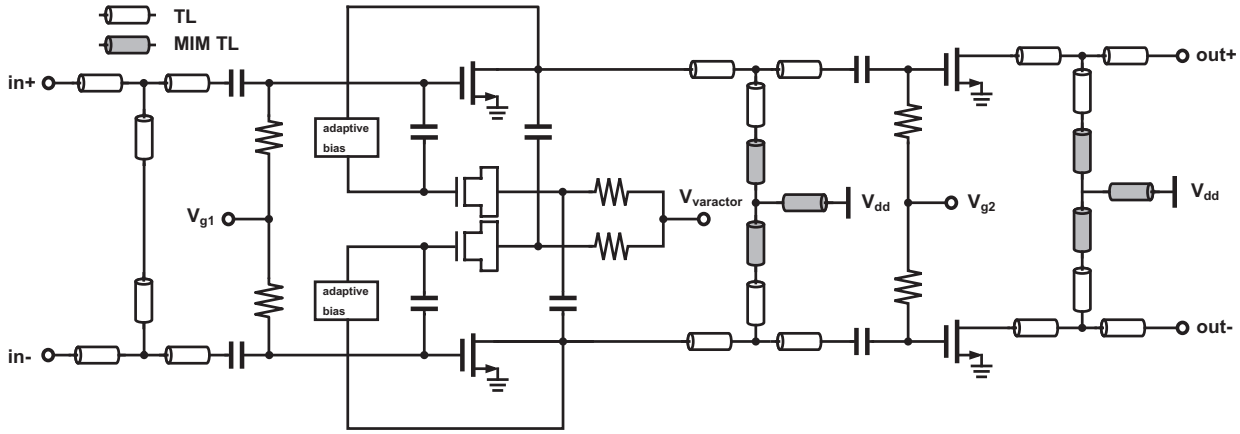

Fig. 7. The circuit of varactor cross-coupling power amplifier with adaptive bias.

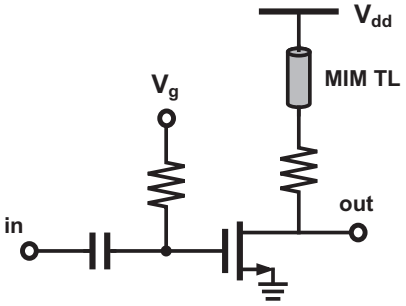

Fig. 8. The circuit of adaptive bias.

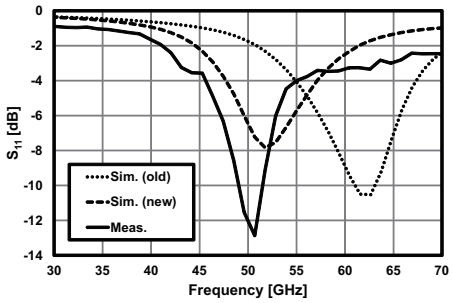

Fig. 9. Measurement result of S_{11}.

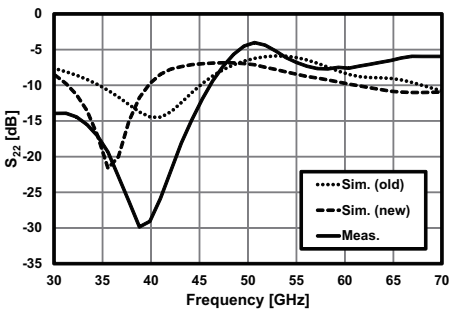

Fig. 10. Measurement result of S_{22}.

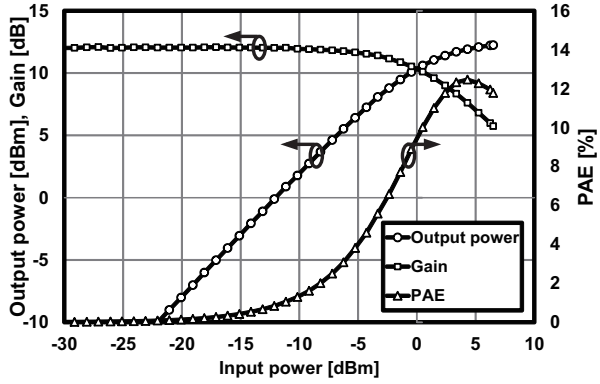

Fig. 11. Measurement result of large signal characteristic.

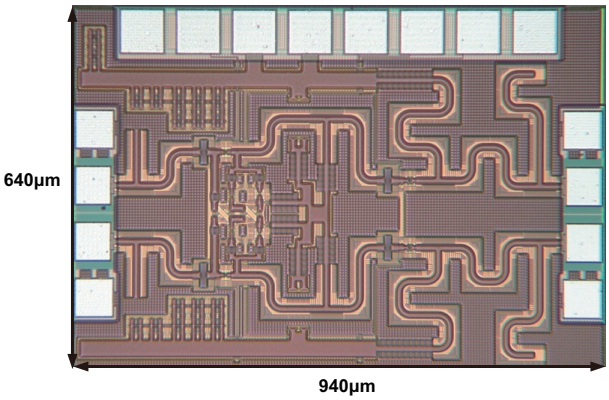

Fig. 12. Chip photograph.

The de-coupling is implemented by using MIM transmission line (MIM TL)[1]. The first stage is used the varactor cross-coupling neutralization and second stage is not. Transistors in the 2-stage PA have a finger width of 2 μm for a better power gain[4], and the total gate width of the final stage is 80 μm.

TABLE I
PERFORMANCE COMPARISON.

	Technology	Power Gain[dB]	P_{1dB}[dBm]	P_{sat}[dBm]	PAE@P_{1dB}[%]	Peak PAE[%]	Power[mW]	V_{DD}[V]
[2]	65 nm	16	2.5	11.5	4.5	11	43.5	1.0
[3]	65 nm	23.2	10.0	14.6	5	16.3	135	1.2
[5]	65 nm	19.2	15.1	17.7	7	11.1	480	1.0
[6]	65 nm	20.3	15	18.6	6.3	15.1	72	1.0
[7]	90 nm	8.3	8.2	10.6	-	5	228.6	1.2
[8]	90 nm	10	8.8	12.6	4	6.9	213	1.0
[9]	90 nm	4.4	12.1	14.2	5.7	5.8	145	1.0
[10]	90 nm	30	10.3	13.8	-	12.6	178	1.8
[11]	90 nm	20	8.2	12	4	9	146	1.2
[12]	90 nm	15.2	10	11	6.3	8.2	150	1.0
[13]	65 nm	5.5	9	12.3	6	8.8	-	1.0
[14]	65 nm	14.3	11	16.6	1.3	4.9	732	1.2
This Work	65 nm	12.1	9.5	12.2	**7.7**	12.5	86	1.2

IV. MEASUREMENT RESULT

Fig. 9 and Fig. 10 show the measurement results of small signal characteristic. In the simulation, this circuit is designed at 60 GHz. The result of "Sim. (old)" shows the characteristic. However the peak of the gain is shifted to about 50 GHz. This is because the accuracy of models which are used for simulation is not high. Thus, the models are updated after the measurement. The result of "Sim. (new)" which use updated models shows the characteristic. As a result, the difference of simulation and measurement is lower than before.

Fig. 11 shows the measurement result of output power, gain, and PAE. These are measured at 50 GHz to evaluate the effect of varactor cross-coupling neutralization due to the frequency shift. As shown in Fig. 11, the PAE at P_{1dB} is 7.7 % and the peak PAE is 12.5 %. The power consumption is 86 mW. Thus the effect of varactor cross-coupling neutralization with adaptive bias is validated.

Fig. 12 shows the chip photograph. The left pad is input side, and the right is output side. The chip area is $640\,\mu\text{m} \times 940\,\mu\text{m}$. Table I summarizes the performance comparison[2], [3], [5]-[14]. The proposed circuit achieves higher PAE at P_{1dB} than the other circuits and low power consumption.

V. CONCLUSION

In this work, the valactor is employed for the capacitive cross-coupled PA, and an adaptive bias is applied to the varactor depending on input power for improving PAE. As a result, the PAE at P_{1dB} can be improved, which is 7.7 % and the best performance in CMOS PAs.

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