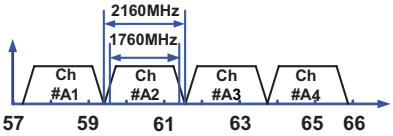
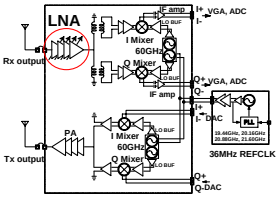
A Wideband LNA with an Excellent Gain Flatness for 60 GHz 16QAM Modulation in 65 nm CMOS

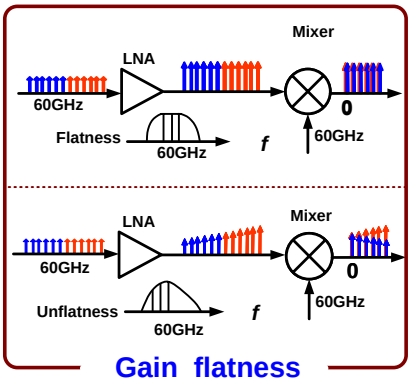
Qinghong Bu, Ning Li, Kenichi Okada and Akira Matsuzawa
Matsuzawa and Okada Laboratory, Tokyo Institute of Technology, Japan

1 Background

- IEEE 802.15.3c specification
  - 9 GHz unlicensed bandwidth
  - 2.16 GHz/ch
  - Several Gbps data transfer
    - QPSK ⇒ 3.5 Gbps • 16QAM ⇒ 7 Gbps





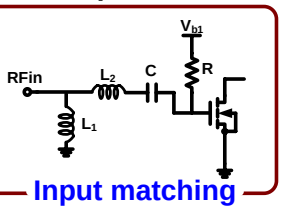


Gain flatness

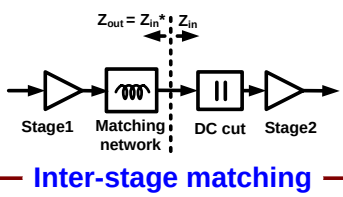
- Gain flatness is important in receivers
- Gain flatness influence the EVM of 16QAM modulation
- Gain degradation is requested less than 1dB in 16QAM modulation

2 LNA circuit design

- Consideration of LNA design
  - Multi-stage for high gain
  - Input matching for low noise
  - ESD protection
  - Inter-stage matching for gain flatness and low power loss

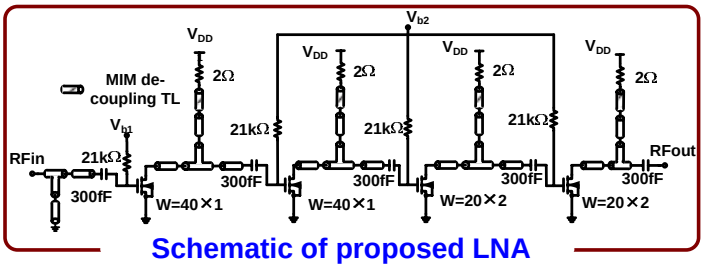


Input matching



Inter-stage matching

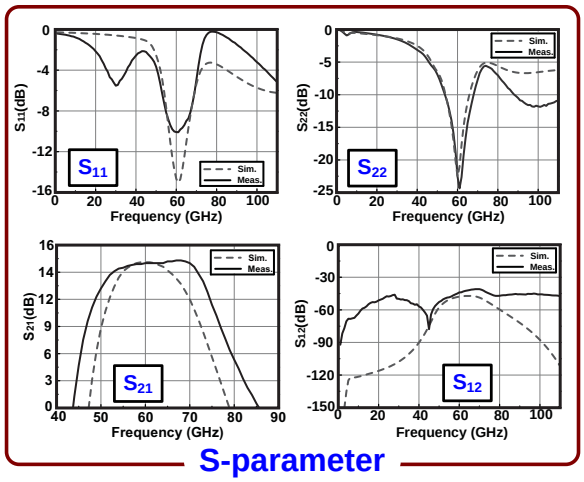
- W_f = 1μm (1st & 2nd stages) for noise opt.
- W_f = 2μm (3rd & 4th stages) for gain opt.
- Variable gain by adjusting bias voltages



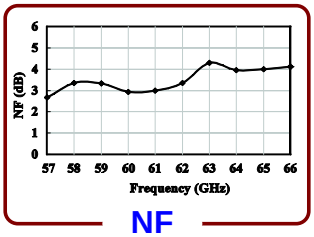
Schematic of proposed LNA

3 Measurement results

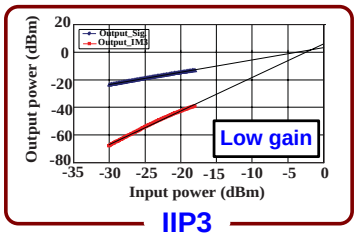
- Condition of measurement results
  - V_{DD} = 1.0 V • Power = 24 mW • V_{b1}/V_{b2} = 0.6 V



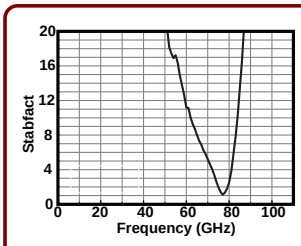
S-parameter



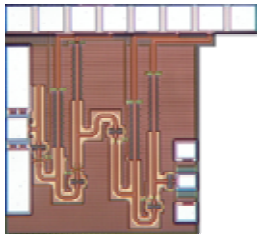
NF



IIP3



Stability



Chip photo

4 Conclusion

Reference	This work	[1] RFIC2008	[2] JSSC2007	[3] JSSC2008	[8] ESSCIRC2010	[10] JSSC2007	[11] VLSI2009
Technology	65nm CMOS	90nm CMOS	90nm CMOS	90nm CMOS	65nm CMOS	90nm CMOS	90nm CMOS
Topology	CS	CS	Cas.	Cas.	CS	CS	Cas
Stage	4	3	2	2	4	2	3
f_{center} [GHz]	68	58	58	64	53	63	63
BW [GHz]	23	5	6	8	17	-	14
Gain [dB]	17.5	15	14.6	15.5	24	12.2	24
NF [dB]	<4.3	4.4	5.5	6.5	4	6.5	6.8
Power [mW]	24	3.9	24	86	30	10.5	36

- Wideband four-stage LNA with excellent gain flatness
  - 3-dB bandwidth: 23 GHz
  - Variable gain: 6.3 dB to 17.5 dB
  - IIP3: -1.8 dBm
  - NF: < 4.3 dB