

A 0.8-1.8 GHz Wideband Low Noise Amplifier with Capacitive Feedback

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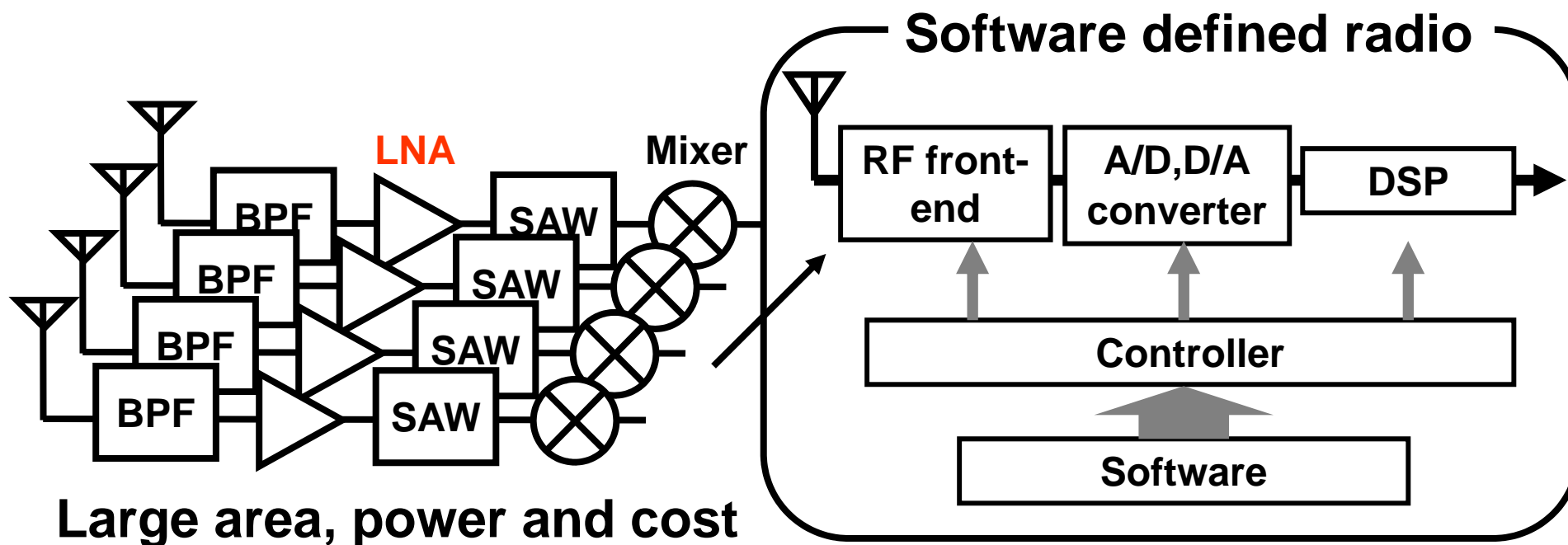
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- **Conventional common-gate topologies**
- **Proposed LNA**
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- **Conclusion**

Necessity of multi standard

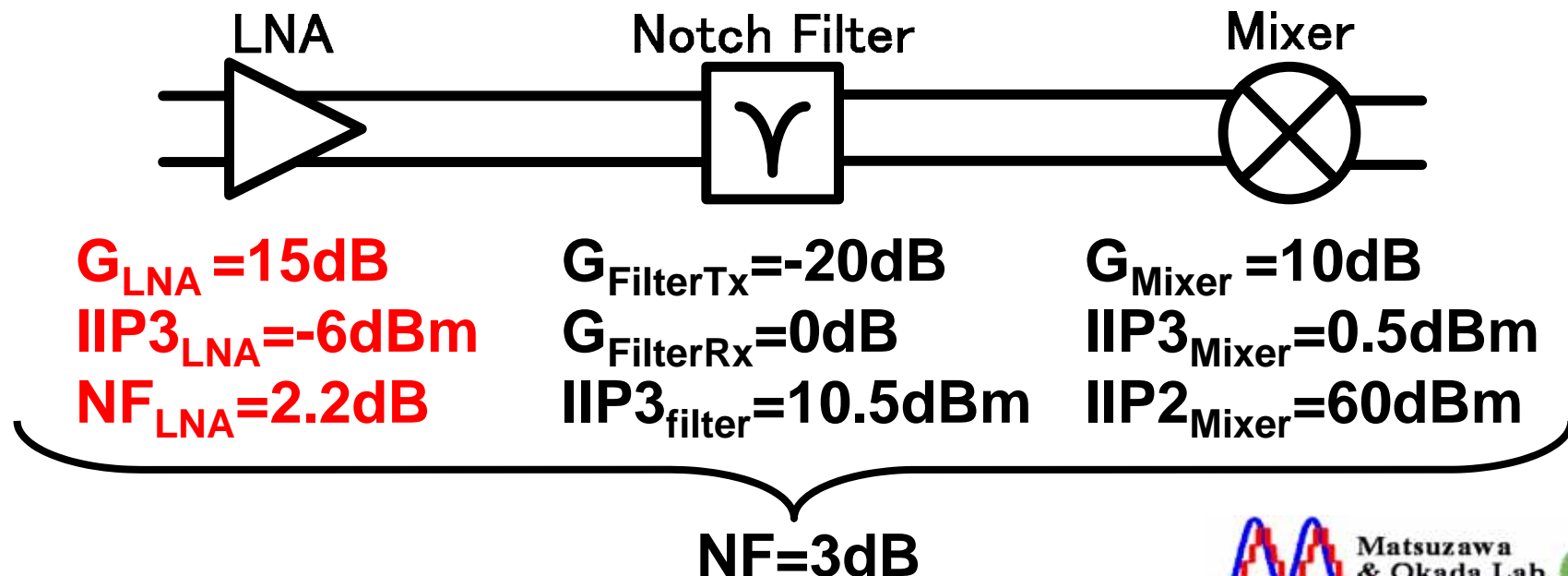
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- Several RFICs are required for each wireless communication standard.
- To improve this situation, SDR is proposed.



Requirements for SAW-less receiver / 3

- Assuming that on chip notch filter is used instead of SAW filters.
- When Tx leak=-30dBm and CW blocker=-60dBm, requirements for components are calculated as follows.



Topology of LNAs

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- **Resistive feedback LNA**
 - High gain, low noise
 - Large power
- **Common-gate LNA**
 - High linearity, low power
 - Lower gain, higher noise than resistive feedback LNA

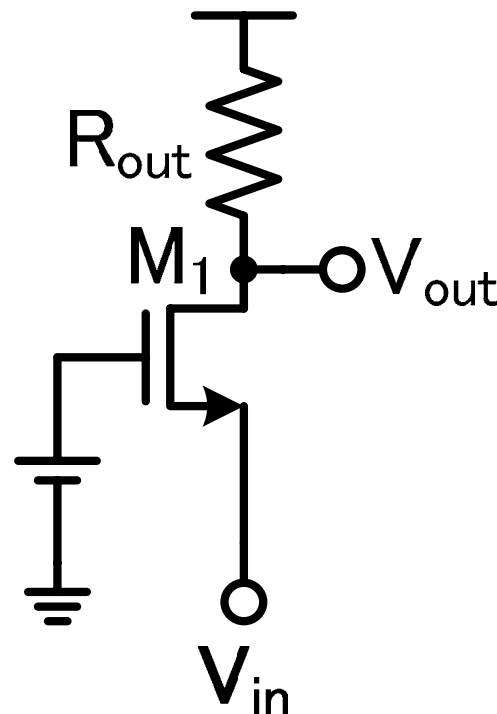
Common-gate topology is employed.

Fundamental common-gate LNA

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- g_m of the common-gate transistor is fixed due to the input impedance matching.
- NF cannot be improved due to fixed g_m .



$$Z_{in} = \frac{1}{g_m} = R_S$$

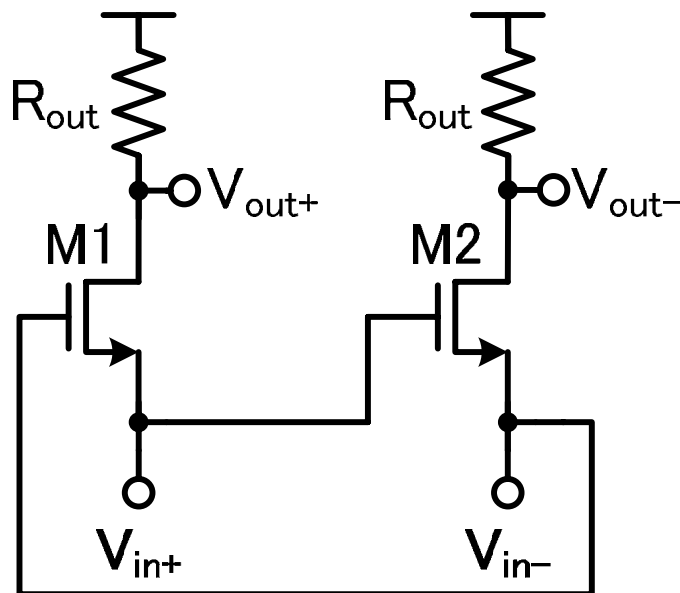
$$F = 1 + \gamma + \frac{4R_S}{R_{out}} = 2.8\text{dB}$$

Capacitive-Cross-Couple LNA

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- This topology achieves a lower noise factor than that of fundamental one.
- However, g_m and noise of common-gate transistor are still fixed.



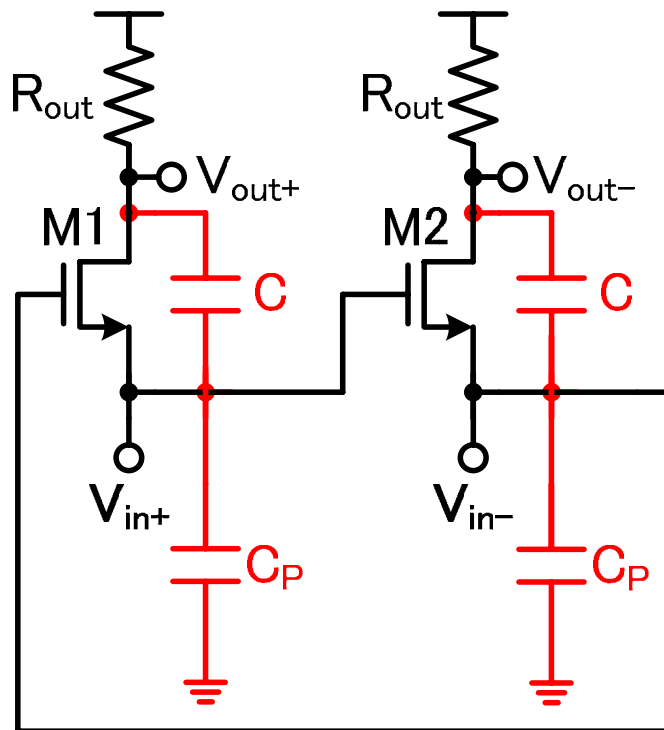
$$Z_{in} = \frac{1}{2g_m} = R_S$$

$$F = 1 + \frac{\gamma}{2} + \frac{4R_S}{R_{out}} = 1.93\text{dB}$$

[1] W. Zhuo, et al. ESSCIRC, 2000.

Proposed topology

- The proposed LNA employs capacitive-cross-couple technique and **capacitive feedback**.
- g_m can be enlarged, NF can be improved.

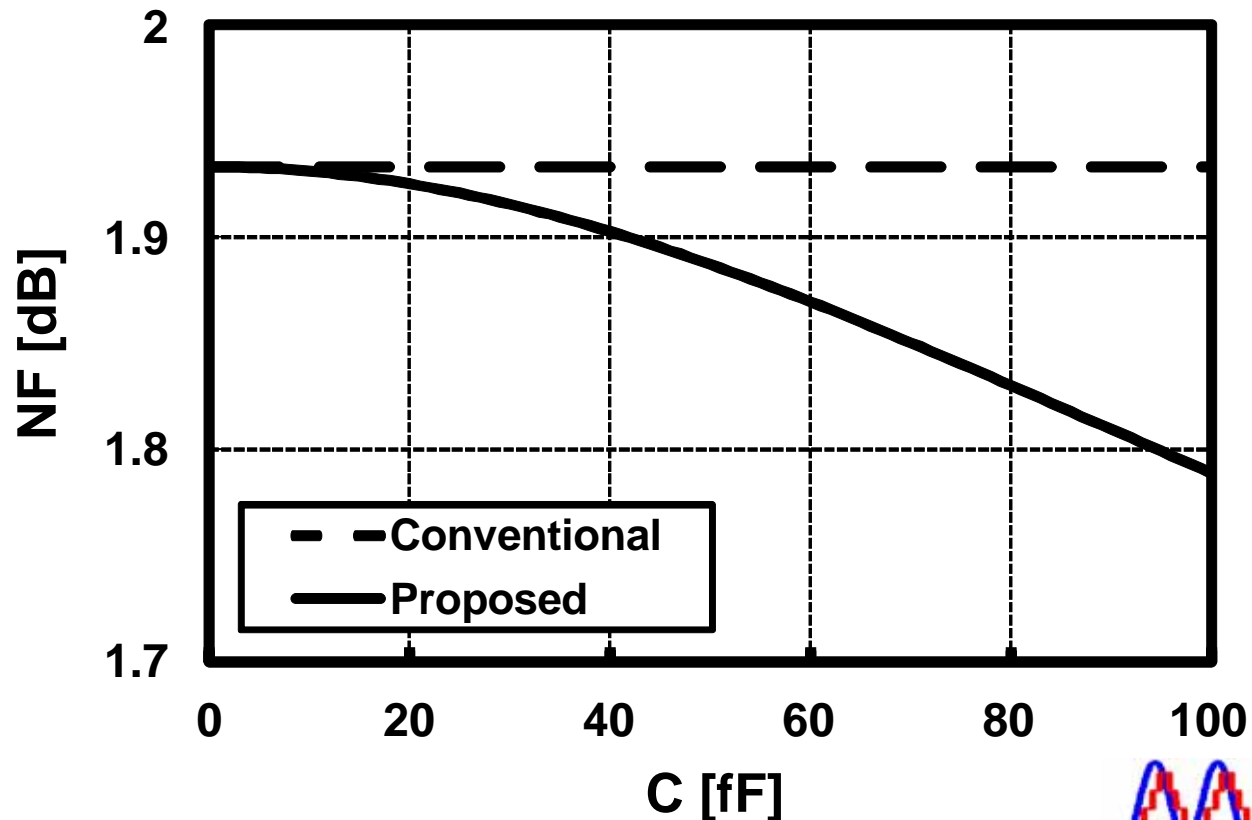


$$\text{Re}(Z_{in}) = \frac{1 + \omega^2 C^2 R_{out}^2}{2g_m} = R_S$$

$$F = 1 + \frac{\gamma}{2 + \frac{\omega^2 C^2 R_S^2}{(1 + \omega^2 C^2 R_{out}^2)}} + \frac{R_S (2 + \omega^2 C^2 R_{out}^2)^2 + \omega^2 C^2 R_S (R_S + R_{out})^2}{R_{out} \left((1 + \omega^2 C^2 R_{out}^2)^2 + \omega^2 C^2 R_S^2 \right)}$$

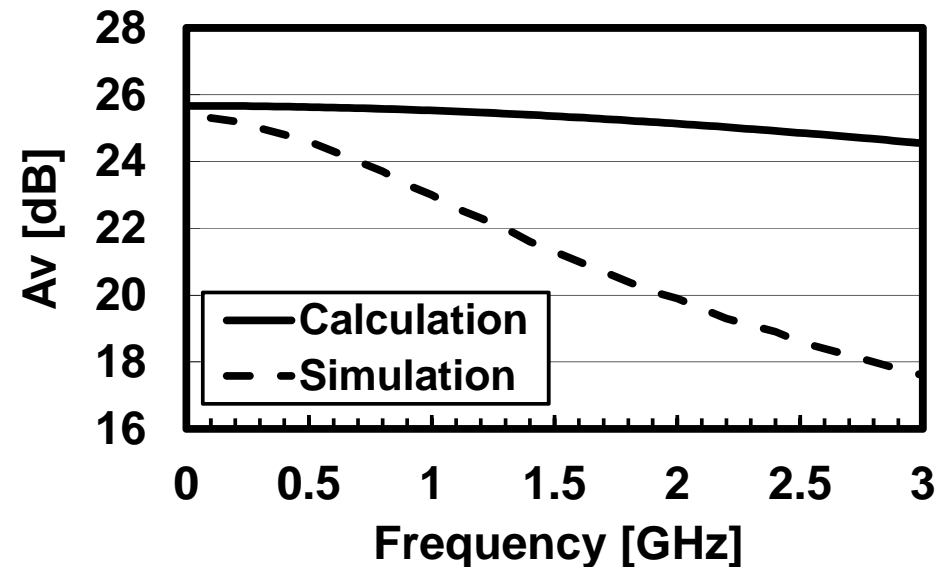
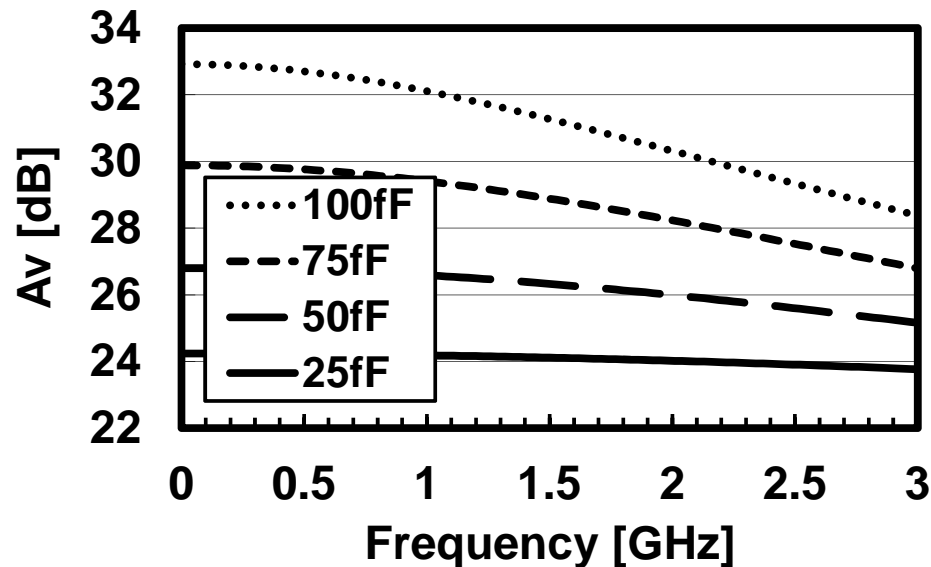
Noise calculation

- Calculated NFs of CCC LNA and capacitive feedback LNA are compared.
- The larger C is, the lower NF is.



Voltage gain

- The larger C is, the larger but less flatness of voltage gain is.
- Simulated result is less flat than calculated one.

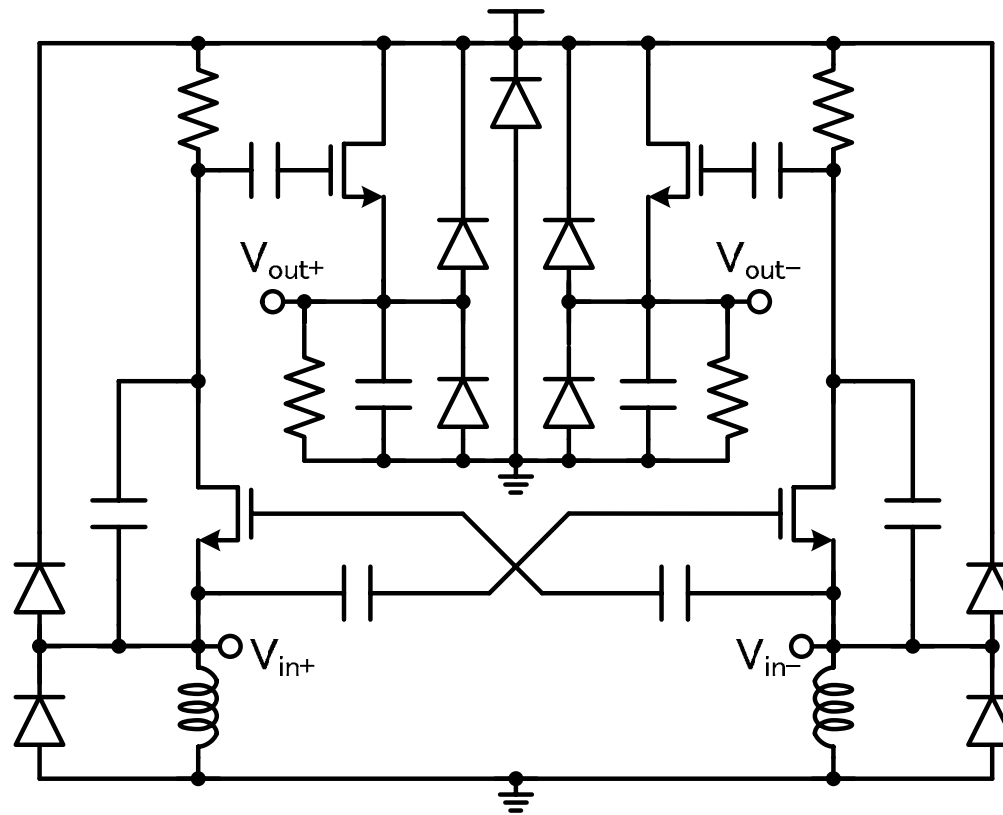


LNA schematic including buffer

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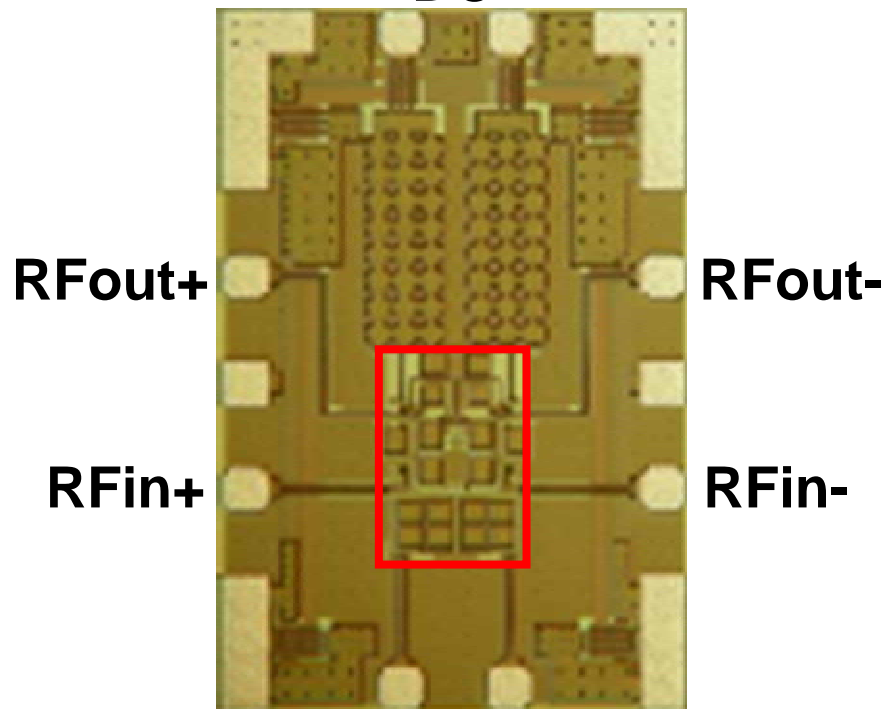
- External chip inductors are used.
- C_p is implemented by ESD diode.
- The source follower buffer is connected



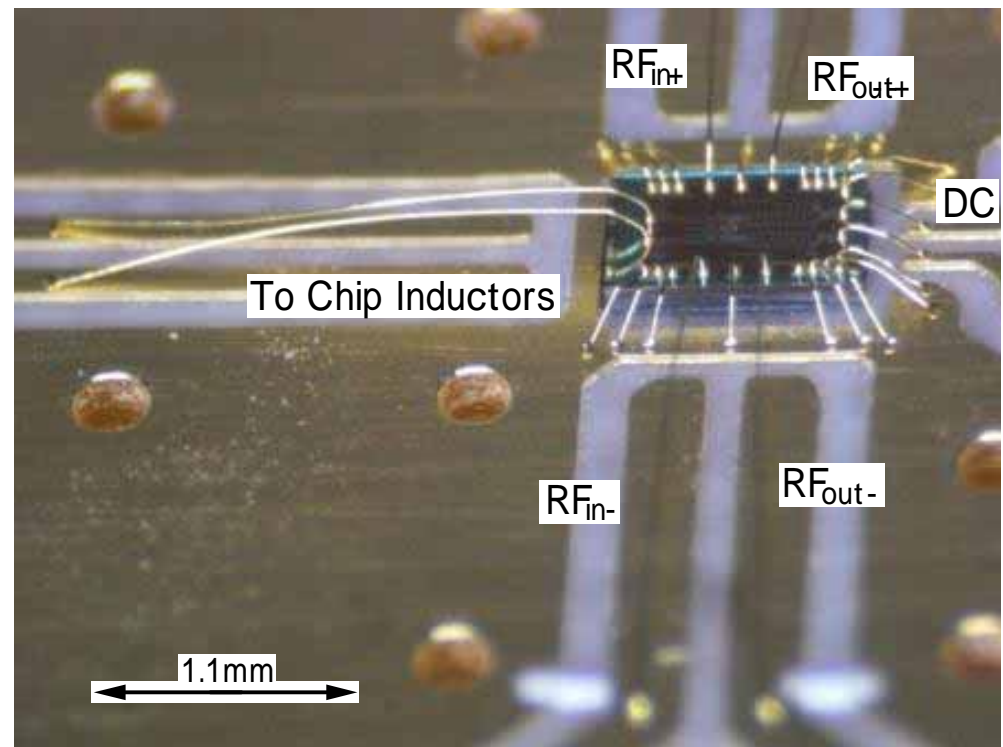
Chip and PCB photo

- Nodes of photographs below correspond to each other.
- Core size is 0.066mm^2

DC



To chip inductors

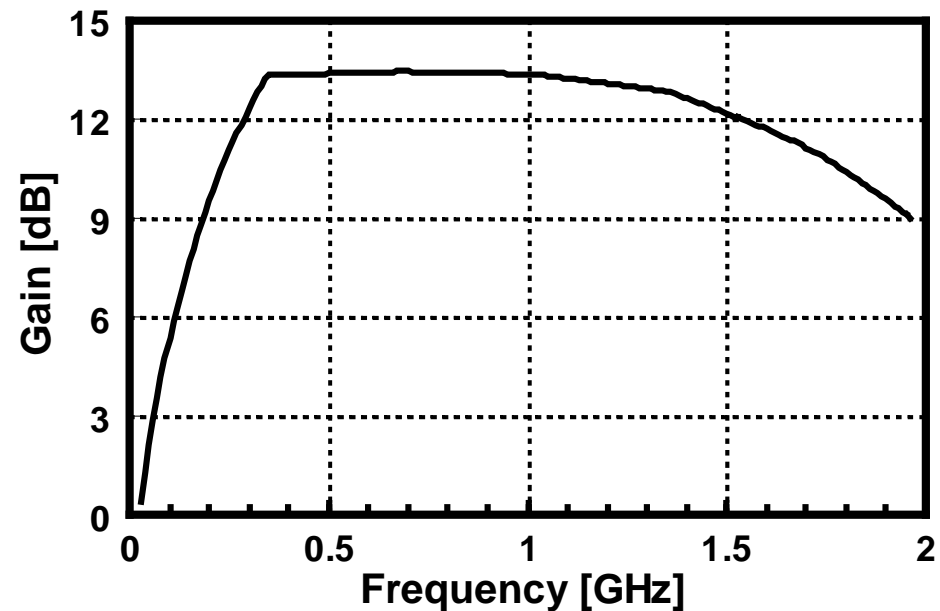
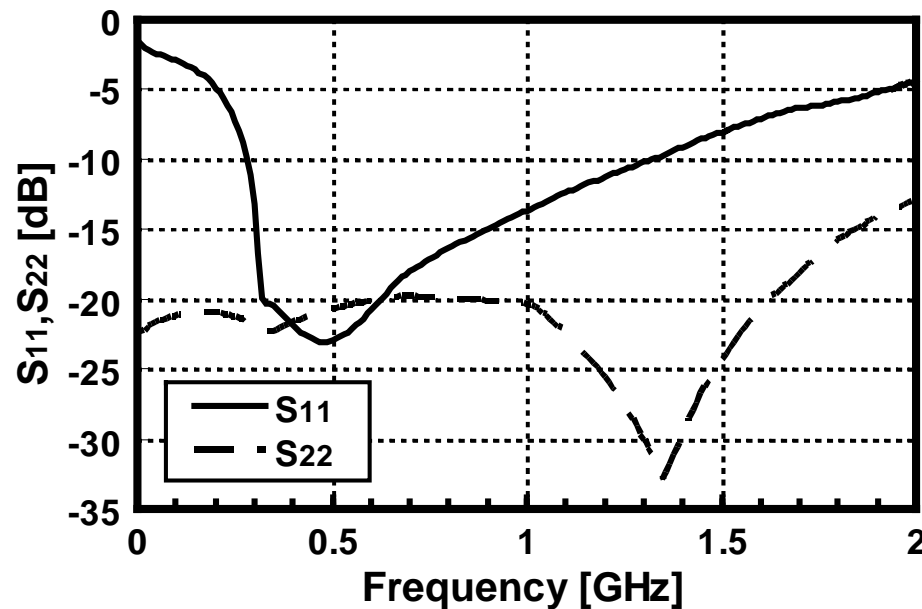


Measured S parameters

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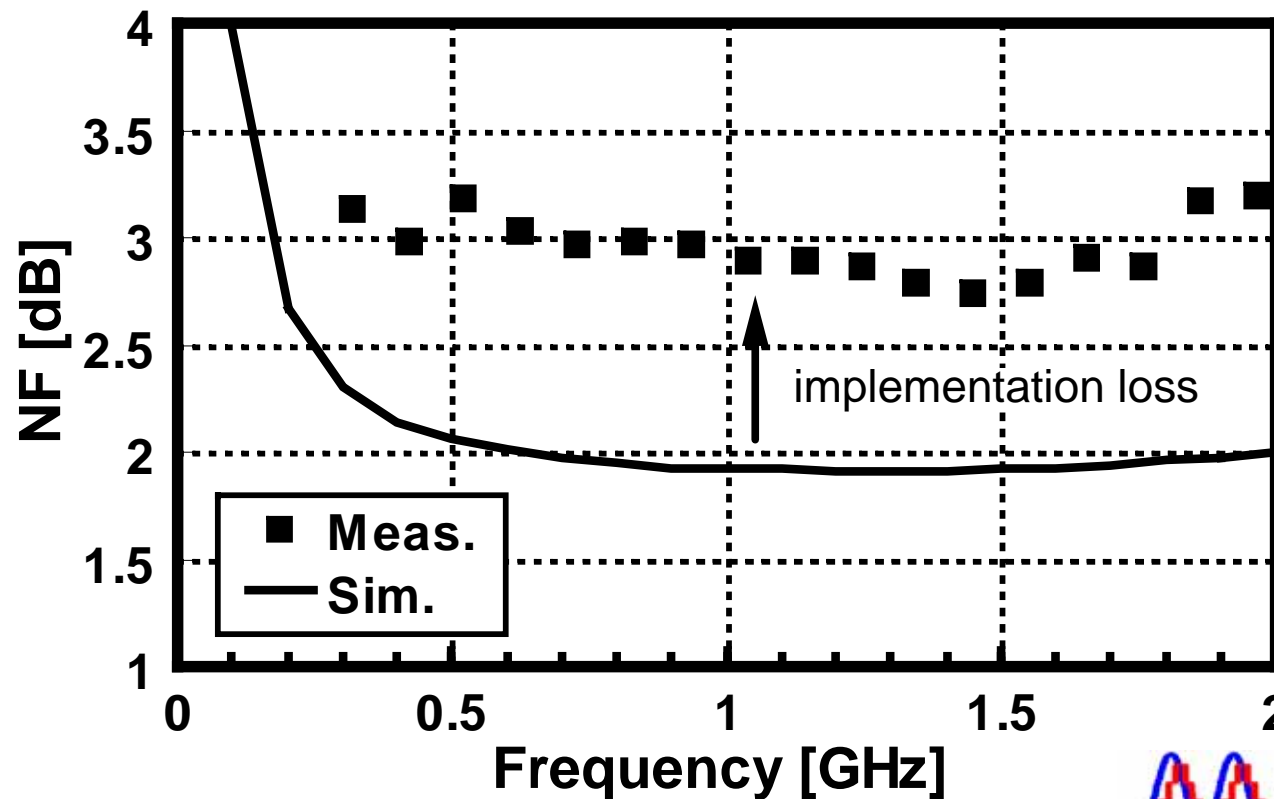
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- $S_{11} < -5\text{dB}$ and $S_{22} < -10\text{dB}$ @ 0.8-1.8GHz
- Maximum power gain is 13.4dB.
- These are calculated from 4-port S-para.

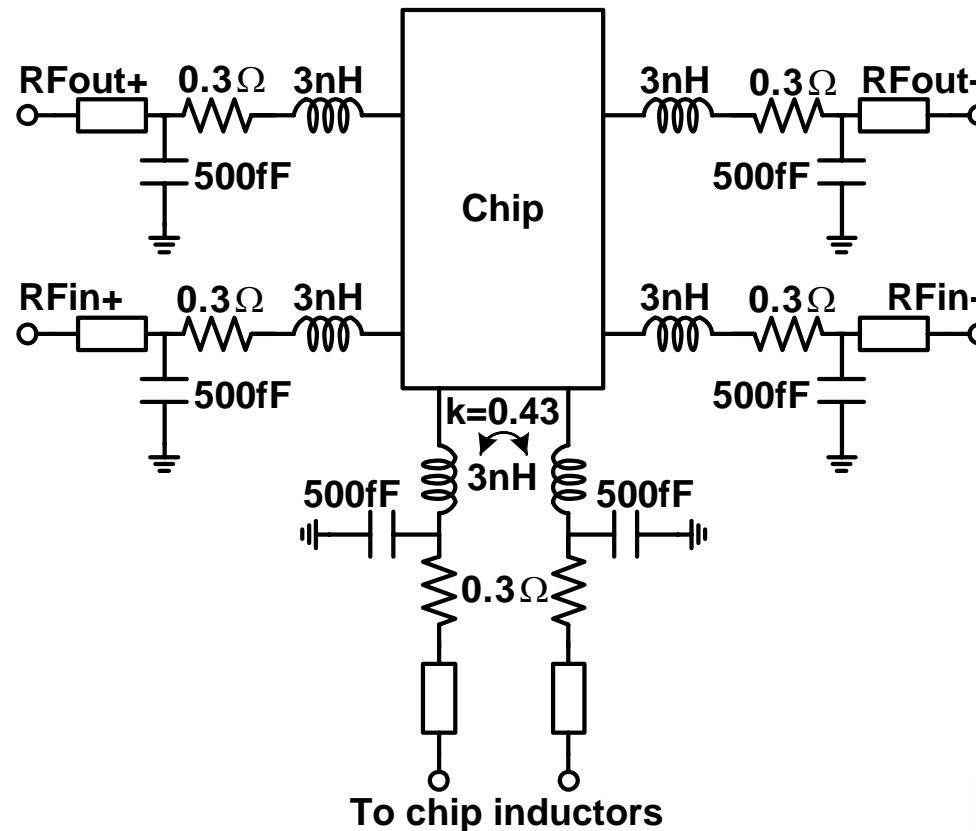


Measured NF

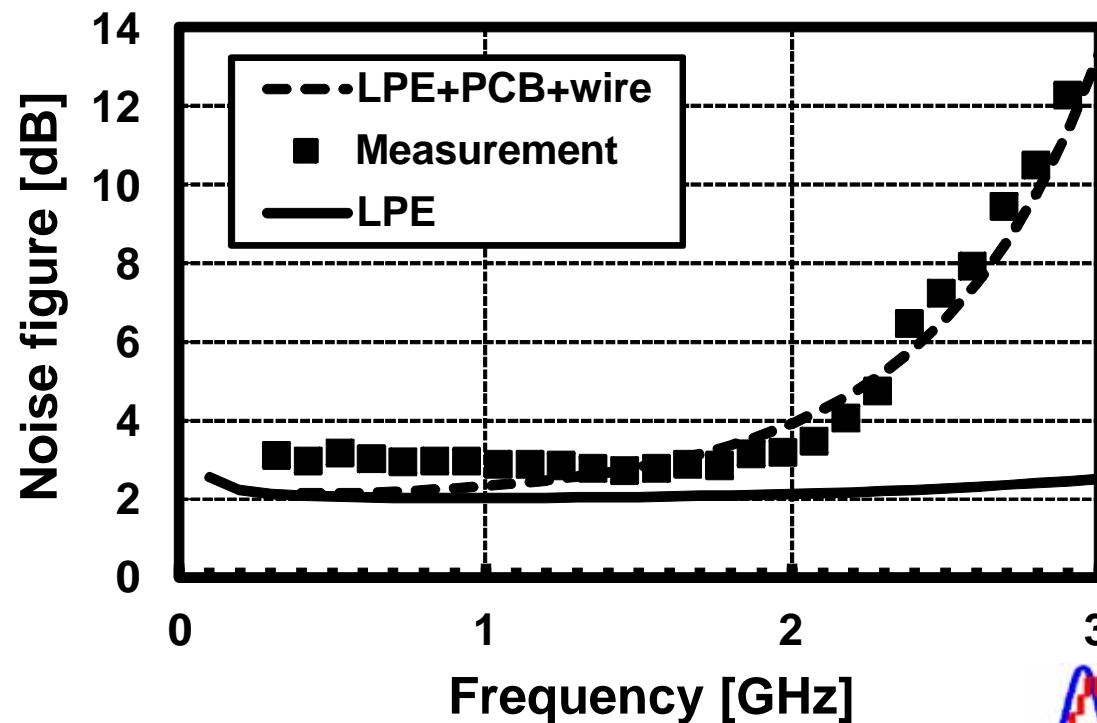
- Measured NF is 2.7dB.
- This result is much higher than simulated one.



- Transmission line of PCB and parasitic of bonding wire model is made.
- Inductor coupling is also considered.



- Measured and simulated with parasitic model NFs are compared.
- Simulation result using parasitic model is similar to the measured result.



- **Simulation results achieve targets and NF is lower than 2dB.**
- **Measured results can be improved in consideration with the parasitics.**

	Goal	This work	[2]
Freq. [GHz]	0.8-2.6	0.8-1.8	0.3-0.92
Gain [dB]	15	13.4	21
NF [dB]	2.2	2.7	2
IIP3 [dBm]	-6	-7	-3.2
P_{dc} [mW]	-	6.5	3.6

[2]S.Woo, et al. ISSCC 2009

- The wideband low noise amplifier with capacitive feedback is proposed.
- The capacitive feedback adds more flexibility in g_m and NF can be theoretically improved.
- Measured and simulated NFs are much different from each other.
- That can be improved in consideration with the parasitic components.

Thank you for your attention!