

A 0.8-1.8 GHz Wideband Low Noise Amplifier with Capacitive Feedback

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Abstract—This paper proposes a wideband common-gate LNA using capacitive feedback. The transconductance of the proposed LNA can be enlarged and noise figure can be improved while the conventional common-gate LNA has to use a smaller transconductance for the input impedance matching. In the experimental results using a 0.18- μm CMOS technology, the gain is 13.4 dB, NF is 2.7 dB, IIP3 is -7 dBm at 0.8 GHz, and the power consumption is 6.5 mW with a 1.8-V supply voltage.

Index Terms—LNA, CMOS, Wideband.

I. INTRODUCTION

Wireless communication systems have been developed for various consumer applications, *e.g.*, GSM/UMTS/LTE, WiFi, Bluetooth, GPS, and so on. Recently, a multi-standard RFIC is required to save footprint size in mobile terminals. To cover present wireless systems, several RFICs are required for each wireless standard, which causes increasing in total chip area, power consumption, and cost. To improve this situation, the software defined radio (SDR) is proposed in [1]. The multi-standard RF front-end for every frequency bands is needed to realize the SDR. In the multi-standard RF front-end, high performance wideband LNA is indispensable. However, it is difficult to achieve that, because there are trade-offs between some parameters, for example gain, noise, linearity, and power consumption. The LNA in [2] achieves wideband characteristics by using resistive feedback. It realizes high gain and low noise, while it consumes larger current. The LNA in [3] employs common-gate topology. This realizes low power consumption, but NF is relatively high. In this paper, low noise common-gate LNA by using capacitive feedback is proposed.

II. COMMON-GATE LNA CALCULATION

In this section, input impedance and noise factor of common-gate LNAs are analyzed.

A. Fundamental Common-Gate LNA

Fig.1(a) shows the most basic topology in common-gate LNAs. The input impedance and noise factor of this LNA can be calculated as follows:

$$Z_{in} = \frac{1}{g_m} = R_S \quad (1)$$

$$F = 1 + \gamma \quad (2)$$

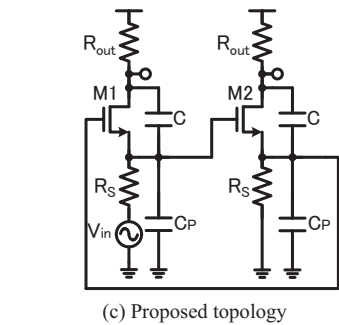
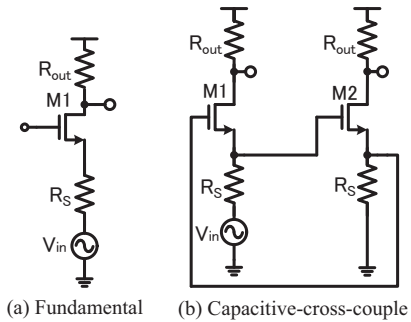


Fig. 1. The conventional and proposed common-gate topologies.

where g_m and γ are the transconductance of M1 and the channel thermal noise coefficient, respectively. g_m and noise of the common-gate transistor are fixed due to the 50Ω input impedance matching, so these parameters cannot be improved any more in the conventional common-gate topologies.

B. Capacitive-Cross-Couple LNA

Fig.1(b) shows the capacitive-cross-couple LNA proposed in [4]. Capacitive-cross-couple technique contributes to improve the noise of input stage. The input impedance and noise factor of this LNA can be calculated as follows:

$$Z_{in} = \frac{1}{2g_m} = R_S \quad (3)$$

$$F = 1 + \frac{\gamma}{4g_m R_S} + \frac{(1 + 2g_m R_S)^2}{4g_m^2 R_S R_{out}} \quad (4)$$

where g_m is the transconductance of M1 and M2. By using Eqs.(3) and (4), noise factor can be expressed as follows.

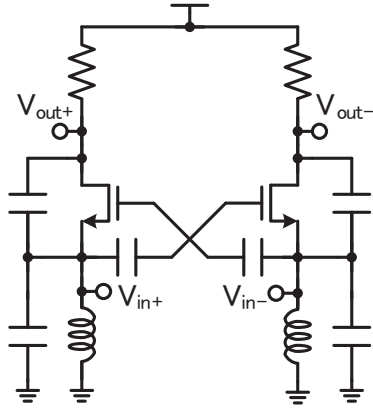


Fig. 2. The proposed LNA schematic.

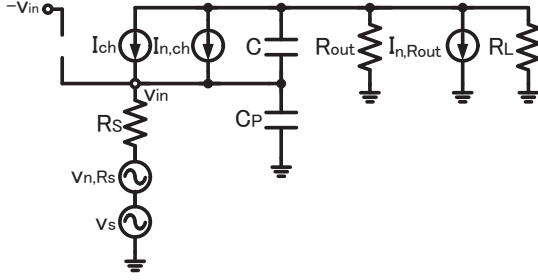


Fig. 3. Small signal equivalent circuit of the proposed LNA.

$$F = 1 + \frac{\gamma}{2} + \frac{4R_S}{R_{out}} \quad (5)$$

Thus, capacitive-cross-couple topology achieves a lower noise factor than that of Fig.1(a). However, g_m and noise of common-gate transistor are still fixed, these parameters cannot be improved.

III. PROPOSED LNA

In this section, some trade-offs of the proposed LNA are shown. The proposed LNA employs capacitive-cross-couple technique and capacitive feedback. Fig.2 shows the schematic of the proposed LNA.

A. Input Impedance

According to Fig.1(c), the input impedance of the proposed LNA can be calculated as follows:

$$Z_{in} = \frac{2g_m + \omega^2 C^2 R_{out} + j\omega(2Cg_m R_{out} - \omega^2 C^2 C_P R_{out}^2 - C_t)}{(2g_m - \omega^2 C C_P R_{out})^2 + \omega^2 C_t^2} \quad (6)$$

where g_m and ω are the transconductance of M1 and M2 and $2\pi f$, respectively. In order to simplify the calculation, the following expressions are used.

$$C_t = C + C_P \quad (7)$$

$$2g_m R_{out} \gg 1 \quad (8)$$

The following condition for C_P has to be satisfied to make the imaginary part of Z_{in} zero.

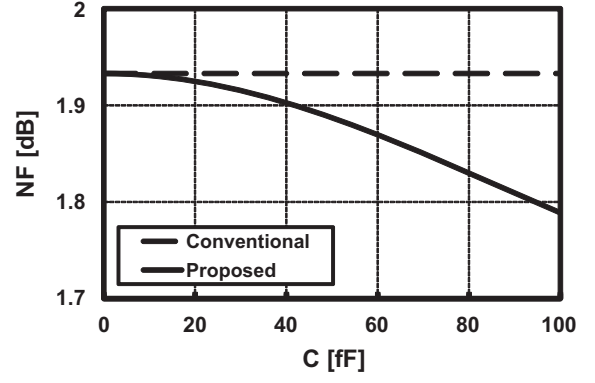


Fig. 4. Calculated NF plotted versus C.

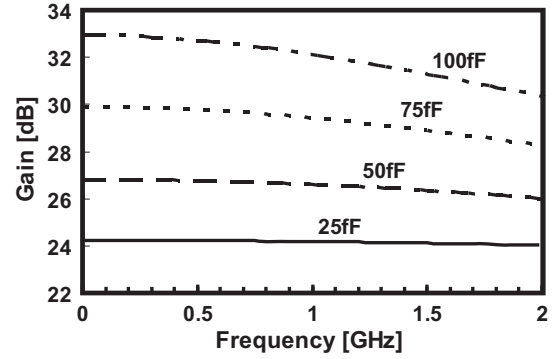


Fig. 5. Calculated gain plotted versus C.

$$C_P = \frac{2Cg_m R_{out}}{1 + \omega^2 C^2 R_{out}^2} \quad (9)$$

By Eqs.(6) and (9), the real part of Z_{in} can be calculated as follows:

$$\text{Re}(Z_{in}) = \frac{1 + \omega^2 C^2 R_{out}^2}{2g_m} = R_S \quad (10)$$

In order to simplify the calculation, the approximate expression below is used.

$$2g_m \gg \omega^2 C^2 R_{out} \quad (11)$$

Eq.(10) shows that capacitive feedback adds more flexibility of g_m , and the noise performance can be improved by using larger g_m .

B. Noise Figure

By using Fig.3, the noise factor of the proposed LNA can be calculated as follows:

$$F = 1 + \frac{\gamma g_m (1 + \omega^2 C_P^2 R_S^2)}{R_S (4g_m^2 + \omega^2 C^2)} + \frac{(1 + 2g_m R_S)^2 + \omega^2 (C + C_P)^2 R_S^2}{R_S R_{out} (4g_m^2 + \omega^2 C^2)} \quad (12)$$

where v_{n,R_s} , $I_{n,ch}$ and $I_{n,Rout}$ in Fig.3 are the noise of R_S , M1 and R_{out} respectively. By substituting Eq.(9) and Eq.(10) to Eq.(12), noise factor can be calculated as follows:

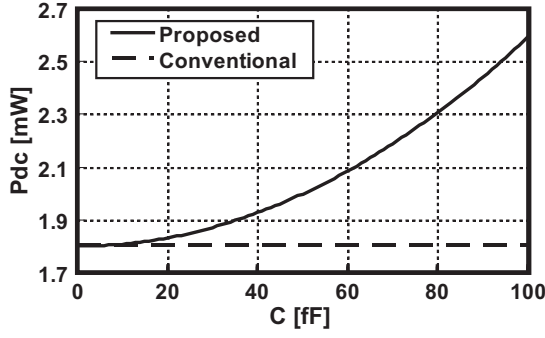


Fig. 6. Calculated P_{dc} plotted versus C .

$$F = 1 + \frac{\gamma}{2 + \frac{\omega^2 C^2 R_S^2}{(1 + \omega^2 C^2 R_{out}^2)^2}} + \frac{R_S(2 + \omega^2 C^2 R_{out}^2)^2 + \omega^2 C^2 R_S(R_S + R_{out})^2}{R_{out}((1 + \omega^2 C^2 R_{out}^2)^2 + \omega^2 C^2 R_S^2)} \quad (13)$$

NF is plotted versus C in Fig.4, where $R_S=50\Omega$, $R_{out}=880\Omega$, $\gamma=2/3$ and $f=1.2$ GHz. The larger C is, the lower noise factor is. By Eq.(13), NF is saturated around 1.5dB at $C=400$ fF. Actually, the value of C used for the proposed LNA in this paper is 36 fF.

C. Voltage Gain

By using a half equivalent circuit shown in Fig.3, voltage gain can be calculated as follows:

$$A_V = \frac{(2g_m + j\omega C)(R_{out} // R_L)}{1 + j\omega C(R_{out} // R_L)} \quad (14)$$

where R_L is the input impedance of mixer. Fig.5 shows the frequency characteristic of voltage gain where $R_L=4$ k Ω . Fig.5 means that the larger C is, the larger but less flatness of voltage gain is.

D. Power Consumption

A drain-source current of a transistor can be expressed as follows:

$$I_{ds} = \frac{g_m(V_{gs} - V_{th})}{2} \quad (15)$$

By using Eq.(15), the power consumption of single side of the proposed LNA can be calculated as follows:

$$P_{dc} = V_{dd}I_{ds} = \frac{g_m V_{dd}(V_{gs} - V_{th})}{2} \quad (16)$$

where g_m , V_{gs} and V_{th} is the transconductance, gate-source voltage and threshold of common-gate transistor at the input.

Eqs.(10) and (16) shows that the larger C is, the larger power consumption is. Fig.6 shows the power consumption as a function of C in Fig.6, where $V_{dd}=1.8$ V, $V_{gs}=0.6$ V and $V_{th}=0.4$ V. Eqs.(13), (14) and (16) show that there are trade-offs between noise, gain flatness and power consumption.

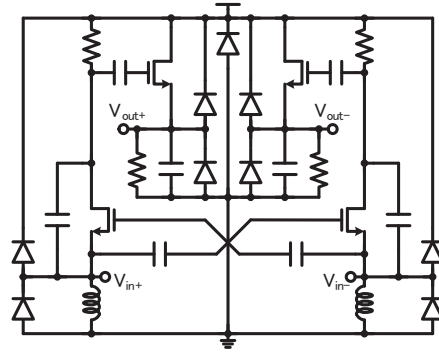


Fig. 7. The proposed LNA schematic including ESD diode.

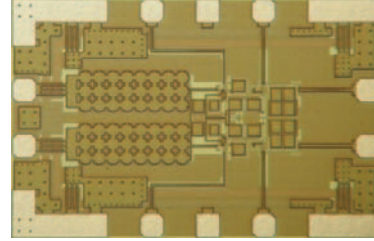


Fig. 8. Chip photograph.

IV. EXPERIMENTAL RESULTS

The proposed LNA schematic with ESD protection is shown in Fig. 7. External chip inductors are used as choke inductors, and C_P is implemented by ESD diode. Fig. 8 shows the die photograph of the wideband LNA. This chip is implemented by 0.18- μ m CMOS process and occupies a chip area of 0.066 mm². The measured results of S_{11} and S_{22} of the LNA are shown in Fig. 9. The measured gain and NF are given in Fig. 10 and Fig. 11, respectively. The noise figure is much lower performance than the simulation results because of the implementation loss. Fig 12 shows the output power and IM3 as a function of input power at 0.8 GHz. In the measured results, IIP3 is -7 dBm at 0.8 GHz. The power consumption is 6.5 mW. Table I shows a performance comparison among wideband low noise amplifiers.

V. CONCLUSION

In this paper, the wideband low noise amplifier with capacitive feedback is proposed to achieve a multi-band receiver. The capacitive feedback adds more flexibility in g_m and NF can be theoretically improved. The LNA realizes a 13.4 dB gain, 2.7 dB NF and -7 dBm IIP3.

ACKNOWLEDGMENT

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TABLE I
PERFORMANCE COMPARISON BETWEEN WIDEBAND LNAs.

	This Work	[2]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]
CMOS Tech	0.18 μ m	0.25 μ m	90nm	0.18 μ m	0.18 μ m	0.13 μ m	0.13 μ m	0.18 μ m	0.13 μ m	90nm	65nm
Freq. [GHz]	0.8-1.8	0.002-1.6	1.6-28	0.11-11	2-4.6	3.1-10.6	0.8-2.1	0.3-0.92	1-7	0-6	0.1-4
Gain [dB]	13.4	13.7	10.7	9.71	9.8	16.5	14.5	21	17	17.4	24
NF [dB]	2.7 (1.9*)	2.4	2.92	2.78	2.3	2.1	2.6	2	2.7	2.5	2
IIP3 [dBm]	-7	0	4	-3.5	-7	-5.1	16	-3.2	-4.1	-8	-5.5
Pdc [mW]	6.5	35	21.6	21.6	12.6	9	17.4	3.6	25	9.8	12

*simulation

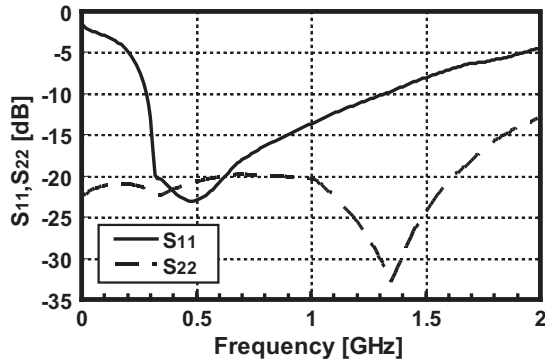


Fig. 9. Measured S_{11} and S_{22} .

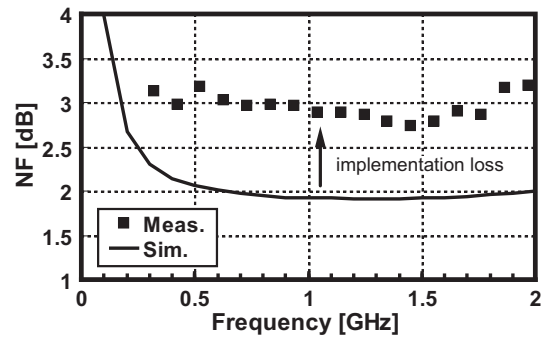


Fig. 11. Measured NF.

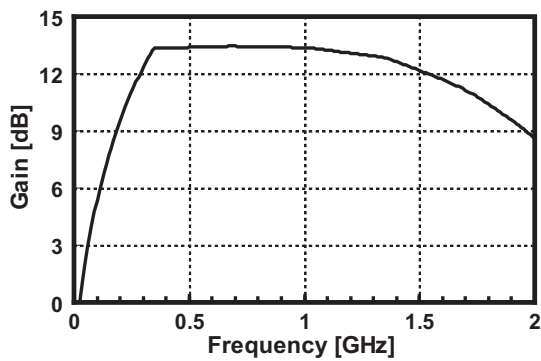


Fig. 10. Measured gain.

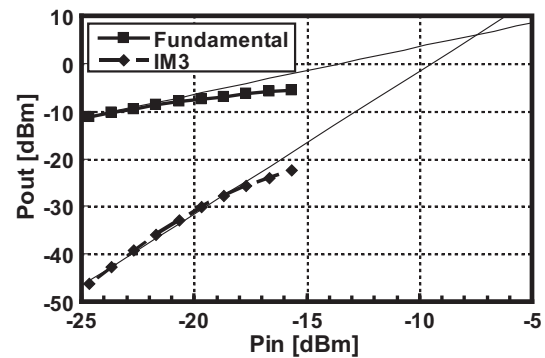


Fig. 12. Measured IM3 at 0.8 GHz.

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