A Wideband LNA with an Excellent Gain Flatness for 60 GHz 16QAM Modulation in 65 nm CMOS

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***Abstract* — In 60 GHz radios, at least 9 GHz flat gain is needed for the whole band for 16-QAM modulation. A 23 GHz 3 dB bandwidth, 6.3 dB to 17.5 dB variable gain, less than 4.3 dB NF, -7.7 dBm IIP3, four-stage common source LNA is proposed in this paper. The LNA uses guided micro-strip transmission line to realize simple input and inter-stage impedance matching networks. The prototype LNA is implemented in 65 nm CMOS with a chip area of 0.354 mm^2 including RF pad.**

***Index Terms* — LNA, variable-gain, 60 GHz, gain flatness.**

I. INTRODUCTION

60 GHz radios have a variety of applications, such as wireless local area networks (WLANs) with extraordinary capacity and short-range high data-rate wireless personal area networks (WPANs). Because of the 9GHz band from 57 GHz to 66 GHz is license free, it is very attractive to both academia and industry [1-6]. Multi-Gbps wireless communication of 60 GHz transceivers have been reported recently [4-5].

Since the LNA is the first gain stage in a receiver path, its performance will determine the sensitivity of the whole system. The basic requirements of an LNA are good impedance matching, low noise, high gain and gain flatness over the band of interest. The gain flatness plays a significant role in both sensitivity and channel capacity. Modulation schemes dictate the specifications of the gain flatness. In 60 GHz radios, at least 9 GHz flat gain is needed for the whole band in order to use 16-QAM modulation. Considering the process, voltage and temperature (PVT) influence, more than 9 GHz bandwidth is required.

In recently reported papers, both the common-source (CS) and cascode (CAS) topology are utilized in millimeter-wave LNA design. Because a single stage amplifer cannot provide sufficient gain and bandwidth, both of the topologies need several stages cascaded together. The inter-stage matching becomes important in reducing the loss and increasing the bandwidth. Because CS topology realizes a smaller noise figure than CAS topology [6], a four-stage CS LNA is designed using a simple inter-stage matching network in this paper. The measured 3-dB bandwidth of the designed LNA is 23 GHz. The power gain can be changed from 6.3 dB to 17.5 dB at 60 GHz by a variable DC bias.

Section II shows the LNA circuit design. The measurement results are given in Section III. The final conclusions are shown in Section IV.

II. LNA CIRCUIT DESIGN

A. Flat gGain flatness at RF radios

Fig. 1 shows the importance of gain flatness in simple receiver architecture. The amplified signals by LNA at 60 GHz radios are changed to baseband using a down conversion mixer. If the gain of the LNA is not flat, the amplification is not constant across the bandwidth resulting in an irregular baseband signal after the down-conversion, which cannot be compensated at baseband (Fig. 1(a)). On the other hand, if the gain of LNA is flat, the amplification is constant across the bandwidth obtaining well-regulated signals, which can be compensated easily at baseband (Fig. 1(b)).

B. Impedance matching consideration

Currently, CMOS millimeter-wave impedance matching can be divided into two approaches, where one uses transmission lines and the other employs spiral inductors. It is difficult to get the exact spiral inductor values in millimeter-wave circuits, while a wide range of scalable inductance values can be easily implemented by adjusting the length of transmission lines (TLs). Bend and branch sections are also important for accurate characterization of TLs. In this paper, the guided micro-strip transmission line and T-junction in [7] is employed for the impedance matching.

The inter-stage impedance matching influences the band width as well as the power gain. At millimeter-wave frequency, the parasitic capacitance and intrinsic capacitance of MOSFETs have to be resonated by adding inductive element to the inter-stage matching network. The third–order high-pass π-section network can achieve a better bandwidth than the traditional L-section network for inter-stage matching. In order to obtain a flat gain, π-section network is considered in this paper.

Inter-stage matching can be treated as two cases. Firstly, the output impedance of first stage can be matched to 50Ω, and the input impedance of second stage can also be matched

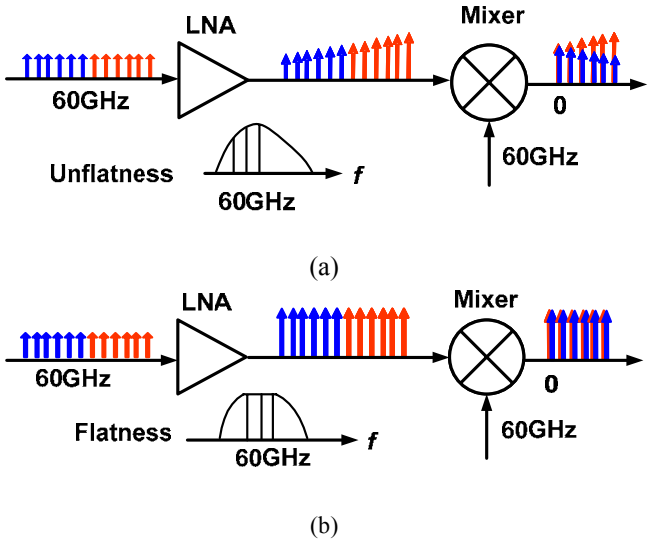


Fig. 1 LNA gain flatness in receiver, (a) gain not flatness, (b) flat gain.

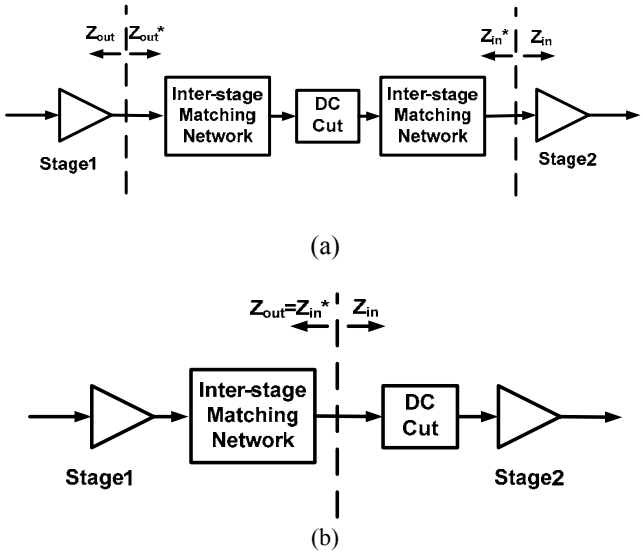


Fig. 2 Two schematic diagrams of inter-stage matching network.

to 50Ω. Secondly, the output impedance of first stage and the input impedance of second stage are conjugated into each other. Fig. 2 shows two schematic diagrams of inter-stage matching networks. Generally, Fig. 2(a) can be considered as a π-section network. While at millimeter-wave frequency, the parasitic capacitance and intrinsic capacitance of MOSFETs are also part of the impedance matching network. Fig. 2 (b) is also treated as a π-section network. Fig. 2(a) needs a more complex network and occupies more chip area than Fig. 2(b). In the four-stage LNA, the schematic of Fig. 2(b) is utilized for inter-stage matching network.

C. Proposed LNA schematic

The schematic of the proposed four-stage LNA is shown in Fig. 3 An accurate transistor model is very important in the circuit design. The transistor models used in this paper are described in [9] by the authors. As introduced in [9], transistors with a 2 μm finger width achieve a better maximum power gain, while the minimum noise finger (NF) depends on the small gate resistance, which is obtained by short finger width. Considering the trade-off between power gain and NF, both finger width of 1 μm and 2 μm are utilized to realize total widths of 40 μm transistors. 40-finger transistors, with each finger width of 1 μm, are utilized in the first two stages to optimize the noise performance. The last two stages utilize 20-finger transistors, with finger width of 2 μm, to optimize for a better power gain. MIM transmission line in [4] and a 2 Ω resistor are used for AC de-coupling and to prevent oscillating in all the DC supply voltage. A bias voltage of 0.6 V is set in the first stage for a current density of 0.15 mA/μm, which is the optimum current density for NF_{min} [8]. The other three stages use one DC bias for gain adjustment. All the DC biases are obtained by 21 kΩ resistors. The inter-stage matching network is simpler than other reported TLs matching networks [8-10].

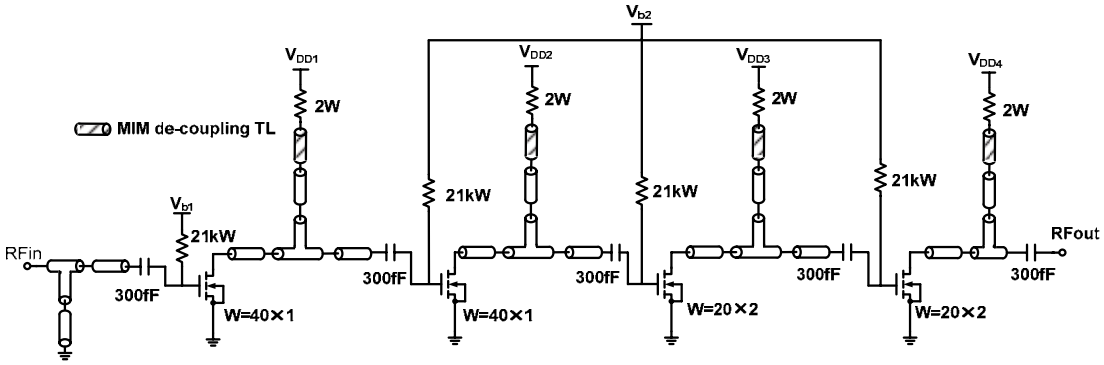


Fig. 3 Schematic of proposed LNA.

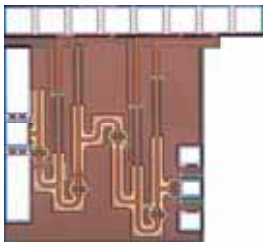


Fig.4 LNA microphoto

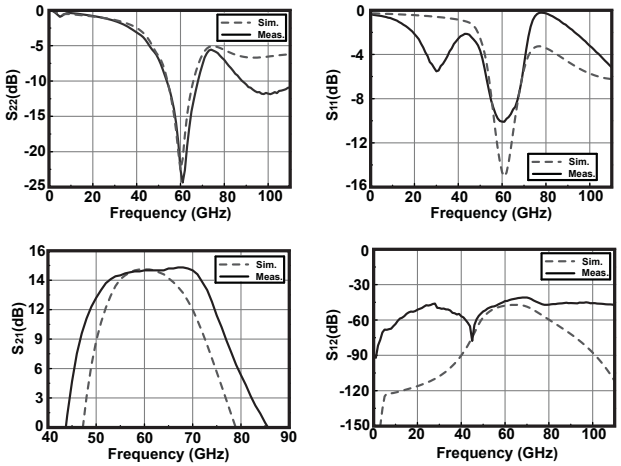
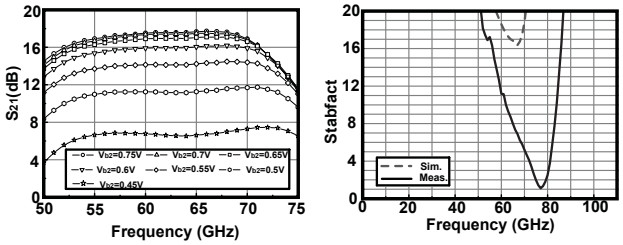


Fig. 5 The simulated and measured S-parameter.



(a) (b)

Fig. 6 (a) Measured variable power at different bias voltage. (b). The simulation and measured stability factor.

III. Simulation and Measurement Results

The designed LNA is implemented in a 65 nm CMOS process. All the devices utilized in the circuit are extracted from measurement data, de-embedded by using the method in [8], and modeled in Agilent ADS. The simulation is also carried out in ADS. The S-parameter up to 110 GHz is measured by Agilent N5250A together with Agilent N5260A

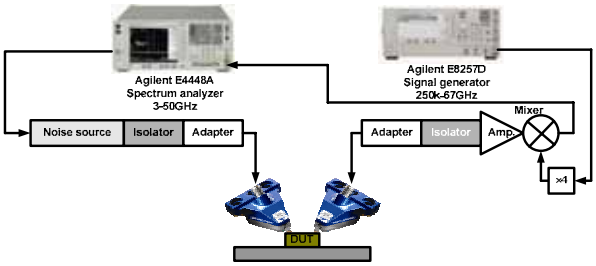


Fig. 7 NF measurement setup

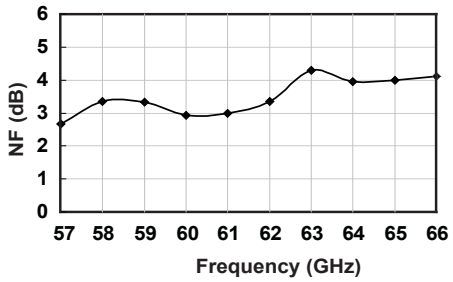


Fig. 8 Measured NF of LNA.

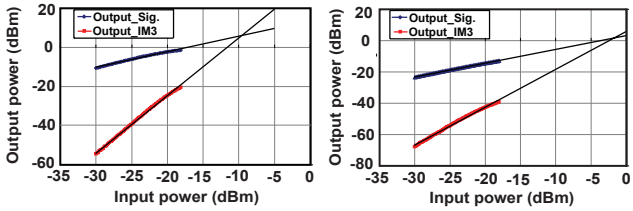


Fig. 9 Measured IIP3 at 60GHz in the high gain (left) and low gain (right) mode.

mm-wave controller. The measurement on wafer includes the pad. Chip photo is shown in Fig. 4. The total size of the LNA including RF pads is about 0.354 mm^2. The simulated and measured S-parameter is shown in Fig. 5.All the DC supply voltage is 1.0 V and all the DC biases are set to 0.6 V, the power dissipation is 24 mW. The measurement input matching does not agree with the simulation well due to the increased of transistor's source impedance caused by the ground plane and the modeling error related to short stub. Furthermore, the white noise floor is the main reason for the disagreement in S_{12}.

Fig. 6 shows the gain adjustment by changing the DC bias voltage and the stability factor. A maximum power gain of 17.5 dB is achieved at 66 GHz in the high gain mode. The measured 3-dB bandwidth is about 23 GHz from 50 GHz to 73 GHz in the high gain mode and the variable gain is realized from 6.3 dB to 17.5 dB at 60 GHz by adjusting the bias voltage. Although the differences of S-parameter

TABLE I
Performance comparison

Reference	**This work**	[1] RFIC2008	[2] JSSC2007	[3] JSSC2008	[8] ESSCIRC2010	[10] JSSC2007	[11] VLSI2009
Technology	**65nm**	90nm	90nm	90nm	65nm	90nm	90nm
Topology	**CS**	CS	Cas.	Cas.	CS	CS	Cas.
Stage	**4**	3	2	2	4	2	3
f_{center} [GHz]	**68**	58	58	64	53	63	63
BW [GHz]	**23**	5	6	8	17	-	14
Gain [dB]	**17.5**	15	14.6	15.5	24	12.2	24
NF [dB]	**<4.3**	4.4	5.5	6.5	4	6.5	6.8
Power [mW]	**24**	3.9	24	86	30	10.5	36

between simulation and measurement cause the measurement stability factor changed a lot comparing the simulation results, it is still above 1 and the LNA is unconditional stable.

Noise measurement and calculation process is using the same method in [8]. The measurement set up is shown in Fig. 7. From 57 GHz to 66 GHz at 1 GHz interval by using double-side band mixing is measured. The measured NF is less than 4.3 dB as shown in Fig. 8. Agilent PNA-X Network analyzer N5247A is used to measure IIP3.The measured IIP3 at 60 GHz is shown in Fig. 9. An IIP_3 of -9.8 dBm in the high gain mode and -1.8 dBm in the low gain mode are realized. The performance comparison is summarized in Table I.

IV. Conclusion

As the first stage of a transceiver, the LNA gain flatness over the band plays a signification role for modulation. A four-stage common source LNA is proposed using simple inter-stage matching network. 23GHz 3-dB bandwidth is obtained in this LNA. The variable gain is realized from 6.3 dB to 17.5 dB by adjusting the bias voltage. The measured NF is less than 4.3 dB, and the measured IIP_3 is -1.8 dBm.

Acknowledgement

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References

[1] E. Cohen, S. Ravid, D. Ritter, "An ultra low power LNA with 15dB gain and 4.4db NF in 90nm CMOS process for 60 GHz phase array radio," *IEEE RFIC.* , pp.61-64, Jun. 2008.

[2] T. Yao., M.Q. Gordon, K.K.W. Tang, K.H.K. Yau, Yang M. Yang; P. Schvan, S. P. Voinigescu, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio,", *IEEE JSSC* , vol.42, no.5, pp.1044-1057, May 2007

[3] S. Pellerano, Y. Palaskas, K. Soumyanath, "A 64 GHz LNA With 15.5 dB Gain and 6.5 dB NF in 90 nm CMOS," *IEEE JSSC*, vol.43, no.7, pp.1542-1552, July 2008

[4] K. Okada, K. Matsushita, K. Bunsen, R. Murakami, A. Musa,T. Sato, H. Asada, N. Takayama, N. Li, S. Ito, W. Chaivipas, R. Minamiand A. Matsuzawa, "A 60GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE 802.15.3c," *IEEE ISSCC*, pp. 160-161, Feb. 2011.

[5] S. Emami, R. F. Wiser, E. Ali, M. G. Forbes, M. Q. Gordon, X. Guan, S. Lo, P. T. McElwee, J. Parker, J. R. Tani, J. M. Gilbert, and C. H. Doan, "A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," *IEEE ISSCC*, pp. 164− 165, Feb. 2011,.

[6] N. Li; K. Okada, T. Suzuki, T. Hirose, A. Matsuzawa, "A three-stage 60GHz CMOS LNA using dual noise-matching technique for 5dB NF," *IEEE APMC*, pp.1-4, 16-20 Dec. 2008

[7] K. Okada, "Test Structures for Millimeter-Wave CMOS Circuit Design," *IEEE GSMM,* Apr. 2009

[8 N. Li; K. Bunsen, N. Takayama, Q. Bu; T. Suzuki, M. Sato, T. Hirose, K. Okada, A. Matsuzawa, , "A 24 dB gain 51–68 GHz CMOS low noise amplifier using asymmetric-layout transistors," *IEEE ESSCIRC*, pp.342-345, 14-16 Sept. 2010

[9] N. Li, K. Matsushita, N. Takayama, S. Ito, K. Okada, and A. Matsuzawa, "Evaluation of a multi-line de-embedding technique up to 110GHz for millimeter-wave CMOS circuit design," *IEICE Trans. on Fund.*, vol. E93-A, no. 2, pp. 431–439, Feb. 2010.

[10] B. Heydari, M. Bohsali, E. Adabi, A. M. Niknejad, "Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS," *IEEE JSSC*, vol.42, no.12, pp.2893-2903, Dec. 2007

[11] Y. Natsukari, M. Fujishima, "36mW 63GHz CMOS differential low-noise amplifier with 14GHz bandwidth," *IEEE VLSI Circuit*, pp.252-253, Jun. 2009