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Two-Stage Band-Selectable CMOS Power Amplifier

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Contents

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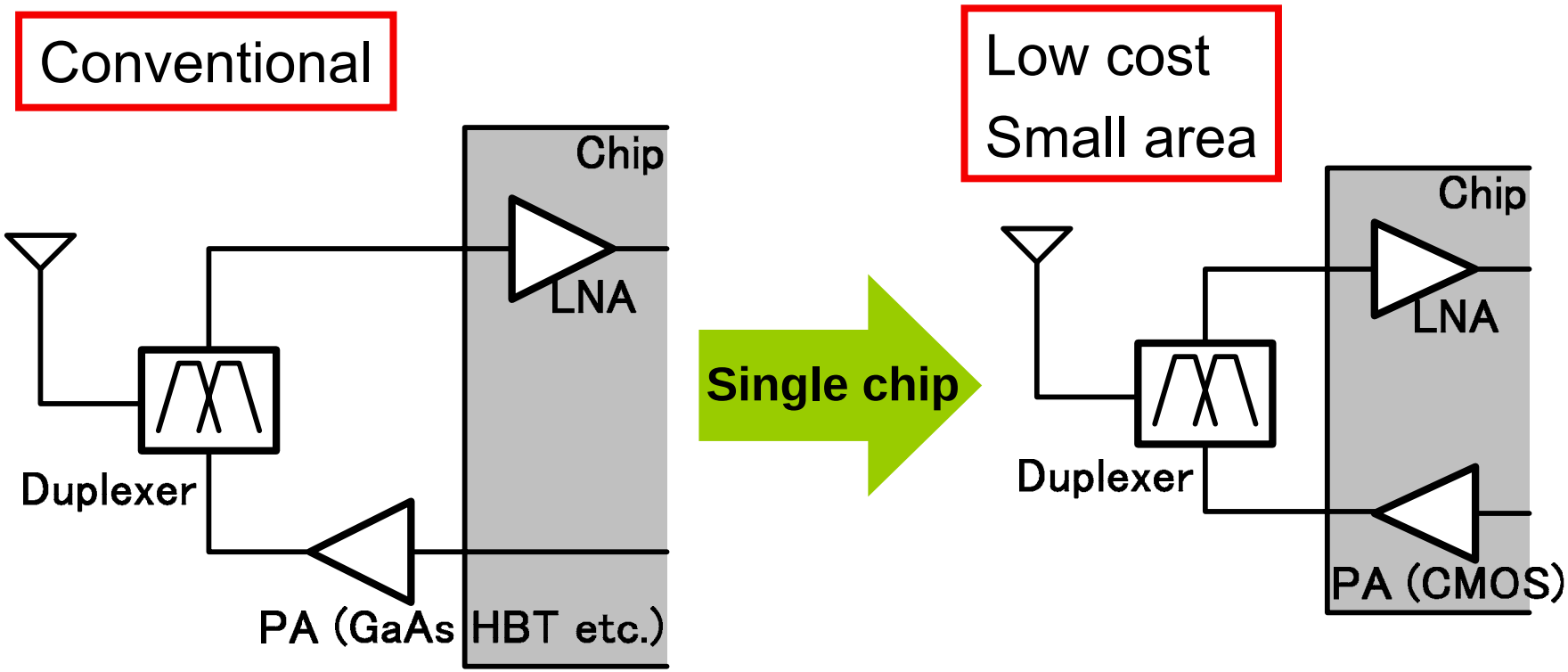
- Introduction
- PA design
- Measurement results
- Conclusion

Single chip transceiver



- Single chip transceiver is demanded because of its low cost and downsizing.

Various wireless applications

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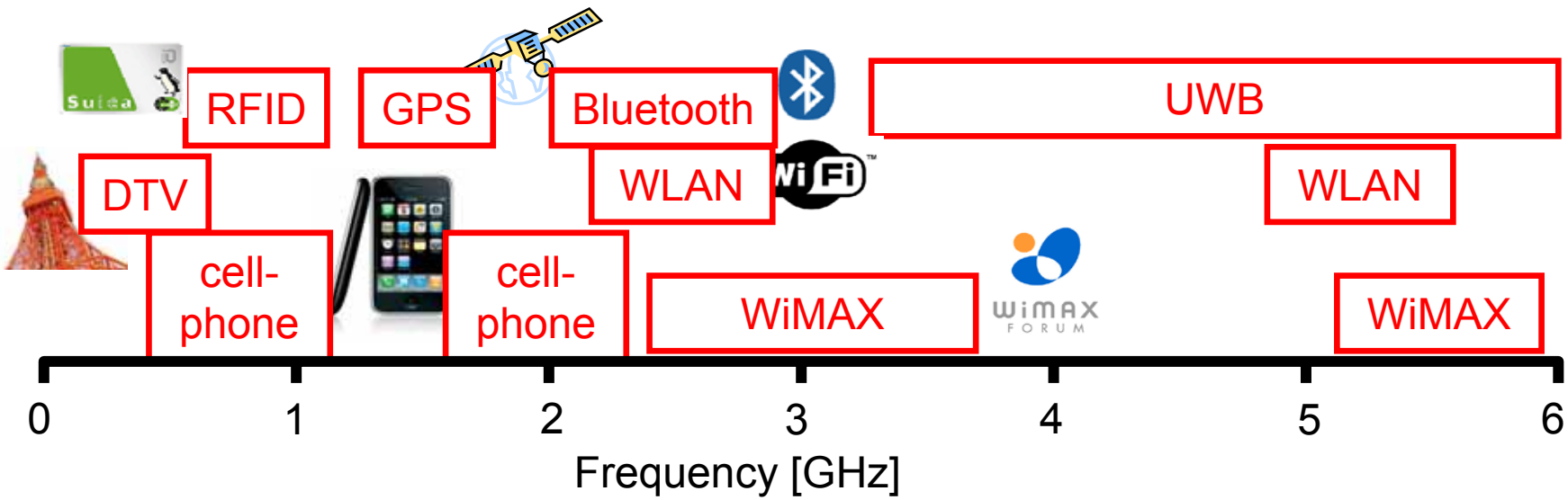
- Various wireless communication standards



- A broad band device (PA) is necessary to support various wireless applications.

Conventional wideband PA

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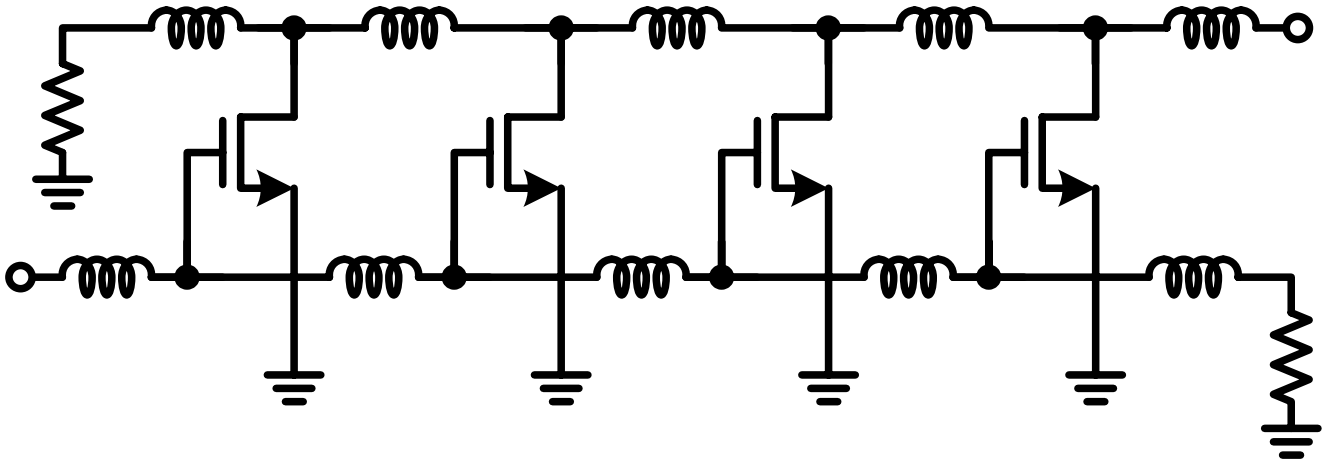
- Distributed power amplifier



✓ **Wideband input / output matching**
→ Possibility of intermodulation

✗ **Lack of the optimum impedance matching**
→ Insufficient output power

✗ **Many inductor** → Large area

Target of proposed PA

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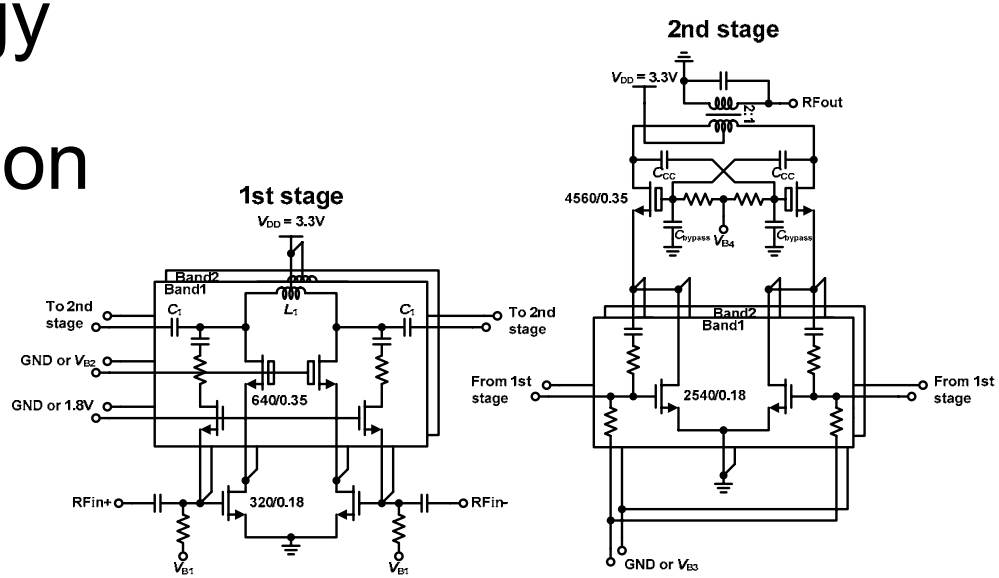
- Large output power
  - High supply voltage
  - Differential topology
  - 2-stage configuration
  - Transformer
- Band-selection
  - Change of impedance matching



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Schematic

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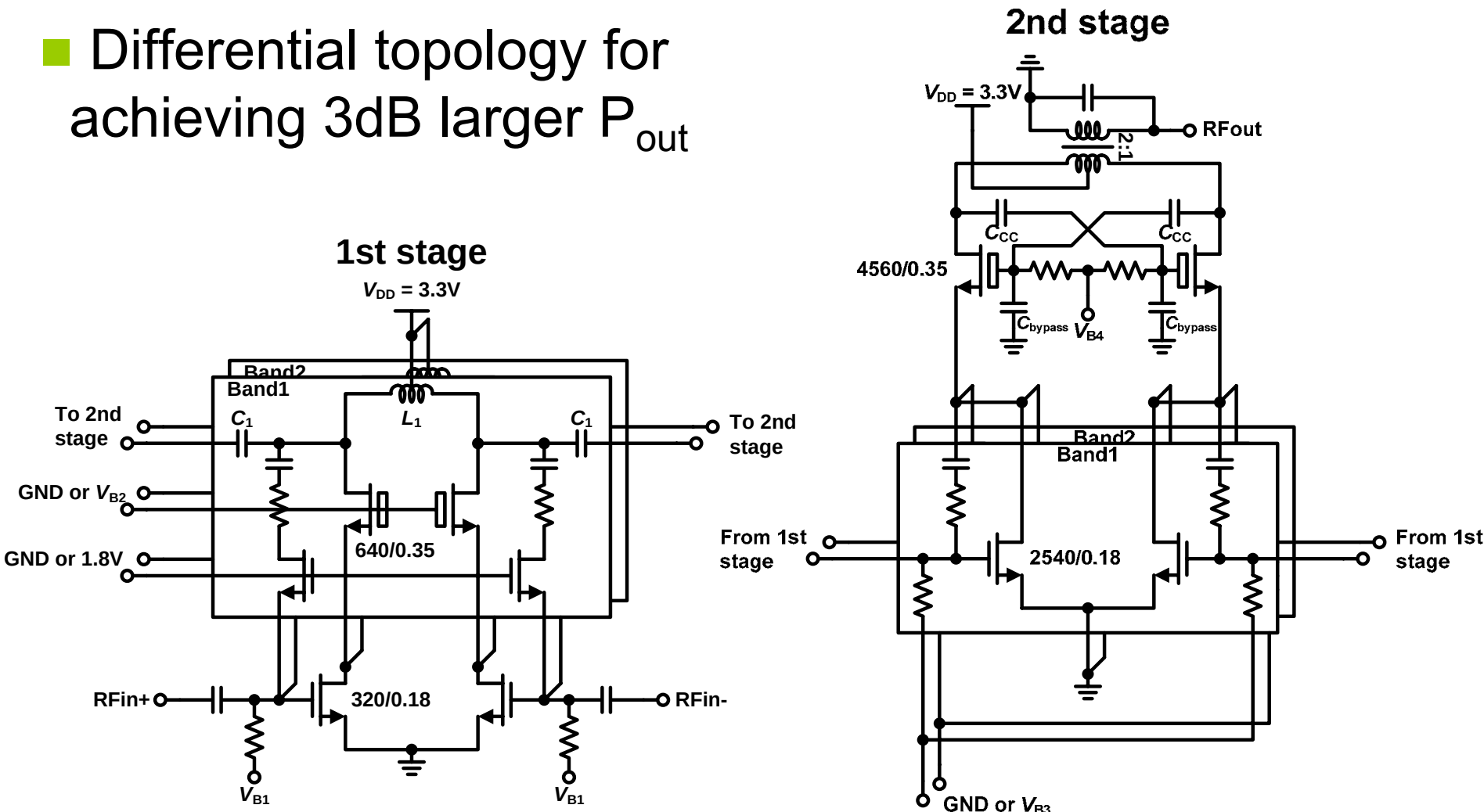
- Class-A bias(1st stage), Class-AB bias(2nd stage)
- Differential topology for achieving 3dB larger P_{out}



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Consideration for voltage stress

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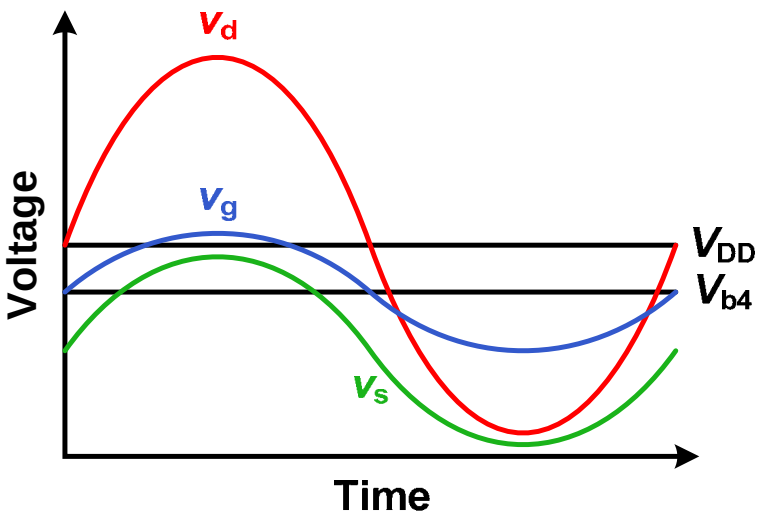
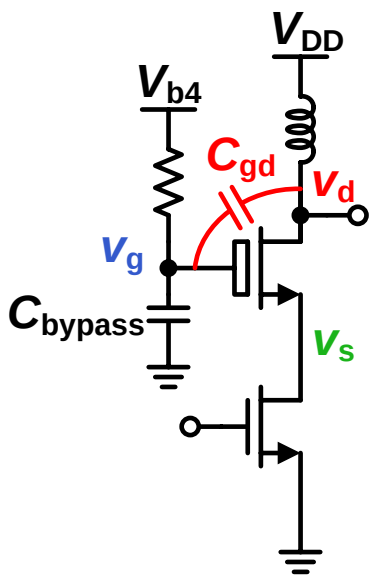
- Cascode topology with thick gate-oxide transistor
- Self-biased cascode: technique that allows RF swings at the common gate transistor. [1] T. Sowlati *et al.*, JSSC 2003.
  - ☺ Reduction of voltage v_{gd}
  - ☺ Prevention of transistor's entering to triode region





V_{DD}=3.3V

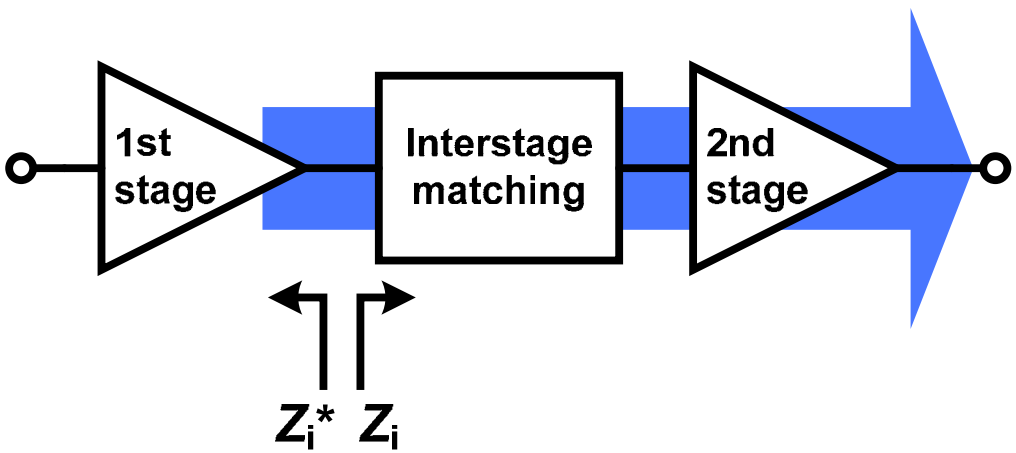
If C_{gs} is neglected,

$$v_g = \frac{C_{gd}}{C_{bypass} + C_{gd}} v_d$$

[Conceptual diagram of voltage waveforms]

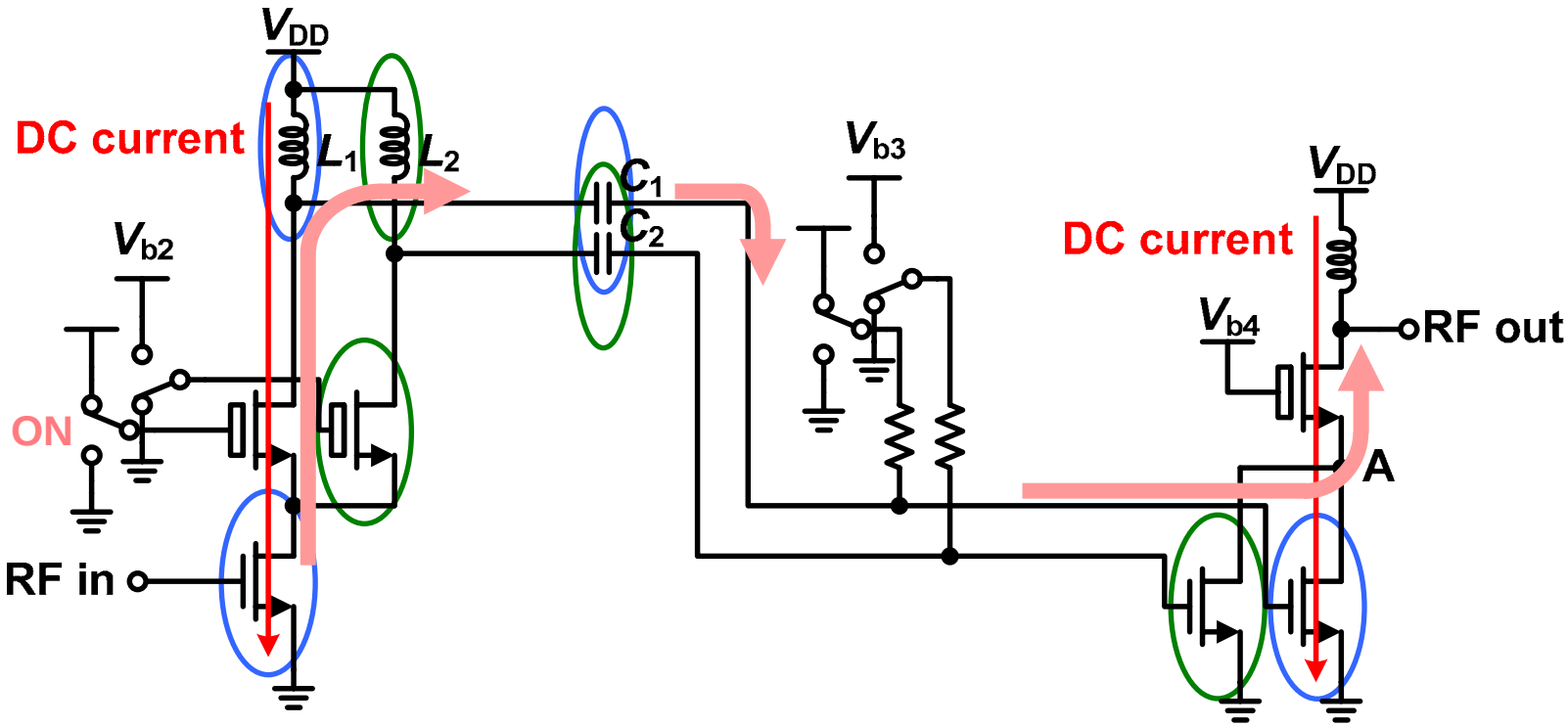
Interstage matching

- To get a sufficient gain practically
  → **a 2-stage configuration**
- To transfer power from the 1st stage to the 2nd stage
  → **a complex conjugate impedance matching**



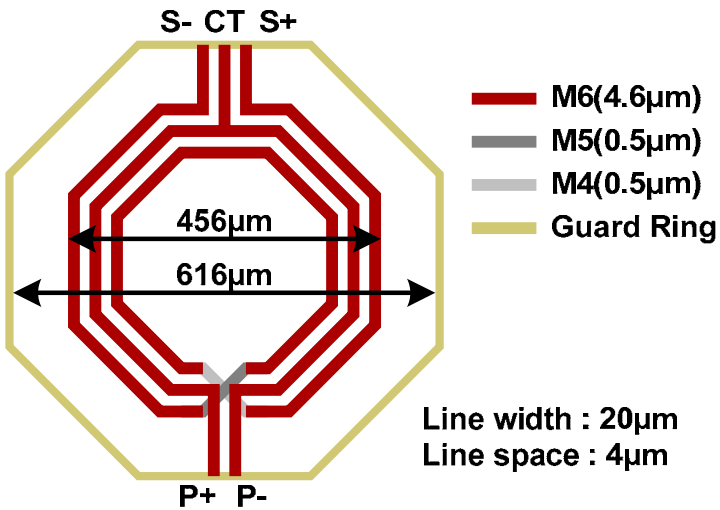
Change of impedance matching

If ***L*-shaped matching** which consists of L_1&C_1 is effective



- Current flows through only the transistors to use
- Switching which consists of inductor and capacitor is realized in low-loss.

Transformer



- **Turn ratio=2:1**
- **Z_{out} (50Ω)**
  → ¼ Z_{out}(12.5Ω)

- **Relation between P_{sat} & Z_{out}**

$$P_{sat} = \frac{\left(V_{DD}/\sqrt{2}\right)^2}{Z_{out}}$$

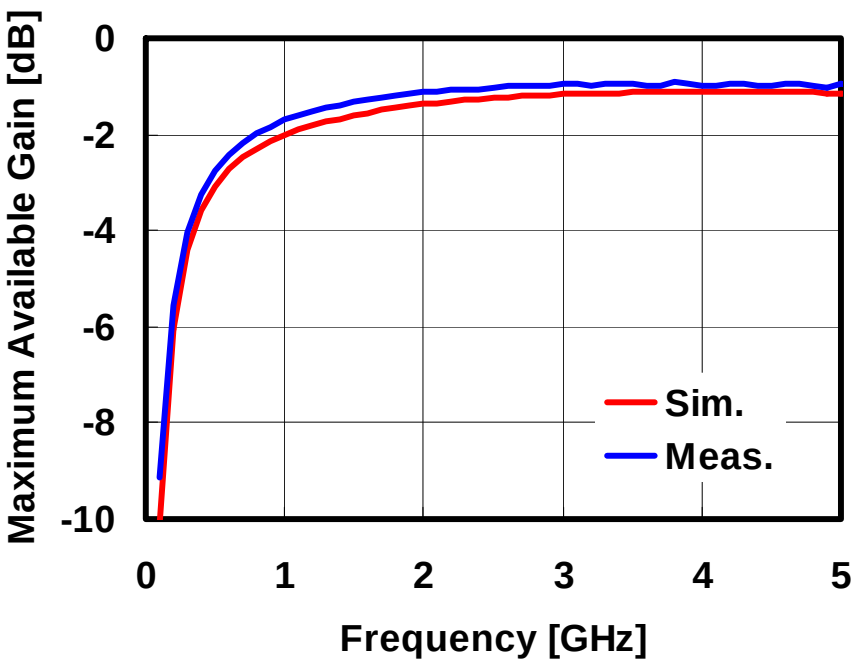
- **Theoretical maximum output power P_{sat}**

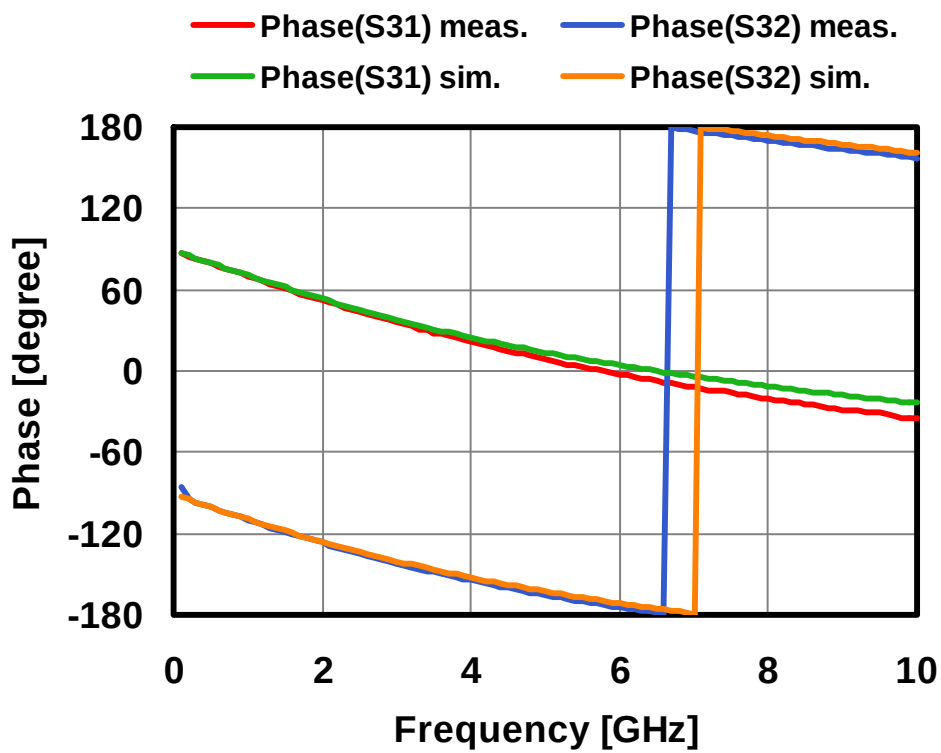
$$P_{sat} = \frac{\left(2\times V_{DD}/\sqrt{2}\right)^2}{\left(2\times \frac{1}{4} Z_{out}\right)} = \frac{\left(2\times 3.3/\sqrt{2}\right)^2}{\left(2\times \frac{1}{4}\times 50\right)}$$

$$= 0.8712[\mathrm{W}] = 29.4[\mathrm{dBm}]$$

Transformer

- Coupling coefficient = 0.7
- Maximum Available Gain(MAG) = -1.05 dB
- Conversion efficiency= $10^{(-1.05\text{dB}/10)} \times 100$ =78.5 %

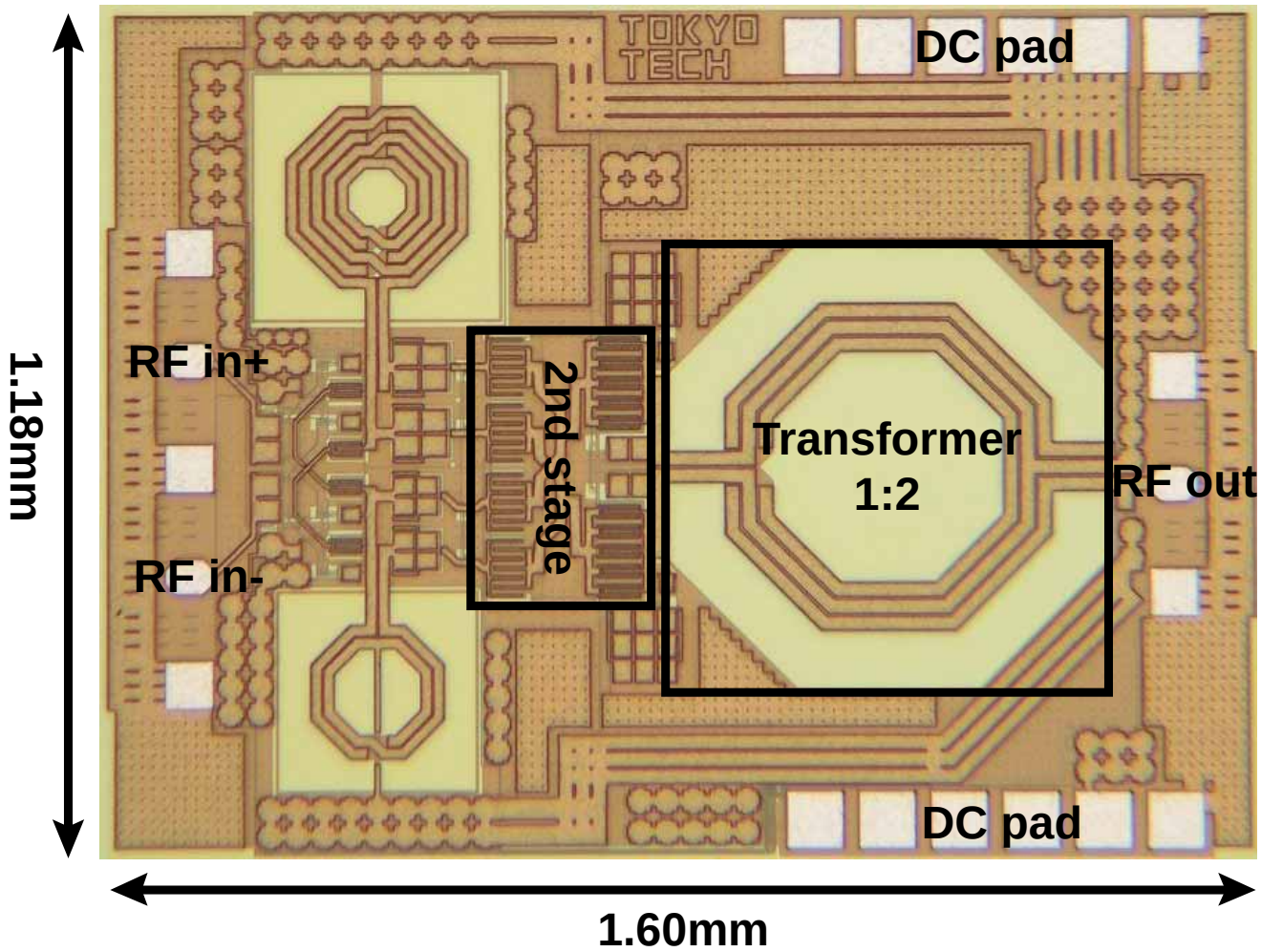




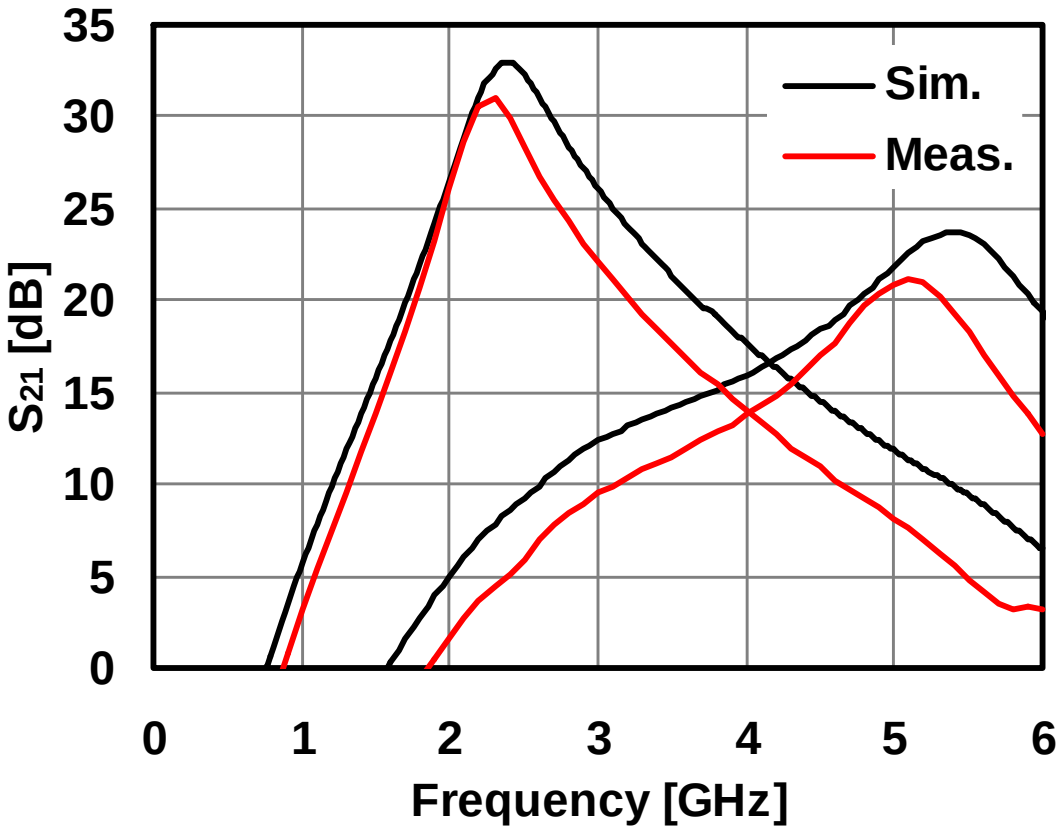
- Measurement and simulation results agree with each other.

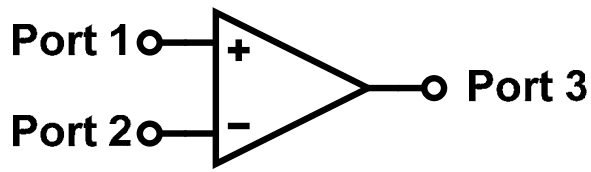
Chip micrograph

- TSMC 0.18μm CMOS process



S-parameter measurement result

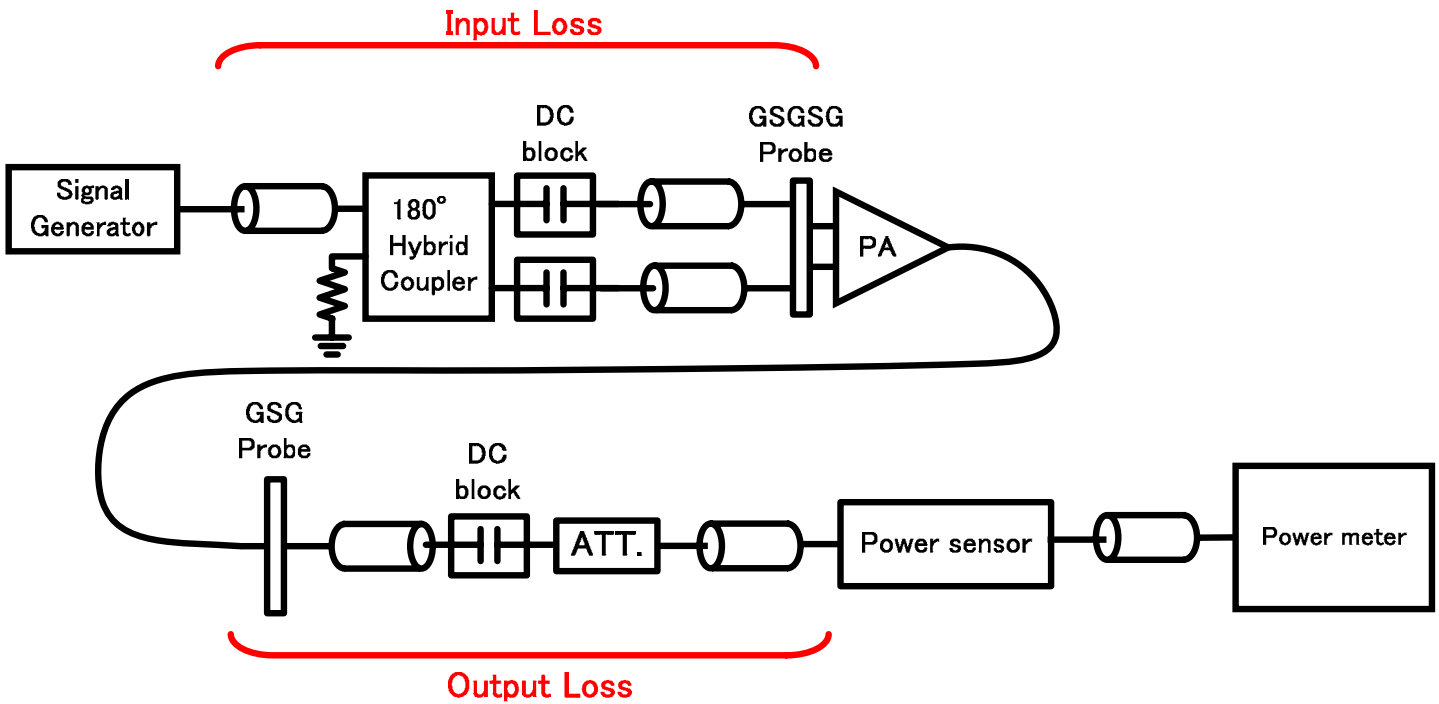




- **Measurement results are roughly in accordance with simulation results**

Measuring system

- **Large signal measurement setup**



- **Input and output losses are measured separately, and are calibrated from results.**

Large signal measurement result

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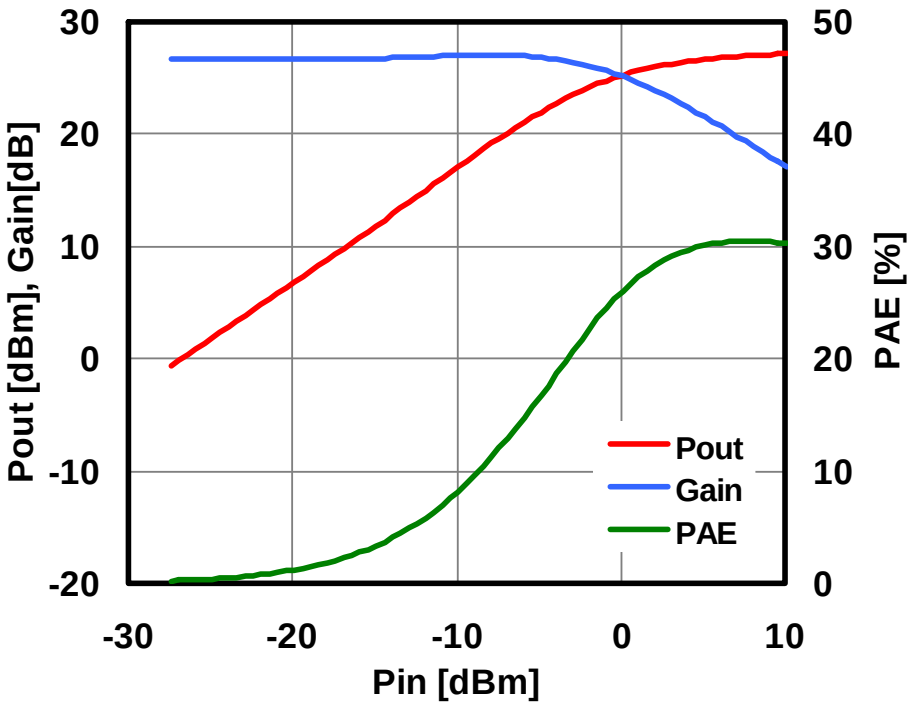
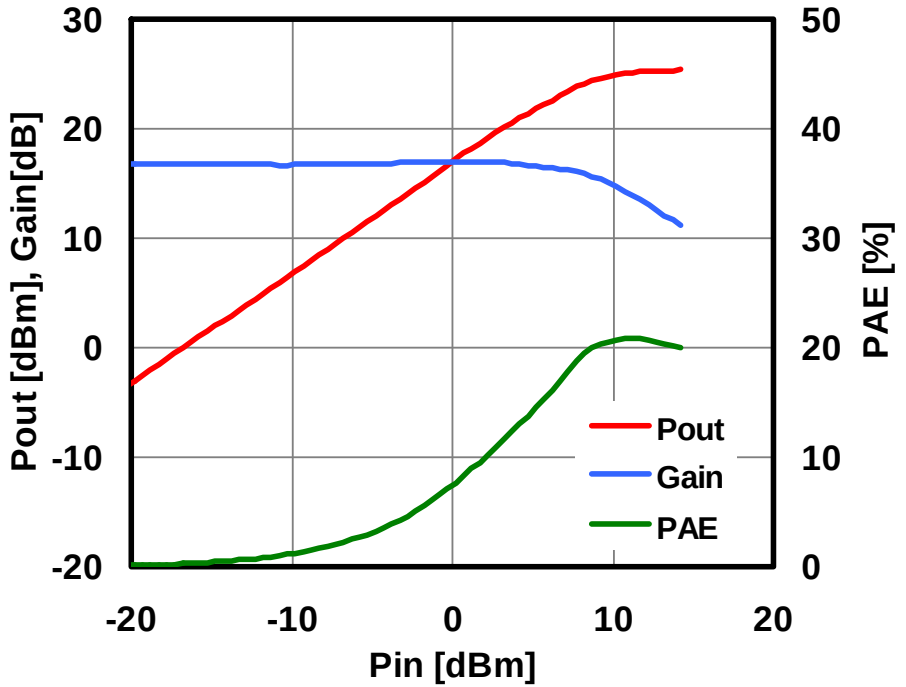
- **Band1 at 2.6GHz**



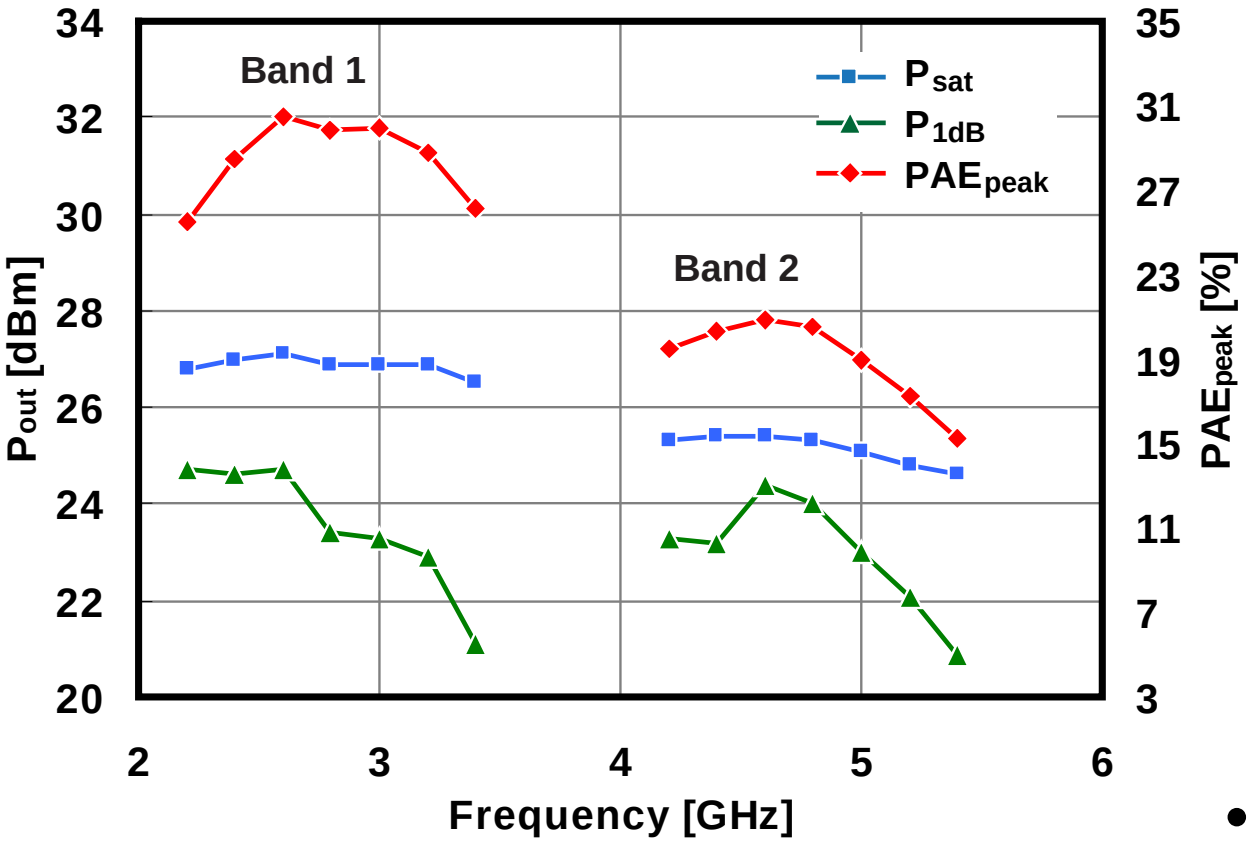
P_{1dB} = 24.7 dBm
P_{sat} = 27.1 dBm
PAE_{peak} = 30.5 %

- **Band2 at 4.6GHz**



P_{1dB} = 24.4 dBm
P_{sat} = 25.4 dBm
PAE_{peak} = 20.9 %

Large signal measurement result



- $P_{1dB} \geqq 21dBm$
- $P_{sat} \geqq 25dBm$
- $PAE_{peak} \geqq 15\%$

Comparison of CMOS PAs

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	[1]	[2]	[3]	This work
Technology	0. 13 μm CMOS process		0.18 μm CMOS process	
V_{DD} [V]	1.5	1.5	3.3	3.3
Frequency [GHz]	0.5~5.0	2.4/3.5	2.1~6.0	**2.2~3.4, 4.2~5.4**
P_{1dB} [dBm]	10~17	-	15~18	**21~25**
P_{sat} [dBm]	14~21	19	18~22	**25~27**
PAE_{peak} [%]	*3~16	43	9~17	**15~30**
Area [mm^2]	3.6	1.3	0.97	1.89

* DE: Drain Efficiency

[1] H. Roderick, et al., "A 0.13μm CMOS Power Amplifier with Ultra-Wide Instantaneous Bandwidth for Imaging Applications," *IEEE ISSCC Dig. Tech. Papers*, pp. 374-375, Feb. 2009

[2] M Ghajar, et al., "Concurrent Dual Band 2.4/3.5 GHz Fully Integrated Power Amplifier in 0.13μm CMOS Technology," *IEEE European Microw. Conf.*, pp. 1728-1731, Sep. 2009

[3] D.Imanishi, et al., "A 2-6 GHz Fully Integrated Tunable CMOS Power Amplifier for Multi-Standard Transmitters," *IEEE Asia and South Pacific Design Automation Conference*, pp. 351-352, Feb. 2010

Conclusion

- 2-stage band-selectable CMOS PA with high PAE
- Circuit design
  - Using TSMC 0.18μm CMOS process
  - Switching of the inter-stage matching to change the frequency
  - Use of 2-stage configuration & differential topology& transformer to obtain high PAE
- Results : **PA with Small size and High performance**
  - Frequency : 2.2 ~ 3.4, 4.2 ~ 5.4 GHz
  - P_{1dB} = 21~25dBm, P_{sat} = 25~27dBm, PAE_{peak} = 15~30%