A 0.5 V, 1.2 mW, 160 fJ, 600 MS/s 5 bit Flash ADC

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5-bit Low-Voltage Flash ADC

1. An ultra-low power ADC is strongly required
   - Portable applications, ubiquitous wireless sensor systems, and green IT
2. A low-voltage operation is required for further technology scaling and low power operation
   - FoM of ADCs should be reduced like digital circuits optimizing speed, resolution and power
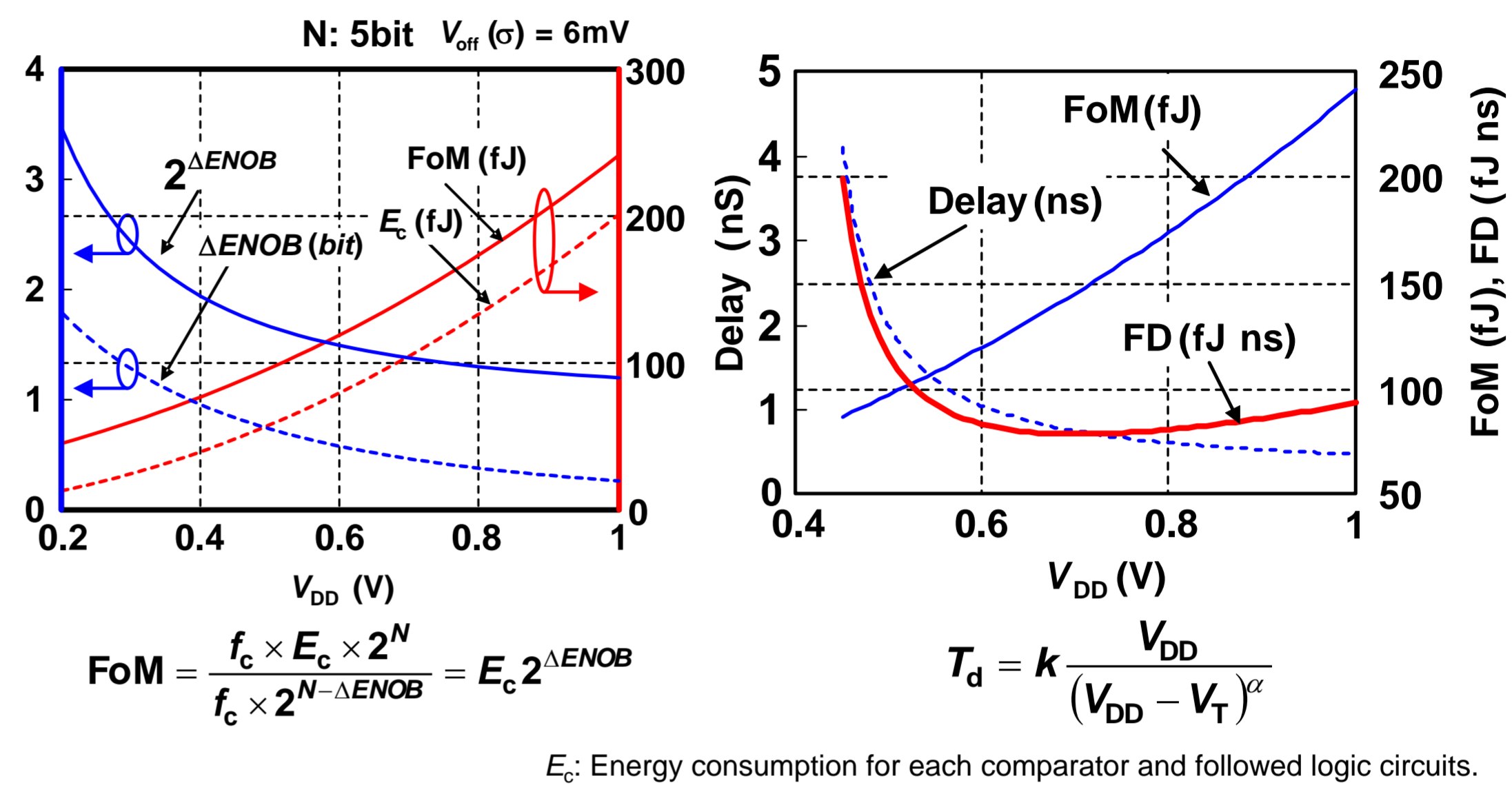   - Low-voltage calibration techniques are required
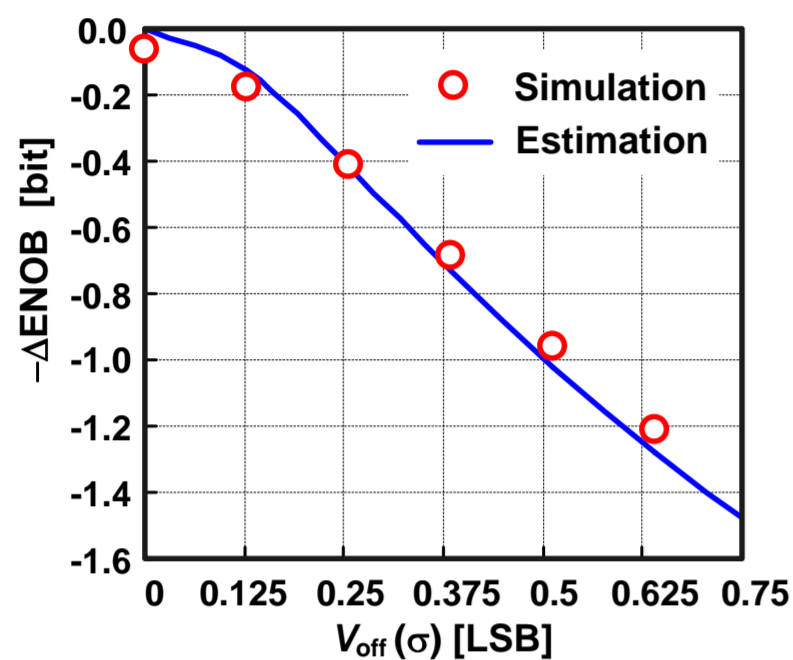
$$FoM = \frac{P_d}{f_c \times 2^{N-\Delta ENOB}}$$

$$\Delta ENOB = \frac{1}{2}\log_2\left(1 + 12\left(\frac{V_{off}(\sigma)}{V_q}\right)^2\right)$$

$V_{off}(\sigma)$:Offset voltage
V_q : 1LSB voltage

Low-Voltage Strategies

- FoM can be significantly reduced with V_{DD} lowering
- The FoM-Delay (FD) product suggests the balance between the interleaving number and energy saving

N: 5bit $V_{off}(\sigma)$ = 6mV

$$FoM = \frac{f_c \times E_c \times 2^N}{f_c \times 2^{N-\Delta ENOB}} = E_c 2^{\Delta ENOB}$$

$$T_d = k\frac{V_{DD}}{(V_{DD} - V_T)^\alpha}$$

E_c: Energy consumption for each comparator and followed logic circuits.

Forward Body Biasing

- Advantages
  - Reduces the delay time to 1/2
  - Allows for 0.5 V operation by reducing V_{TP} and V_{TN} by 60 mV and 100 mV, respectively
- Disadvantage
  - Leakage current in the proposed ADC is increased by 0.32 mA

V_{DD}

V_{TP} ↓60mV
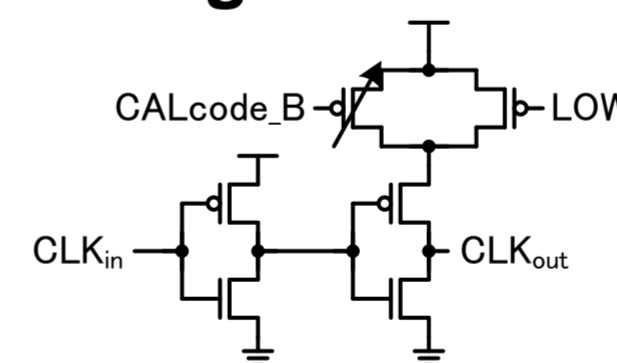
IN — OUT

V_{TN} ↓ 100mV
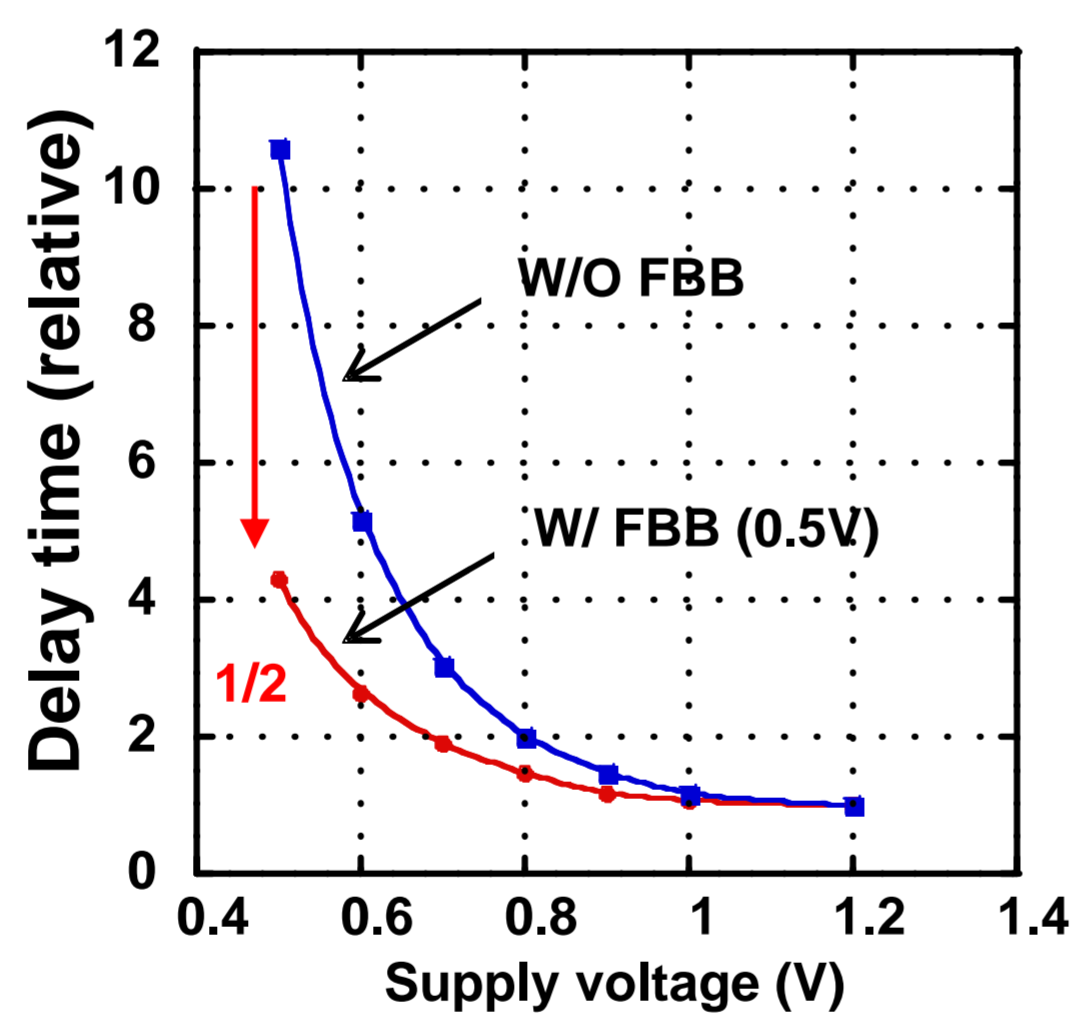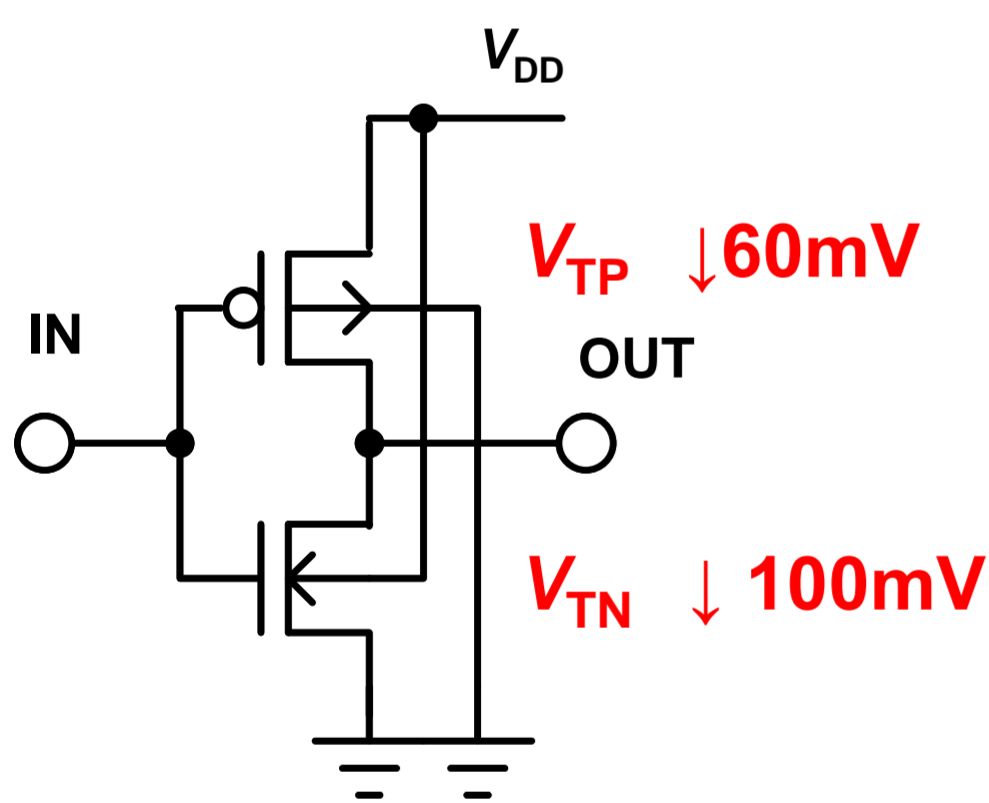
Timing-based Calibration

- Conventional capacitor DAC calibration [1] operating under low voltage
  - MOS varactor's sensitivity decreases
  - Delay time and power consumption increases
- Proposed timing-based calibration
  - Time is independent of supply voltage lowering
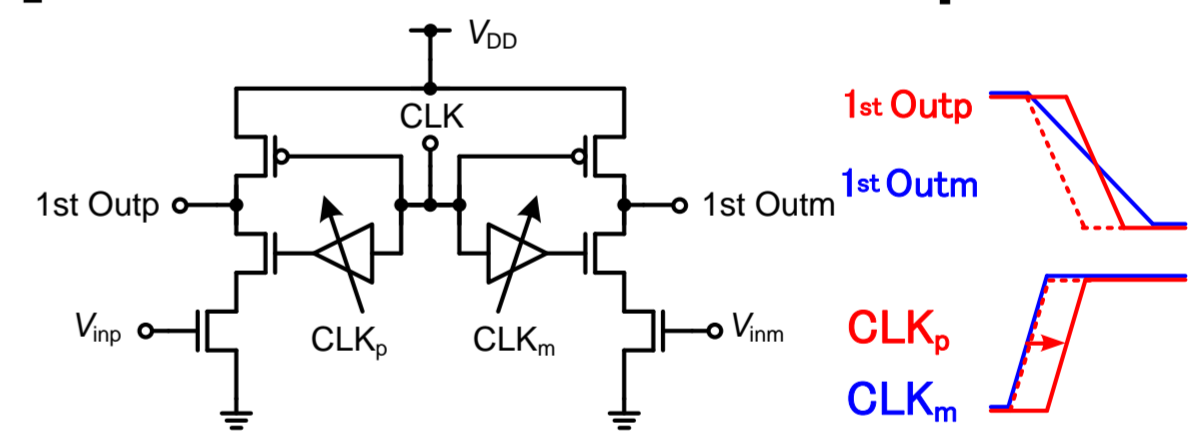 - DNL/INL 2 LSB → 0.5 LSB

Conventional Cap.-DAC Calibration Technique [1]
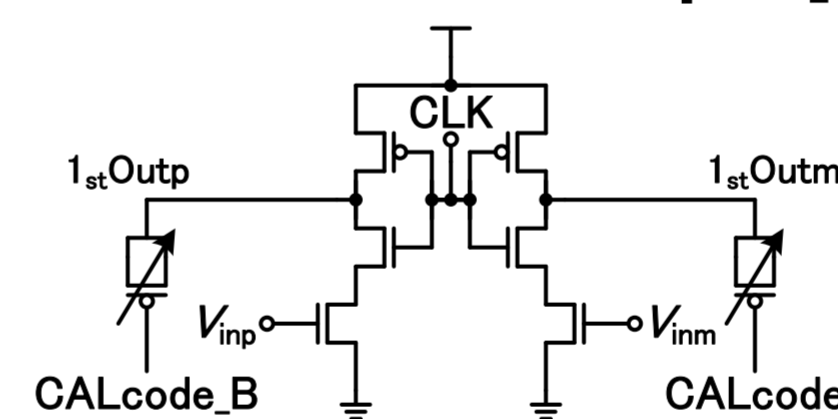
Proposed Timing-based Calibration Technique

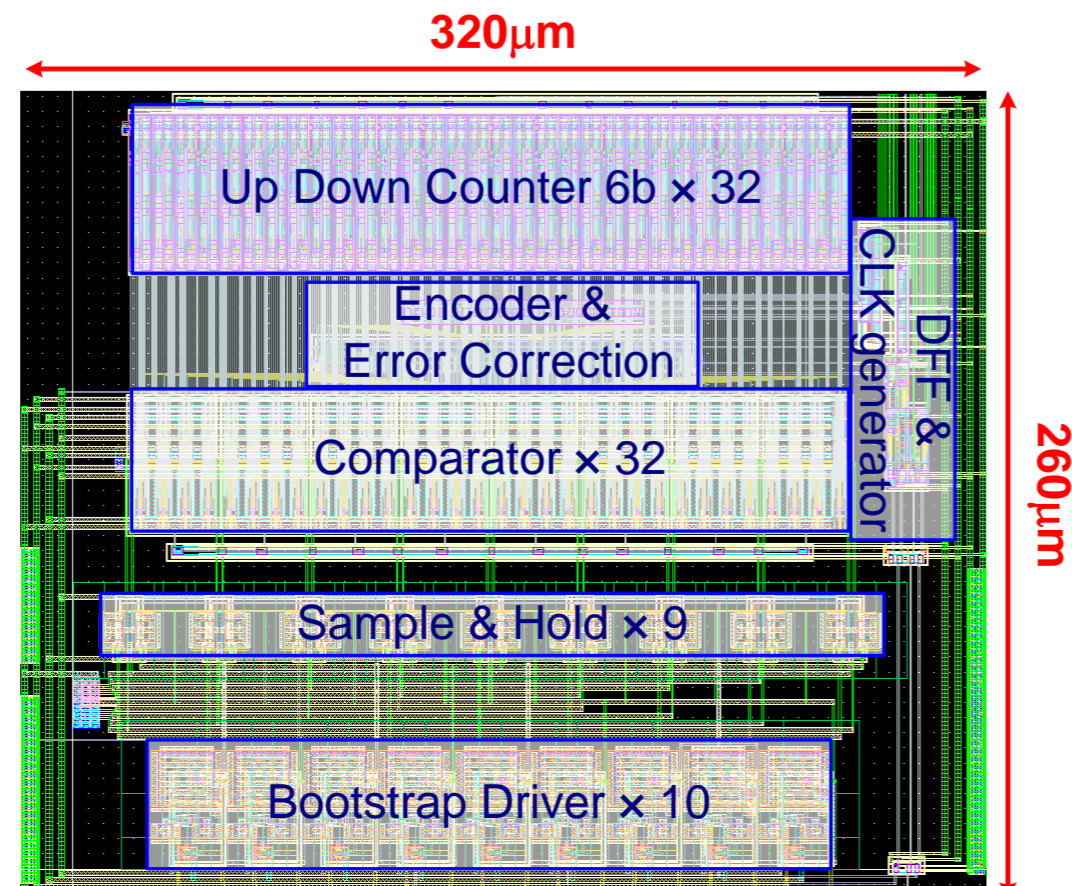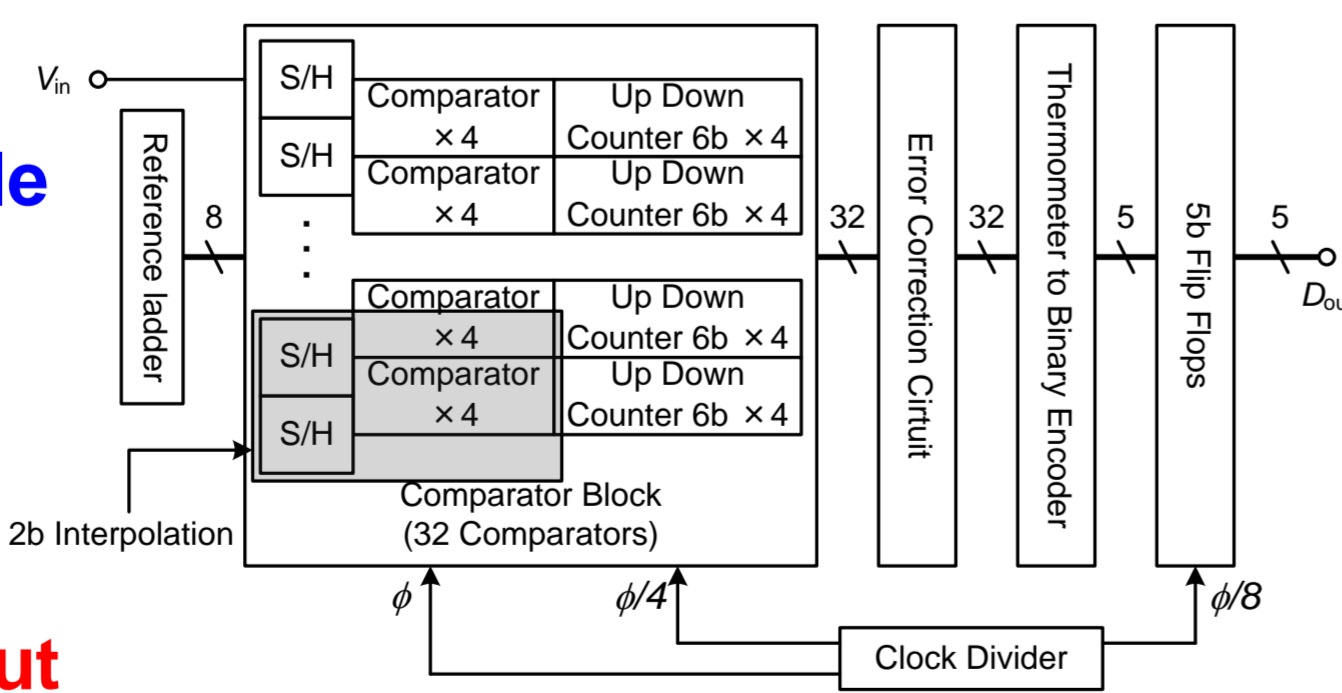**Timing controller**

V_{DD}=0.5V, f_s=500MHz

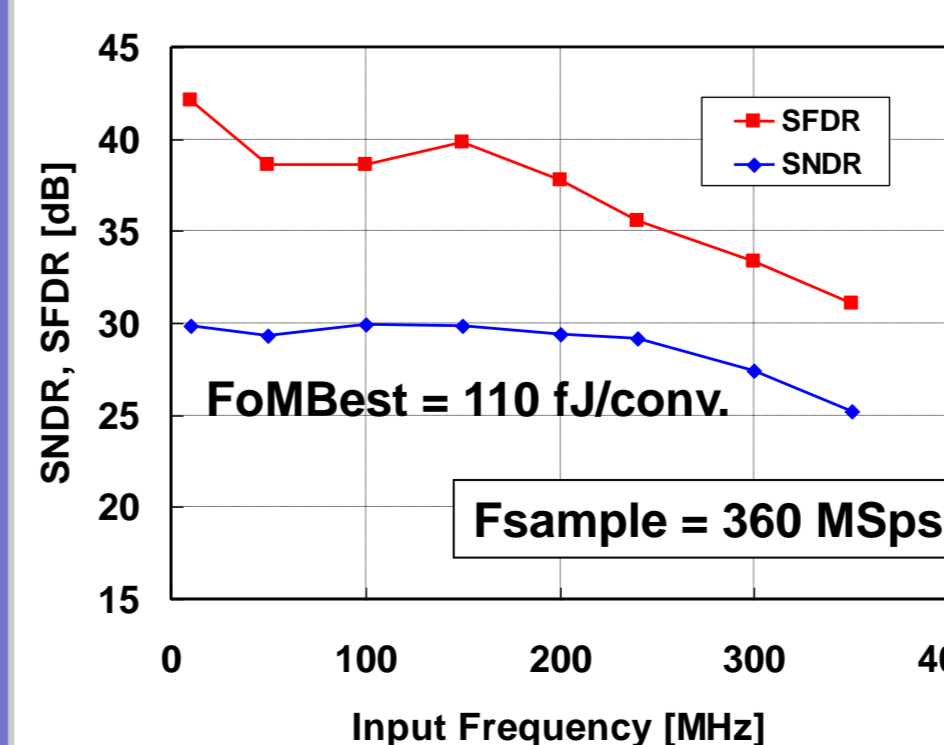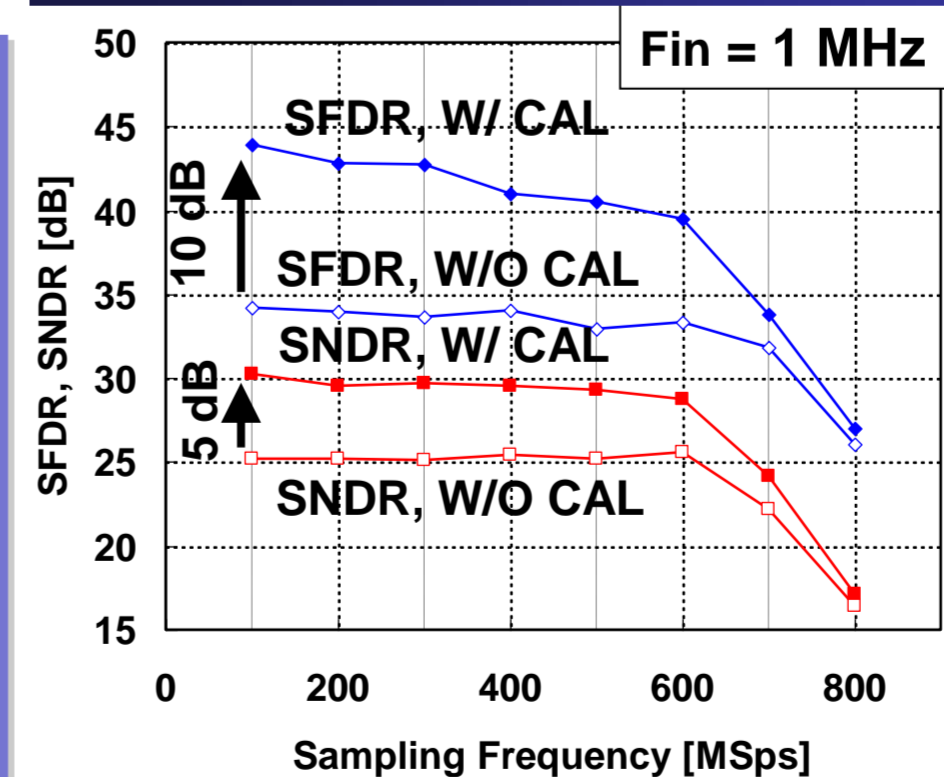|	no CAL	Cap CAL [1]	Proposed
$V_{off}(\sigma)$ [mV]	10.1	5.79	1.49
P_d [μW]	14.5	21.4	24.5
Delay [ps]	365	756	511

[1] V. Giannini, ISSCC2008

Overall Design

- 8 S/H circuits
  - Increase available input frequency
  - Allow flexible interface
  - Increase input capacitance, input swing current, and power dissipation
- 2-bit gate-interpolated comparators [2]
  - Reduce power consumption

320μm

260μm

- Up Down Counter 6b × 32
- Encoder & Error Correction
- Comparator × 32
- Sample & Hold × 9
- Bootstrap Driver × 10
- CLK generator
- DFF & ...

[2] Y. Asada, ASSCC2009

Measurement Results of the 5-bit ADC

Fin = 1 MHz

SFDR, W/ CAL
SFDR, W/O CAL
SNDR, W/ CAL
SNDR, W/O CAL

- ENOB
  (Effective Number of Bits)
  - 4.6 bits @ 600 MSps
- ERBW
  (Effective Resolution Bandwidth)
  - 200 MHz
- Effects of the cal.
  - Increase SNDR by 5 dB
- FoM
  (Figure of Merits)
  - 110 fJ/conv. @ 360 MSps
  - 160 fJ/conv. @ 600 MSps

FoMBest = 110 fJ/conv.

Fsample = 360 MSps