A Challenge to a 60GHz CMOS Wireless Transceiver for 40Gbps

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We are now trying to realize Multi-Gbps wireless communication using 60GHz carrier, and our group has already realized a 60-GHz direct-conversion transceiver, which can communicate at the IEEE802.15.3c full-rate for every 16QAM/8PSK/QPSK/BPSK mode. The maximum data rates with an antenna built in the package are 8Gbps in QPSK mode and 11Gbps in 16QAM mode within a BER of $< 10^{-3}$ [1]. In this presentation, some important circuit blocks are introduced, and the future 40Gbps front-end is also discussed, which can be theoretically realized by 64QAM with 4 channel bonding.

Fig. 1 shows circuit schematic of 60GHz low-noise amplifier[2]. As a low-noise amplifier, gain and noise figure are commonly important, and linearity and gain control are also important for wide dynamic range in communication distance. In addition, gain flatness becomes considerably important because the flatness has significant influence on ISI. The proposed LNA maintains the gain flatness and low-noise high-gain characteristic by asymmetric transistor and low-loss T-line as shown in Fig. 3.

Fig. 4 shows block diagram of 60GHz quadrature frequency synthesizer using the injection-lock technique [3]. Fig. 5 shows phase noise of locked state, and Fig. 2 and 6 show chip microphoto.

References

[1] K. Okada, *et al.*, "A 60-GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE802.15.3c," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2011.

[2] A. Musa, R. Murakami, T. Sato, W. Chiavipas, K. Okada, and A. Matsuzawa, "A 58-63.6GHz Quadrature PLL Frequency Synthesizer in 65nm CMOS," IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2010.

[3] N. Li, *et al.*, "A 24 dB Gain 51-68 GHz CMOS Low Noise Amplifier Using Asymmetric-Layout Transistors," IEEE European Solid-State Circuits Conference (ESSCIRC), pp.342-345, Sep. 2010.

TABLE I

PERFORMANCE COMPARISON

Reference	RFIC2008	JSSC2007	ESSCIRC2007	JSSC2007	ISSCC2008	VLSI2009	**This work[2]**
Technology	90 nm	90 nm	90 nm	90 nm	65 nm	90 nm	**65 nm**
Topology	CS	Cas.	Cas.	CS	Cas.	Cas.	**CS**
#stage	3	2	2	2	3	3	**4**
f_{center} [GHz]	58	58	64	63	60	63	**53**
Gain [dB]	15	14.6	15.5	12.2	19.3(diff)	20	**24**
NF [dB]	4.4	5.5	6.5	6.5	6.1	6.8	**4.0-7.6**
3dB BW [GHz]	56-61#	53.5-60.5#	60-68#	-	55-63#	56-70#	**51-68**
P_{DC} [mW]	3.9	24	86	10.5	35	36	**30**

Graphically estimated

TABLE II

PERFORMANCE COMPARISON

	This Work	[1]	[10]	[11]	[6]	[7]	[12]
CMOS Tech	65nm	45nm	130nm	130nm	90nm	90nm	130nm
Supply [V]	1.2	1.1	1.2	1.5	1.2	1.2	1.5/0.8
Ref. Frequency [MHz]	36	100	251.3	203.2	234	60	44.8~49.3
Frequency [GHz]	58 ~ 63	57 ~ 66	64.3 ~ 66.2	50.8 ~ 53	58 ~ 60.4	61 ~ 63	46 ~ 50.5
Phase Noise@1MHz [dBc/Hz]	**−96 (60.48GHz)**	−75	−84.1 6	−85.07	−85.1	−80	−72
Power Consumption [mW]	**77.5 (60.48GHz)**	78	72	87	80	78	57
Ref. Spur Level [dBc]	−67 ~ −58@20GHz	−42	−15.2	−59.88	−50.75	−49	−27
Division Ration	1620, 1680, 1740, 1800	512-8184	128	256	256/258	1024	1024
Output Type	**Quadrature**	Quadrature	Differential	Differential	Differential	Differential	Differential

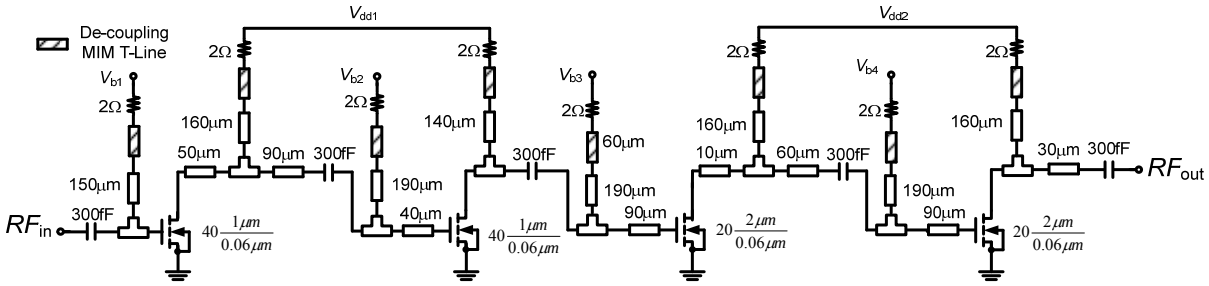

Fig.1: Schematic of 60GHz low-noise amplifier

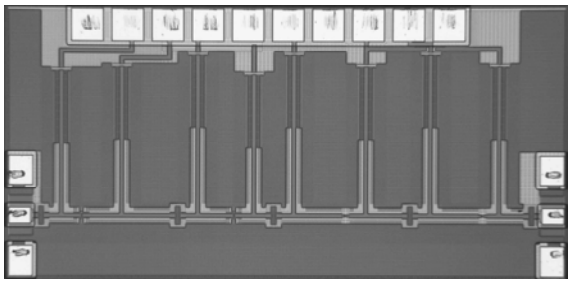

Fig.2: Chip microphoto of LNA

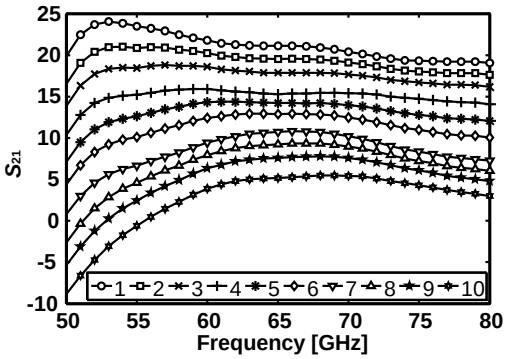

Fig.3: Gain control of LNA

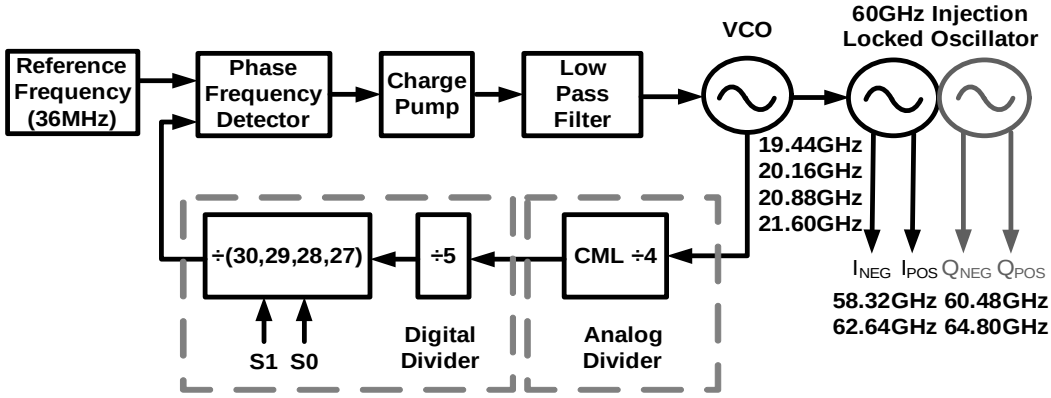

Fig.4: 60GHz Frequency synthesizer using quadrature injection-locked oscillator (QILO)

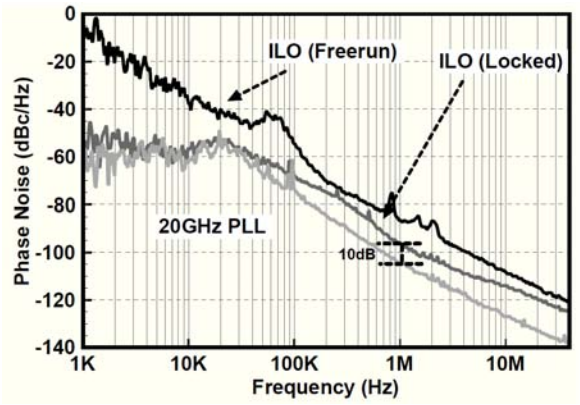

Fig.5: Phase noise of QILO

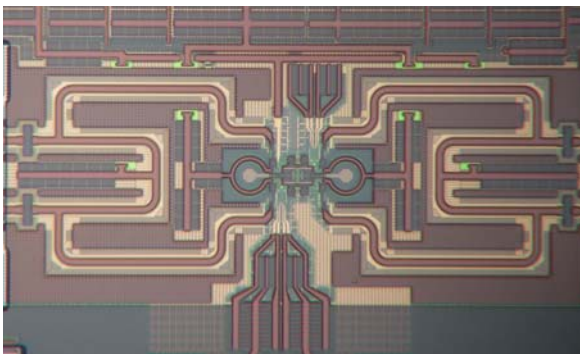

Fig.6: Chip microphoto of QILO