CMOS Device Modeling for Millimeter-Wave Power Amplifiers

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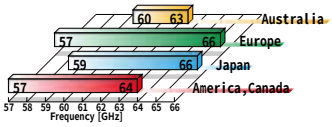
Conclusion

- The simulation results of the 1-stage PA and 4-stage PA are corresponded with the measurement results.
- Measurement results of the 4-stage PA : Gain 20.5 [dB], P_{1dB} 9.9 [dBm]

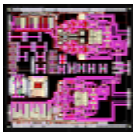
1. Background

- 60GHz band
A wide band can be used by unlicensed.
Using for the high-speed wireless communications in the short distance.

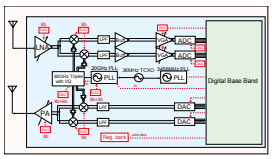


Utilizable bandwidth by unlicensed

- Design of RF frontend



Chip layout

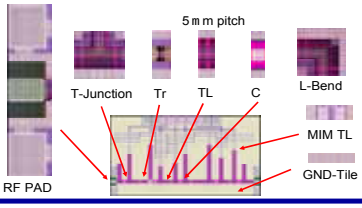


RF frontend block diagram

60GHz 2.16GHz-**full 4ch direct-conversion** by **CMOS**
QPSK 3.5Gbps & **16QAM 7Gbps & 64QAM 14Gbps**
IEEE 802.15.3c conformance
Dynamic power management: <300mW for RF front-end

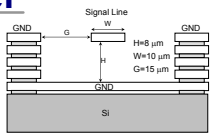
2. Approach to 60GHz CMOS robustness design

- Matching by transmission line
- In-house PDK based on measurement
- Tile-base layout

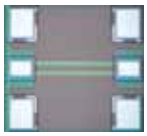


3. Transmission line model

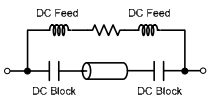
- Guided Micro-Strip Line was used for the transmission line.
- The model was made as α, β, Q value, and characteristic impedance Z_0 that showed the characteristic of the transmission line were corresponding.



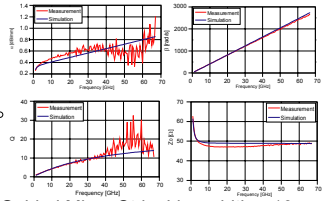
The structure of TL



Micrograph of TL



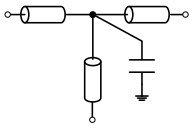
Model of TL



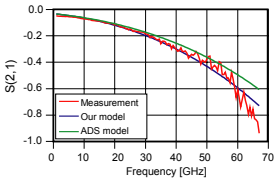
Guided Micro-Strip: Line width = 10 μm

4. T-junction model

T-jubction model is made from the measurement result.
Capacitance is added to the transmission line model.



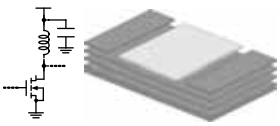
Model of T-junction



T-junction S(2,1)

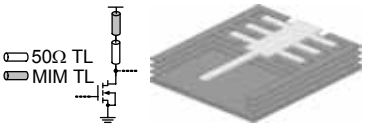
5. Decoupling capacitor model

Model at low frequency
- Planar unit
- Model as lumped parameter



Decoupling capacitor at low frequency

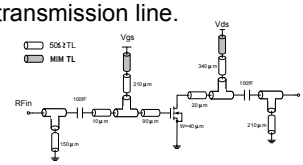
Model at millimeter waveband
- Interdigital type
- L and C are distributed and the resonance frequency is improved.
- Model as transmission line



Decoupling capacitor at millimeter waveband

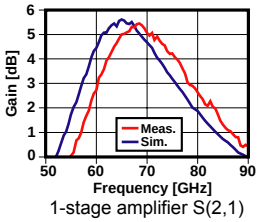
6. 1-stage PA

To verify the accuracy of the models, a 1-stage PA is fabricated by using the modeled transistor and transmission line.



Circuit of 1-stage amplifier

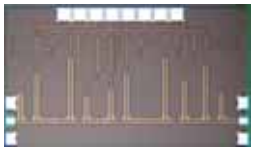
Micrograph of 1-stage amplifier



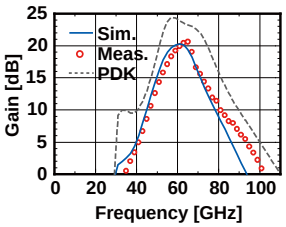
1-stage amplifier S(2,1)

7. 4-stage PA

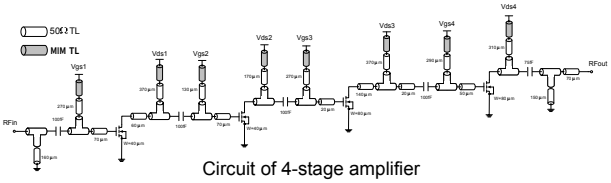
- The measurement results and the simulation result almost agree with each other.
- Measurement results of the 4-stage PA : Gain 20.5 [dB] P_{1dB} 9.9[dBm]



Micrograph of 4-stage amplifier



4-stage amplifier S(2,1)



Circuit of 4-stage amplifier

Performance summary

Reference	CMOS Node [nm]	Freq. [GHz]	Gain [dB]	P1dB [dBm]	PAE [%]	PDC [mW]	VDD [V]
[1] ISSCC 2009	65	60	15.8	2.5	3.95	43.5	1
[2] ISSCC 2009	45	60	13.8	11	-	-	1.1
This work	**65**	**61.5**	**20.5**	**9.9**	**6.68**	**144**	**1.2**

[1] W. L. Chan, *et al.*, ISSCC 2009 (IMEC) [2] K. Raczkowski, *et al.*, ISSCC2009 (Arizona Univ.)