A 6 bit, 7 mW, 250 fJ, 700 MS/s Subranging ADC

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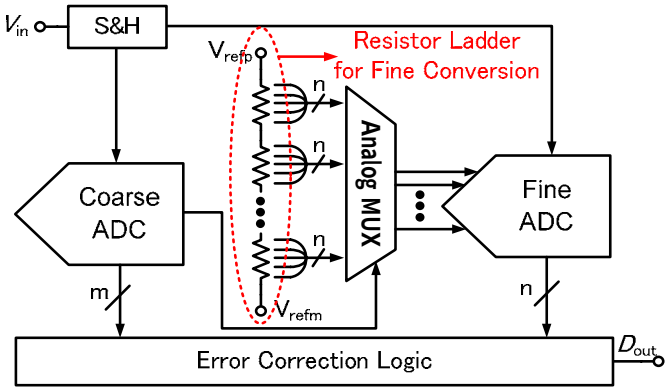
Motivation

- 6~7 bit, around 1 GS/s ADCs have many applications
  - Disk drive front-ends, ultra-wideband receivers
- Low power operation is most important issue for portable applications and green IT regulation

Problem of conventional topology

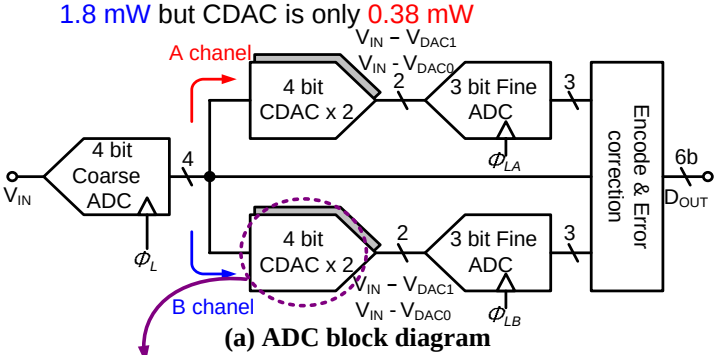
- Static power consumption in resistor ladder
- Large resistance causes settling problem
  → There is a trade-off between power consumption and settling time



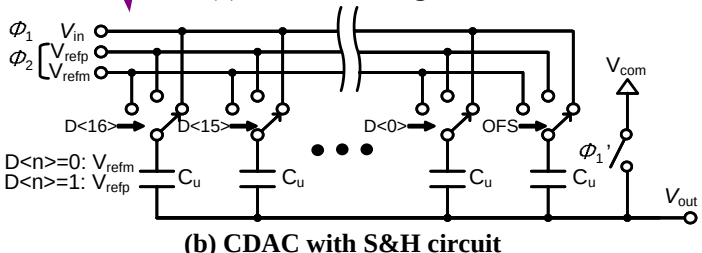
Block diagram of the conventional subranging ADC

Proposed ADC Architecture

- 4 b coarse stage and 3 b fine stage
  - Fine stage is interleaved to relax settling time
- CDAC with a S&H circuit achieves low power consumption and fast settling time
  - For 700 MS/s operation, RDAC consumes 1.8 mW but CDAC is only 0.38 mW



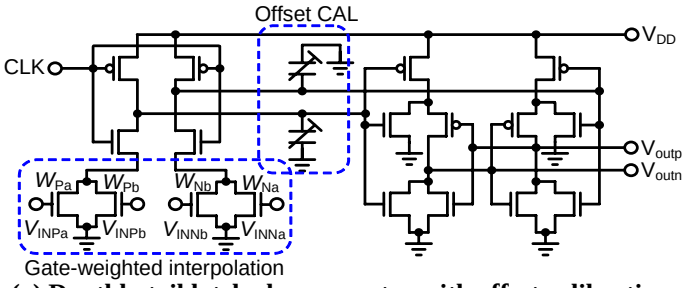
(a) ADC block diagram



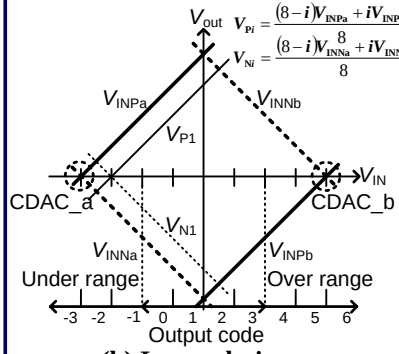
(b) CDAC with S&H circuit

Gate-weighted Interpolation

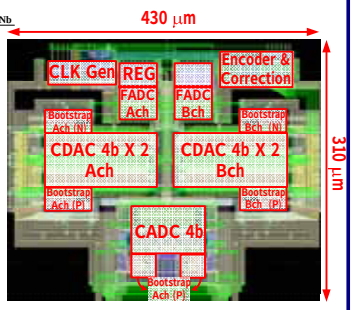
- Double-tail latched comparator is introduced for lower input noise
  - Capacitive calibration reduces offset to 0.9 mV at 1 σ
- Interpolation scheme reduces S&H circuits



(a) Doutble-tail latched comparator with offset calibration



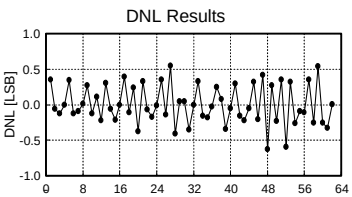
(b) Interpolation

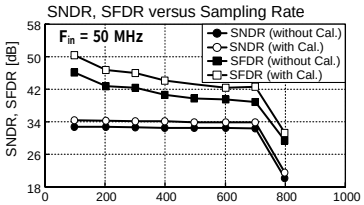


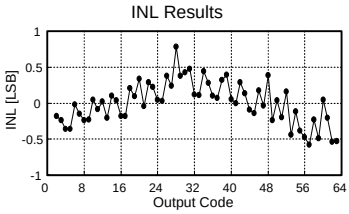
(c) ADC Layout

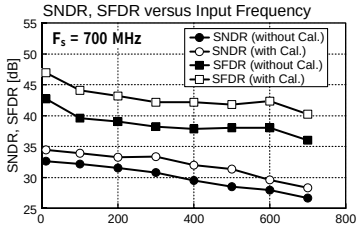
Measurement Results

- DNL and INL are less than +0.6/-0.6 and +0.8/-0.6, respectively
- SNDR keeps 34 dB until Nyquist at 700 MS/s









ADC Performance Table (6 bit)

Reference	Process [nm]	Sampling frequency [Gs/s]	Power dissipation [mW]	SNDR (DC/Nyq.) [dB]	FoM [pJ/conv.]	Active area [mm²]	Supply Voltage [V]	Architecture
ASSCC'08	130	1.2	75	34/33	2.17	0.43	1.2	Flash
ASSCC'08	130	0.7	24	31/30	1.31	0.052	1.2	Pipeline
ISSCC'08	130	1.25	32	34/28	1.22	0.09	1.2	2b-SAR
ASSCC'08	90	1	30	35/33	0.8	0.18	1.2/1.0	Subrange
This Work	**90**	**0.7**	**7**	**35/34**	**0.25**	**0.13**	**1.2**	**Subrange**

Matsuzawa & Okada Lab.