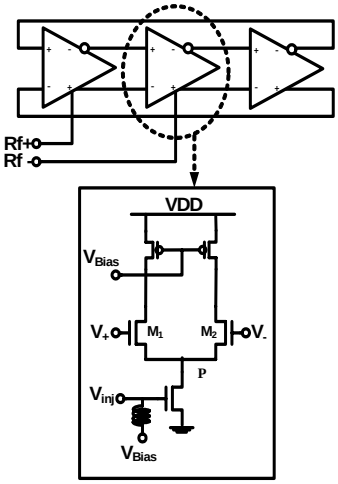
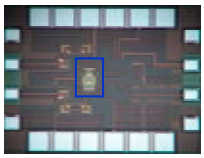
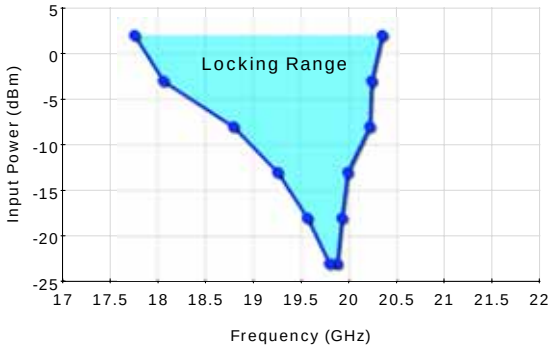
5 High Frequency Divider (ILFD)





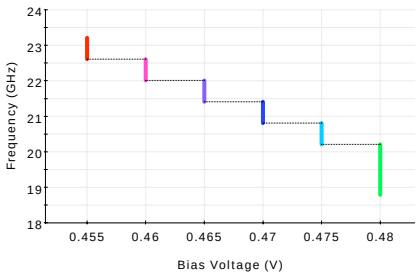
チップ写真

200um*
170um



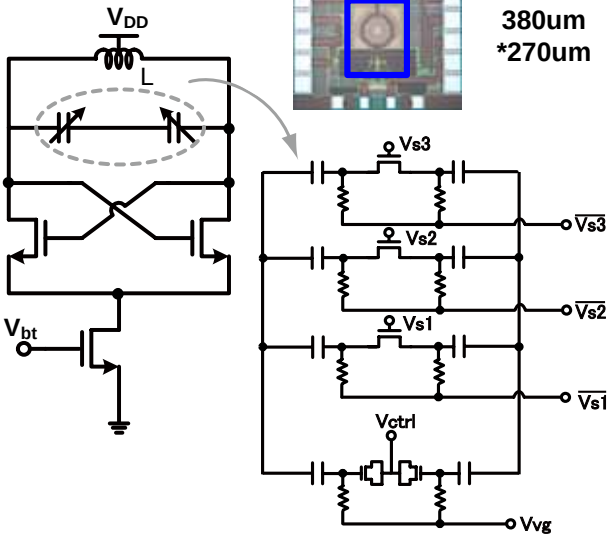
広いロックレンジをカバー

周波数に対応したバイアス電圧



	Simulation	Measurement
Process	65nm	65nm
Supply Voltage	1.2	1.2
Lock Range (GHz)	3	2.17
Total Lock Range	-	12 ~ 26.15 (GHz)
Free Running Freq. Range (GHz)	Less then 1 ~ 17	0.27 ~ 9.48
Current (Inc. Buffer)	5.7mA	6.8mA

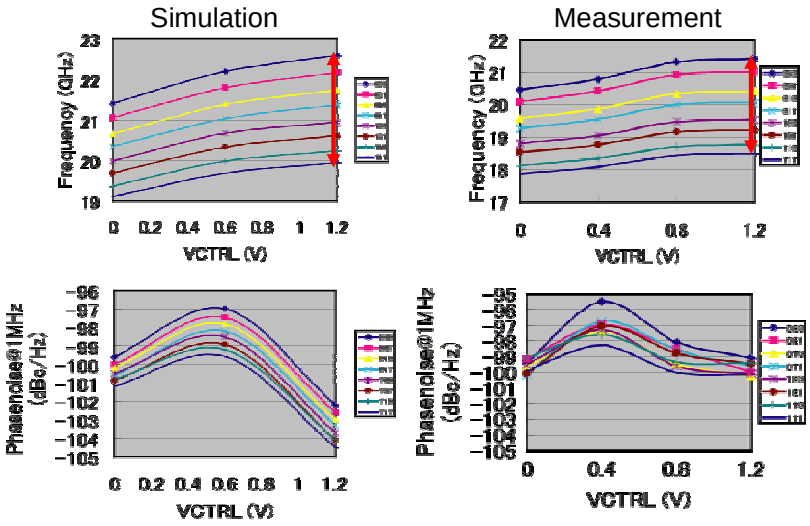
6 VCO



チップ写真

380um
*270um

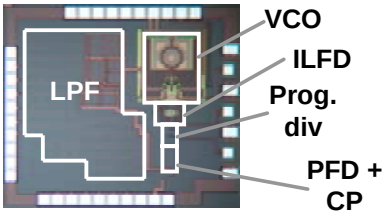
シミュレーションと実測結果の比較



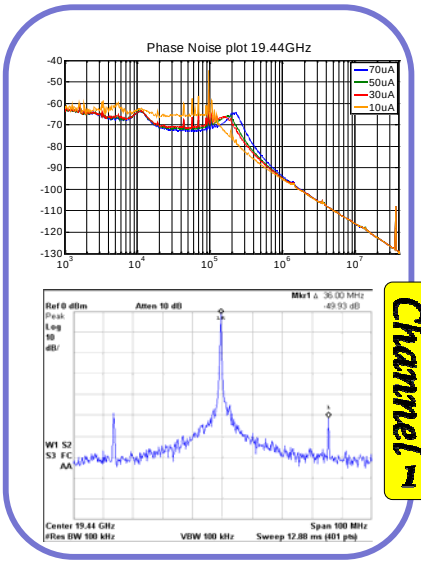
7 測定結果

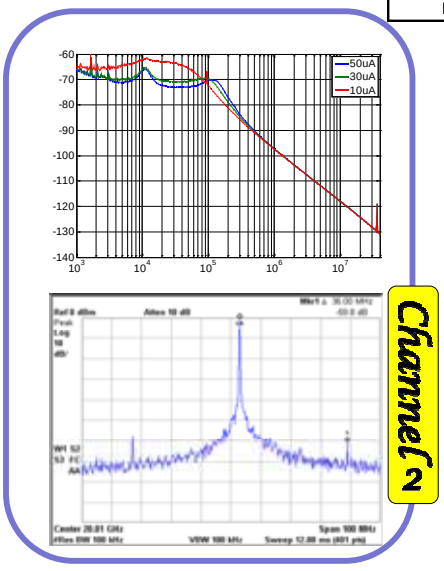
チップ写真

1350um*
1100um



	Sim/Cal	Measurement
VCO Freq (GHZ)	19 – 23 (19%)	17.8 – 21.4 (18.4%)
Freq. lock	19.44, 20.16, 20.88, 21.6	19.44, 20.16, 20.74 GHz
Ref. Spurs (dBc)	-71 to -51	-60 to -49
PN1MHz (dBc/Hz)	-95 to -100	-94 to -97
Total Power (mW)	58.8	88.8
Supply (v)	1.2	1.2
Process	65nm	65nm





高いQ値で発振させた20GHz信号をインジェクションすることによって，
PN=-97dBc/Hz
の低位相雑音な信号を出力

⇨ 4Gbps無線通信が可能

今後の課題

- このPLLに接続可能なILOの設計
- チューナブルにしているLPFやCPをスリム化し，最適化を図る．
- より広帯域な周波数で駆動させる．