Multi-Line De-Embedding Technique for Millimeter-Wave Circuit Design

Qing-Hong Bu, Ning Li, Naoki Takayama, Kenichi Okada and Akira Matsuzawa

Department of Physical Electronics, Tokyo Institute of Technology
2-12-1-S3-27 Ookayama, Meguro-ku, Tokyo, 152-8552, Japan.
Tel & Fax: +81-3-5734-3764, E-mail: buqh@ssc.pe.titech.ac.jp

1. Introduction

Device modeling becomes very important for millimeter wave (MMW) circuits design since the model provided by foundries are not accurate any more at MMW frequency. Test elementary group of passive and active devices including pads and interconnects for measurement have been implemented before circuits design. To obtain the characteristic of the device under test (DUT), a proper de-embedding method is required to eliminate the parasitics. Open short (OS) method have been widely used and the accuracy has been proved at low frequency [1], [2]. However, it becomes very difficult to realize ideal short with frequency increasing. Through-only is a simply method and has been verified up to 110 GHz [3]. Nevertheless, it is usually over de-embedding the DUT and the isolation between probes is not good sometimes since the distance is too short. A method by using two transmission lines with different length has been proposed [4]. It has been proved to be a very accurate method for de-embedding transmission line (Tline). However, large area is needed by using this method to de-embed different types of Tlines because two lines with different length are necessary for de-embedding each type of transmission lines. Cost becomes a severe problem especially when it comes to deep sub micron CMOS process such as 65 nm CMOS process. In this paper a simple method has been proposed for saving area. It has been verified that high accuracy up to MMW can be realized by using the proposed method.

2. De-embedding Method

Fig. 1 shows two Tlines of length l_1 and l_2 where $l_2 = 2l_1$. Both of the two transmission lines are symmetric and the measurements are reciprocal ($S_{21} = S_{21}$). The Tline can be decomposed into a cascade of 5 two-port networks consisting of the shunt parasitics of the pad, the intrinsic device and the series part of the pad. Therefore, the ABCD matrix of the Tline with a length of l_i can be represented as the following product:

$$F^t_{li} = F_{pl} F_{sl} F_{li} F_{sr} F_{pr} \tag{1}$$

where F^t_{li} represents the intrinsic line segment of structure ; F_{pl} and F_{sl} represents the parallel and serial parasitics of the left pad; F_{sr} and F_{pr} represents the serial and parallel parasitics of the right pad. We can have $F^t_{li} = F_{sl} F_{li} F_{sr}$ Then (1) can be simplified to

$$F^t_{li} = F_{pl} F'_{li} F_{pr} \tag{2}$$

The following parts will explain the de-embedding procedure in detail which is shown in Fig. 2.

Step 1) Calculate the Y-parameter of the l_1 Tline.

Multiplying F^t_{l2} with the inverse of F^t_{l1}, where l_2 is equal to $2l_1$. Using the method described in [4], the Y-parameter of the l_1 Tline can be expressed by

$$Y_{l2-l1} = \frac{Y^h_{l2-l1} + Swap(Y^h_{l2-l1})}{2} \tag{3}$$

where Y_{l2-l1} is the Y-parameter of the line segment of the length $l_2 - l_1$ for $l_2 = 2l_1$, then $Y_{l2-l1} = Y_{l1}$.

Step 2) Calculate the parallel parasitics of the pad.

By using the calculation result given by Step 1), the parallel parasitics of the pad can be expressed as

$$Y_p = \frac{Y^{Meas}_{l1} - Y_{l1}}{2} \tag{4}$$

$$Y_{sh} = \frac{Y_p(1,1) + Y_p(2,1) + Y_p(1,2) + Y_p(2,2)}{2} \tag{5}$$

where Y^{Meas}_{l1} is the measurement Y-parameter of the l_1 Tline and Y_{sh} is the shunt parasitics.

Step 3) Calculate the serial parasitics of the pad.

Firstly subtracting the parallel parasitics of the pad from the measurement Y-parameter of the l_1Tline,

$$Y'_{l1} = Y^{Meas}_{l1} - \{\{Y_{sh}, 0\}, \{0, Y_{sh}\}\} \tag{6}$$

Next subtracting the Z-parameter Z_{l1} in step 1) from the Z-parameter Z'_{l1} of step 3) and the serial part is shown as

$$Z_s = \frac{Z'_{l1} - Z_{l1}}{2} \tag{7}$$

The total de-embedding procedure can be implied as

$$Z_l = ytoz(Y^{Meas}_{l1} - \{\{Y_{sh}, 0\}, \{0, Y_{sh}\}\}) - 2Z_s \tag{8}$$

where *ytoz()* means the conversion from Y-parameter to Z-parameter.

3. Experimental Results

Two kinds of Tline have been implemented in CMOS 65 nm process. Slow-wave coplanar wave guide (SWCPW) transmission lines are employed to extract the parasitics of the pad. To verify the accuracy of the proposed method, CPW Tlines with two-layer metal ground have also been fabricated and de-embedded in different ways. The chip photo is shown in Fig.3. Fig. 4 shows that the OS de-embedding results have a large difference at high frequency which is supposed to be identical. The de-embedding results by using TO method and the proposed method are given in Fig. 5. It can be seen here that the characteristic impedances are matched very well for the 200µm and 400µm Tlines in both of the two methods. However, the attenuation and phase constant have large difference by the TO method. Although there are little difference for the frequency beyond 80 GHz, good match has been realized for the 200µm and 400µm Tline by the proposed method.

4. Conclusions

mi. In this method only one kind of Tline with different lengths is needed .One’ length is twice the other one’, therefore it can save chip area. By employing a 200μm and a 400μm Tline the parasitics of the pad can be calculated and modeled. Other types of Tlines can be de-embedded by eliminating the parasitics of the pad. Experimental results have shown the validity of this method up to MMW frequency.

Acknowledgements

This work was partially supported by MIC, MEXT, STARC, NEDO, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

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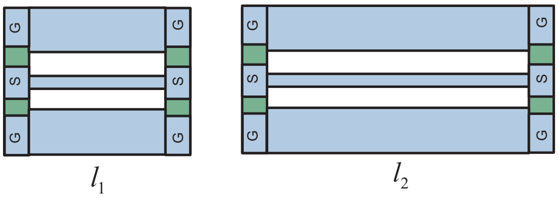


Fig.1.Test sture

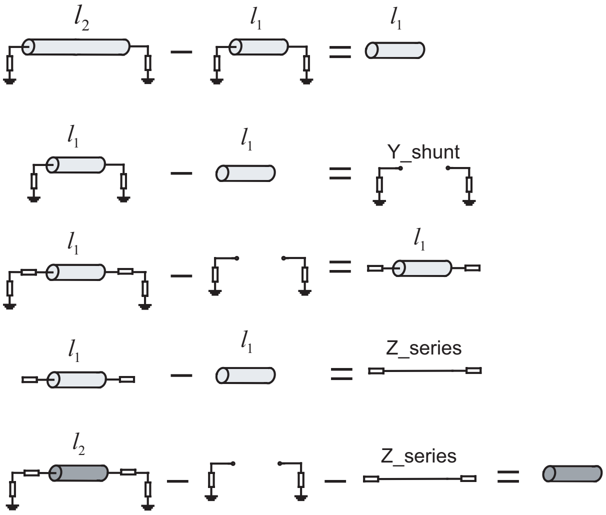


Fig.2. De-embedding procedure

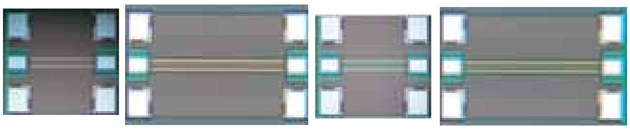


Fig.3. Photograph of the 200μm and 400μm transmission line

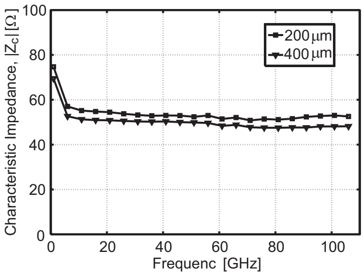
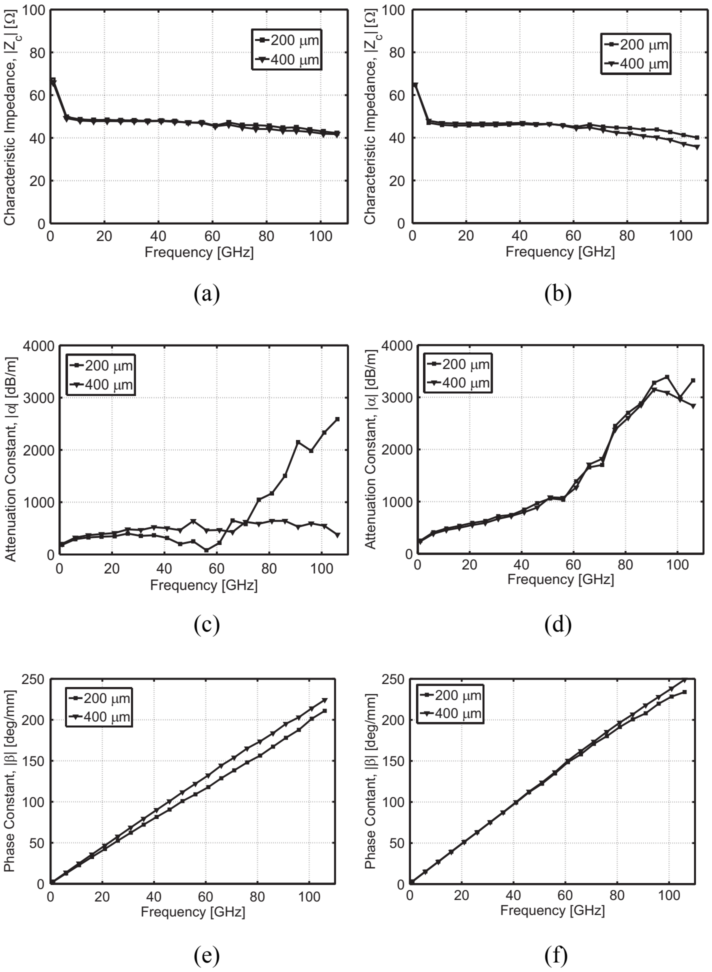


Fig.4. Open-shout de-embedding method for the characteristic impedance of 200μm and 400μm transmission lines



(a) (b)

(c) (d)

(e) (f)

Fig.5. Through-only and proposed de-embedding methods for the 200μm and 400μm transmission lines (a) Characteristic impedance of Through-only (b) Characteristic impedance of proposed (c) Attenuation constant of Though-only (d) Attenuation constant of proposed (e) Phase constant of Though-only (f) Phase constant of proposed