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PAPER Special Section on Analog Circuit Techniques and Related Topics

An 8-Bit 600-MSps Flash ADC Using Interpolating and Background Self-Calibrating Techniques

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SUMMARY This paper describes a flash ADC using interpolation (IP) and cyclic background self-calibrating techniques. The proposed IP technique that is cascade of capacitor IP and gate IP with dynamic double-tail latched comparator reduces non-linearity, power consumption, and occupied area. The cyclic background self-calibrating technique periodically suppresses offset mismatch voltages caused by static fluctuation and dynamic fluctuation due to temperature and supply voltage changes. The ADC has been fabricated in 90-nm 1P10M CMOS technology. Experimental results show that the ADC achieves SNDR of 6.07 bits without calibration and 6.74 bits with calibration up to 500 MHz input signal at sampling rate of 600 MSps. It dissipates 98.5 mW on 1.2-V supply. FoM is 1.54 pJ/conv.

key words: *analog-to-digital converter, cyclic background calibration, self-calibration, interpolation*

1. Introduction

A fixed wireless access (FWA), whose frequency band is around 38 GHz, is a communication system to transmit a huge amount of data. The targeting data transfer rate of the future FWA is about 1 Gbps and 16QAM or 64QAM will be used. Therefore, a required resolution of ADC is more than 7 bits and a conversion frequency higher than 500 MSps.

A sub-range type is a proper candidate for the specification, because it may operate at a few GHz and the number of components in the sub-range type is smaller than the other types. However, its settling time and timing skews between course and fine conversions will become significant bottlenecks when the operating frequency is getting higher. Considering that a bandwidth of the system is required to be wider in the near future, the flash-typed architecture is more appropriate for the future need.

This paper describes an 8-bit 600-MSps flash ADC fabricated in 90-nm process. Because of the minimum designable MOS channel length, a scaled process is suitable for the design of high speed ADCs; however, it reduces the maximum allowable supply voltage and signal swing, it also increases the mismatches of device. One of them is a threshold voltage mismatch of MOS transistors. The threshold voltage mismatch of MOS transistors is expressed as [1] and [2];

$$\Delta V_{\mathrm{th}} = \frac{q \cdot t_{\mathrm{ox}} \cdot \sqrt{2N \cdot t_{\mathrm{depl}}}}{\varepsilon_0 \cdot \varepsilon_{\mathrm{ox}} \cdot \sqrt{W \cdot L}} \propto \frac{t_{\mathrm{ox}}}{\sqrt{W \cdot L}} \sqrt[0.25]{N} \quad (1)$$

where t_{ox} is a gate oxide thickness, W is a MOS channel width, L is a MOS channel length, and N is doping density. Dimensions (t_{ox}, W, and L) of the MOS transistors are reduced by a scaling factor of S. However, the doping density, N, is increased by a factor of S or S^2 [3]. Therefore, the threshold voltage mismatch increases in the scaled process such that the conversion accuracy of an ADC is reduced. To overcome the trade-off between conversion frequency and accuracy of an ADC in a scaled process, this research implements cascade of interpolating techniques and a background calibration circuit in the ADC.

A flash architecture is known as the fastest architecture in ADC design. However this requires many components and occupies larger die size as resolution increases. As a result, a large die size limits conversion speeds of the flash ADC, because parasitic resistance and capacitance are proportional to the occupied area. Therefore, this paper proposes cascade of two conventional topologies, a capacitor type IP [4] and a MOS gate type IP [5], to reduce size and the number of components. As a result, design difficulty of circuit components is also mitigated.

2. ADC Architecture and Calibrating Method

2.1 ADC Architecture

The ADC architecture is shown in Fig. 1. The proposed architecture consists of amplifiers, capacitors for 1-bit IP, comparators executing 3-bit IP, resistor ladder producing reference voltages, and cyclic calibration logic. The cyclic logic selects compensated comparators in the background. The amplifiers are implemented in front of the comparators, because three sigma offset voltage (V_{offset} (σ) = 1.69 mV) of the comparators is larger than 0.25 LSB (~1 mV) [6].

Current consumed by the amplifiers should be determined by considering both a load capacitance and a thermal noise. The thermal noise can not be ignored under a small LSB. A simulation result shows that comparator's thermal noise, about 4.52×10^{-6} V^2, is larger than quantization noise, about 1.27×10^{-6} V^2. When one amplifier is connected to a comparator, the pre-amplifier is not able to suppress sufficiently the thermal noise of the comparator because an intrinsic gain of a MOS transistor is decreased in sub-micron processes [3], [7]. This means that the thermal noise caused

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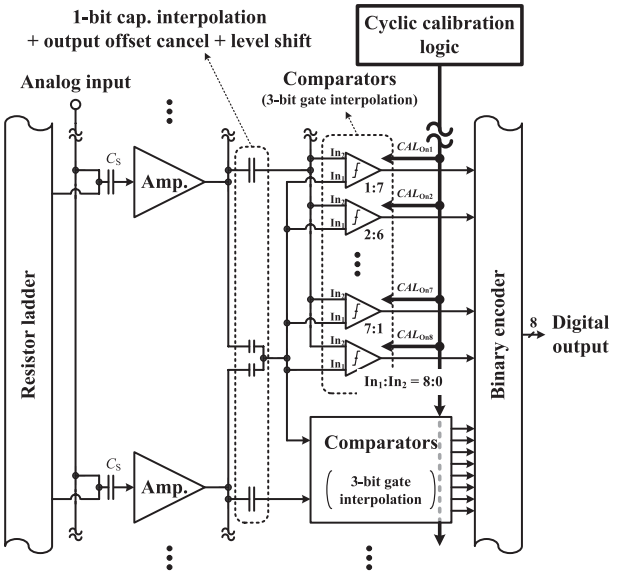

Fig. 1 ADC architecture.

by an amplifier cannot be ignored, although the amplifier decreases input-referred noise of the comparator. Increase of the current at the amplifier can be reduced the input-referred thermal noise, however it results in the increase of the whole current consumption in an ADC. Cascaded amplifiers may also be an alternative. However, added number of the amplifier increases power consumption and yields another thermal noise sources. Additionally, it complicates a clocking timing.

In this paper, one amplifier is connected to a number of comparators such that the input-referred thermal noise can be reduced without the increase of the whole current consumption in an ADC.

The input-referred thermal noise of an ADC is derived. Here, topology of the amplifier is considered as a fully differential type. A total thermal noise is mainly decided by the sampling capacitance, the amplifiers and the comparators.

$$\begin{aligned} v_{\text{th,total}}^2 &\approx 2\frac{kT}{C_\text{S}} + \left\{ v_{\text{th,amp}}^2 + \frac{v_{\text{th,comp}}^2}{G_\text{amp}^2} \right\} \times \left(\frac{C_\text{S} + C_{\text{P,amp}}}{C_\text{S}} \right)^2 \\ &= 2\frac{kT}{C_\text{S}} + \left\{ \frac{16kT \cdot \gamma \cdot V_\text{overdrive}}{3} \cdot \frac{\Delta f}{I_\text{DS}} + \frac{v_{\text{th,comp}}^2}{G_\text{amp}^2} \right\} \\ &\quad \left(1 + \frac{C_{\text{P,amp}}}{C_\text{S}} \right)^2 \end{aligned} \tag{2}$$

where $v_{\text{th,total}}^2$ is a input-referred total thermal noise, $v_{\text{th,amp}}^2$ is a thermal noise of the amplifier, $v_{\text{th,comp}}^2$ is a thermal noise of the comparator, G_amp is a gain of the amplifier, C_S is the sampling capacitance, $C_{\text{P,amp}}$ is a parasitic capacitance seen from an input of the amplifier, k is a Boltzmann constant, T is a temperature, γ is an excess noise factor, $V_\text{overdrive}$ ($= V_\text{GS} - V_\text{th}$) is an overdrive voltage of MOS transistors, I_DS is a half consuming current of the amplifier, and Δf is a noise bandwidth. Here, the noise bandwidth can be interpreted as a function of the I_DS.

$$\begin{aligned} \Delta f &= \frac{\pi}{2} \times Bandwidth \approx \frac{\pi}{2} \times \frac{1}{2\pi \cdot R_\text{out} \cdot C_\text{L}} \\ &\approx \frac{1}{2 \cdot G_\text{amp} \cdot V_\text{overdrive} \cdot C_\text{L}} \times I_\text{DS} \end{aligned} \tag{3}$$

where C_L means a load capacitance of the amplifier. In Eq. (3), it is assumed that consuming current, I_DS, is only determined by a response speed of the amplifier. The load capacitance is determined by the number of the comparators which are connected to an amplifier and output parasitic capacitance of an amplifier. And a signal attenuation caused by $C_{\text{P,amp}}$ also influences decision of the sampling capacitance. If $C_{\text{P,amp}}$ becomes small, C_S can be reduced. Consequently, a total input sampling capacitance also decreases. Similarly, If C_L becomes small, I_DS can be reduced. And $C_{\text{P,amp}}$ also decreases. Here, C_S and C_L are assumed to be proportional to the $C_{\text{P,amp}}$.

$$\begin{cases} C_{\text{P,amp}} \equiv \alpha_1 \cdot C_\text{S} \\ C_{\text{P,amp}} \equiv \alpha_2 \cdot C_\text{L} \end{cases} \tag{4}$$

where α_1, designable factor, is normally smaller than 1, and α_2 is almost decided by process. Substituting Eqs. (3) and (4) in Eq. (2), then

$$\begin{aligned} v_{\text{th,total}}^2 &\approx 2\frac{kT}{C_\text{L}} \times \frac{\alpha_1}{\alpha_2} + \left\{ \frac{8kT \cdot \gamma}{3G_\text{amp}} \cdot \frac{1}{C_\text{L}} + \frac{v_{\text{th,comp}}^2}{G_\text{amp}^2} \right\} \\ &\quad \times (1 + \alpha_1)^2 . \end{aligned} \tag{5}$$

As the bit number of the IP increases, the load capacitance of the amplifier, C_L, increases. The input-referred total noise therefore decreases, from Eq. (5). Consequently, the increased current dissipation of the amplifier suppresses the thermal noise. If the interpolating technique is unused, current of the amplifier should be increased inefficiently due to the thermal noise.

Thermal noise and the capacitor mismatch decide the minimum capacitance of the sampling capacitor. When each comparator has an amplifier, total sampling capacitance and power dissipation increase dramatically. However, by using the interpolating technique, the number of sampling capacitors and amplifiers can be reduced. For the ease of explanation, it is assumed that sampling capacitance is 10 fF, which is decided by design rule of the metal-insulator-metal (MIM) capacitor; thermal noise by sampling capacitance, 10 fF, reaches two third of quantization noise at room temperature. At an 8-bit flash, the total sampling capacitance is over 2.5 pF. Moreover, layout is burdened with too many MIM capacitors. Therefore, using an interpolating technique, total input capacitance is reduced to 1 pF and layout becomes eased. And the number of the amplifiers decreases from 255 to 19. Figure 2 shows component reduction by using the interpolating technique.

2.2 Cyclic Background Calibration

In 90-nm technology, the offset voltage of the comparators

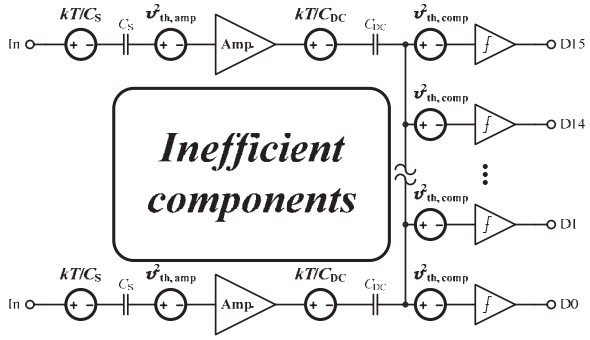

Fig. 2 Component reduction by using the IP (at 4-bit IP).

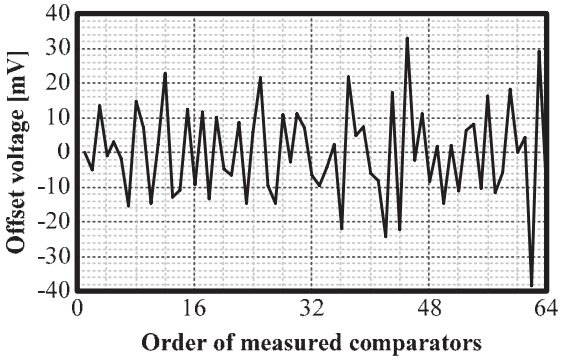

Fig. 3 Measured offset voltage of the 64 comparators which architecture is described in [6] (V_{offset} (σ) = 13.7 mV).

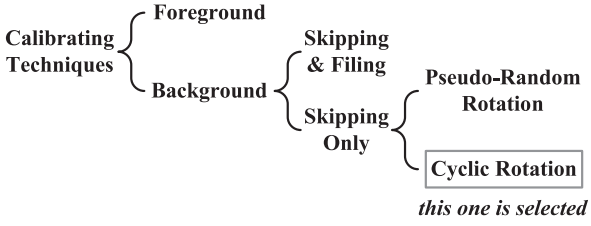

Fig. 4 Kinds of calibrating techniques.

may reaches 40 mV as shown in Fig. 3. This time invariant offset voltage is typically caused by device mismatch. Furthermore, time variant offset voltages, caused by; chip temperature change, and fluctuation of the supply voltage, can be an issue. To overcome these problems, we implement charge pump (CP) in the comparator [6], and compensate the offsets periodically in the background. As a result, offsets caused by device mismatch and time variant factors can be calibrated simultaneously.

Calibrating techniques are divided into foreground and background as shown in Fig. 4. Foreground is performed only when a circuit becomes powered up. Therefore, foreground cannot deal with temperature variation and supply voltage fluctuation. As a result, background calibration may be a practical mean.

For background calibration, a comparator under calibration cannot convert analog input into digital output. This unconverted data can be deduced from the data generated

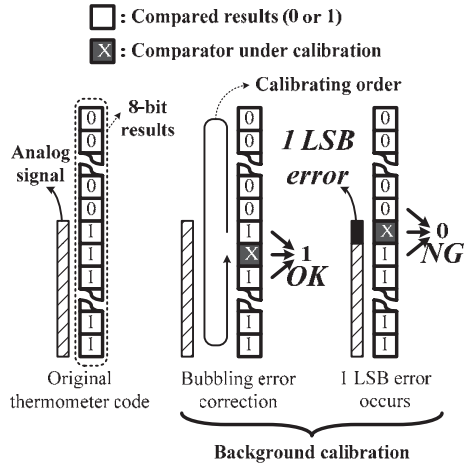

Fig. 5 Error occurrence and correction of the background calibration.

by neighboring comparators [8]. However, this complicates circuit design. Alternative method is skipping only method. The skipping only method causes bubbling error as shown in Fig. 5. This error is however corrected by the bubbling error correction technique [9]: the bubbling error is corrected, if compared results of neighboring comparators next to the comparator under calibration are the same. However, if the compared results of neighboring comparators are different, the skipped data becomes zero mandatorily.

In this research, cyclic background calibration is selected for circuit simplicity and small area, such that this may yield critical problem when frequency of an input signal is synchronized with the cyclic calibration frequency. A pseudo-random calibrating pattern may solve the synchronized trouble, though it may induce another problem. The problem is correlated to a calibrated time interval between one calibrating moment and the next calibrating moment on the same comparator. Because of the feature of the pseudo-random pattern, the time intervals of the every comparator are not the same. This means that converting points of each comparator fluctuate at different frequencies, because every compensated moment converting point of the comparator varies. Therefore, the pseudo-random method invokes different noise caused by calibration on each comparator. It may increase random noise of the ADC.

In the skipping only background self-calibration, if the number of simultaneously calibrated comparators is increased, the effective resolution is deteriorated. This causes a converting error and it can be considered as noise;

$$v_{\text{n,cal}}^2 = \frac{D}{2^N - 1} V_q^2 \tag{6}$$

where D is the number of the comparators compensated simultaneously, N is the resolution of the ADC, and V_q is the quantum voltages. If noise caused by the calibration is sufficiently smaller than the thermal noise, ENOB deterioration by the cyclic calibration can be ignored. Figure 6 shows how the number of simultaneously calibrated comparators deteriorates the signal-to-noise ratio (SNR). Therefore, we

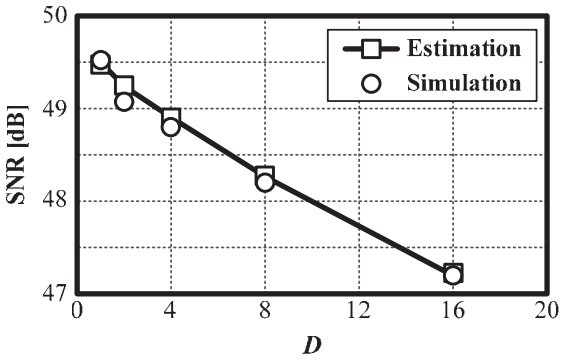

Fig. 6 SNR vs. the number of simultaneously calibrated comparators (D).

selected D of 4 in this ADC.

3. Comparator

3.1 Self-Calibration of Gate Interpolating Comparator

Figure 7 shows a double-tail latched comparator with gate IP and offset voltage compensation. The double-tail latched comparator is based on [10]. A distinct difference between [10] and this research is absence of an inverse latching clock. In [10], skew between direct and inverse latching clock is a bottleneck on performance of a comparator. This problem becomes more critical in high-speed ADCs. Therefore, this paper replaces the MOS transistor, which is for the inverse latching clock in [10], with two differential MOS transistors, which are M_{17} and M_{18} in Fig. 7. Performance of M_{17} and M_{18} are interlocked with the first stage of the comparator. Accordingly, the second stage is always latched after latching clock of the first stage becomes high. Figure 8 shows effect of the offset voltage compensation. From measurement results, V_{offset} (σ) decreases from 13.7 mV to 1.69 mV.

Calibration in comparators is conventionally conducted under a zero-crossing point of differential input signals. When this technique is applied to n-bit gate interpolating comparators, $2^n - 1$ reference voltages are needed. It is assumed that references of In_{p1}, In_{n1}, In_{p2}, and In_{n2} shown in Fig. 7 are V_{ref}, $-V_{\text{ref}}$, $(i+1)V_{\text{ref}}$, and $-(i+1)V_{\text{ref}}$, respectively. The input signals of the gate interpolating comparators are expressed as

$$\begin{cases} v_{\text{in,p1}} = v_{\text{in}} - i \cdot V_{\text{ref}} \\ v_{\text{in,n1}} = -(v_{\text{in}} - i \cdot V_{\text{ref}}) \end{cases}, \quad \text{and} \tag{7}$$

$$\begin{cases} v_{\text{in,p2}} = v_{\text{in}} - (i+1)\, V_{\text{ref}} \\ v_{\text{in,n2}} = -(v_{\text{in}} - (i+1)\, V_{\text{ref}}) \end{cases}. \tag{8}$$

Figure 9 shows 4 required signals, which are $\pm V_{\text{ref}} \times (2^n - x)/2^n$, $\pm V_{\text{ref}} \times x/2^n$, to execute x:$(2^n - x)$ IP at an n-bit IP. For the calibration of the x:$(2^n - x)$ interpolating comparator, these 4 signals are required. Consequently, 15-typed signals are necessary for the calibration under the conventional technique. Because input signals of the comparators are transferred from the amplifiers in this research, additional amplifiers are required for calibration.

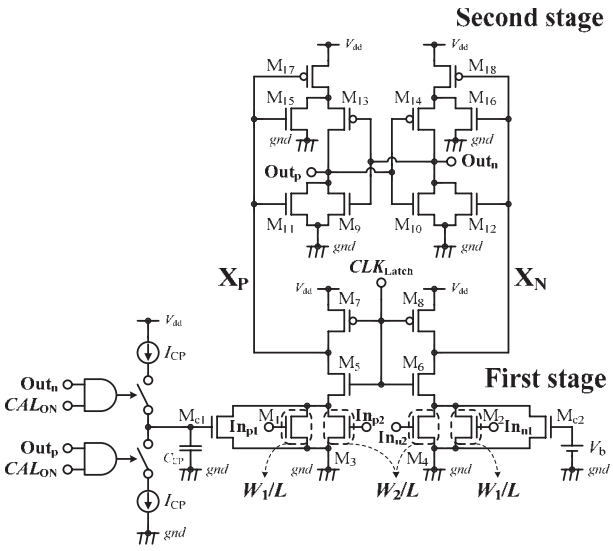

Fig. 7 The proposed gate interpolating and self-calibrating comparator.

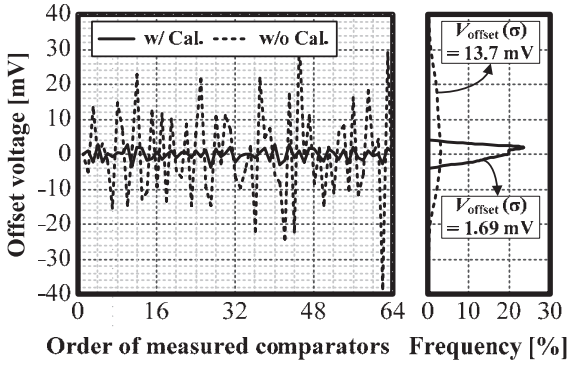

Fig. 8 Measured offset voltage of the 64 comparators with and without calibration (architecture of the comparator is [6]).

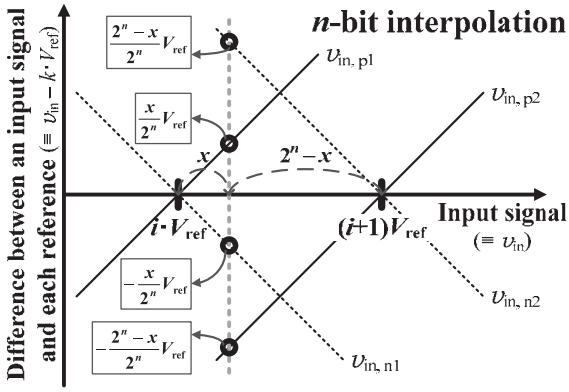

Fig. 9 Four required signals for x : $(2^n - x)$ IP between $i \cdot V_{\text{ref}}$ and $(i + 1)V_{\text{ref}}$ at an n-bit IP.

As a more practical calibrating technique, regardless of their interpolating ratios, comparators are calibrated while all input nodes are connected to an input common-mode

voltage. Here, relationship between drain currents and overdrive voltages in M_1, M_2, M_3, and M_4 in Fig. 7 is assumed to be constant;

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}). \quad (9)$$

In the comparators, the latch (second stage) regenerates the input signals by sensing voltage differences between node X_P and X_N in Fig. 7. Although drain voltages influence the drain currents, voltages of both sides (X_P, X_N) are the almost same at a zero-crossing point. The drain voltages affecting the compared results can be neglected.

Therefore, only gate voltages of the input MOS transistors are considered to influence the results as shown in Eq. (9′).

$$I_{DS} \approx \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (9')$$

However, the calibrating accuracy deteriorates in submicron process under the hypothesis. Carrier velocity saturation may be one of the causes. In short-channel MOS transistors, the carrier velocity is a function of an overdrive voltage, as expressed in [3];

$$\mu_n(eff) = \frac{\mu_{no}}{1 + \eta \cdot (V_{GS} - V_{th})} \quad (10)$$

where μ_{no} is the low-field surface electron mobility and η is an empirical coefficient. Equation (10) expresses that the carrier velocity is varied by an overdrive voltage. The carrier velocity on the input common-mode voltage is not equal to one on the zero-crossing point. Consequently, the proposed method is worse than the conventional method. However, the conventional method can be obtained under an ideal condition ignoring layout; it is not practical to connect 15-typed signal generated from amplifiers for calibration to each 8-bit comparator without any delay and voltage drop.

Monte Carlo simulation is performed to confirm the calibration effect. Some period is required before the calibration is activated, as shown in Fig. 10. After V_C approaches V'_{offset}, the offset voltage is measured. Figure 11 shows the effects of the proposed self-calibrating technique with regard to the mismatch. From the simulation results, the offset voltages of the proposed method are 2 or 3 times larger than that of conventional. However, since the offset voltages are small enough for the target, we use the method that 8 types of the gate interpolating comparators are compensated by using only one reference.

3.2 Gate Interpolation

3.2.1 Conventional Gate Interpolations

A general non-dynamic gate IP [11] type, which consumes static power, causes errors neglectfully. In the saturation region, the drain current of the MOS is

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{th})^{\alpha}(1 + \lambda V_{DS}) \quad (11)$$

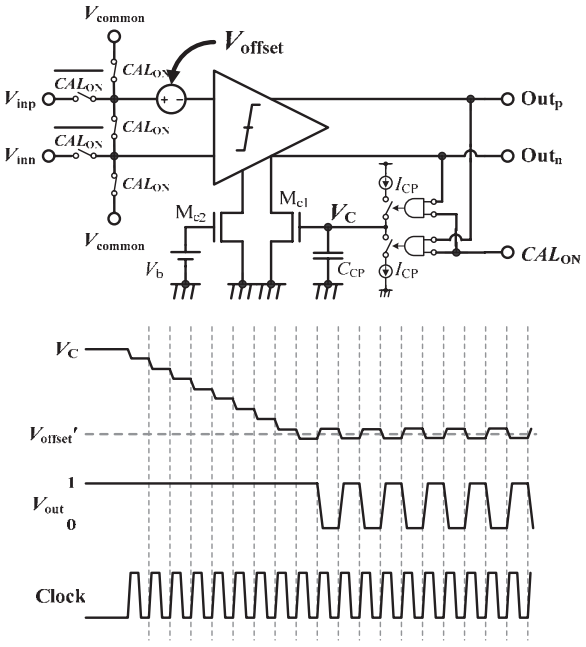

Fig. 10 Simulation method for confirming the calibration effect.

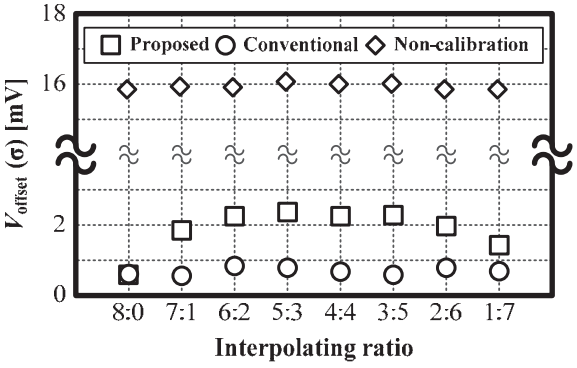

Fig. 11 Effects of the proposed self-calibration.

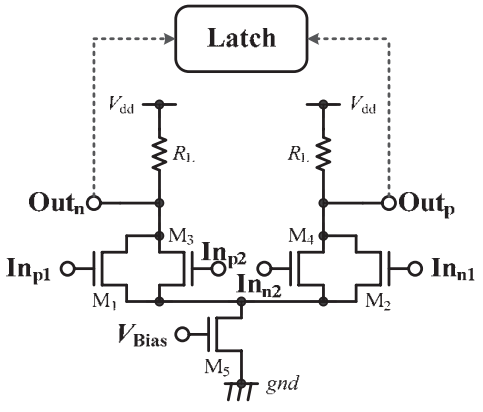

Fig. 12 Non-dynamic gate interpolation.

where α is from 1 to 2 [12]. Based on Eq. (11), errors in non-dynamic gate IP, shown in Fig. 12, are calculated and the result is shown in Fig. 13. When α is 1, the interpo-

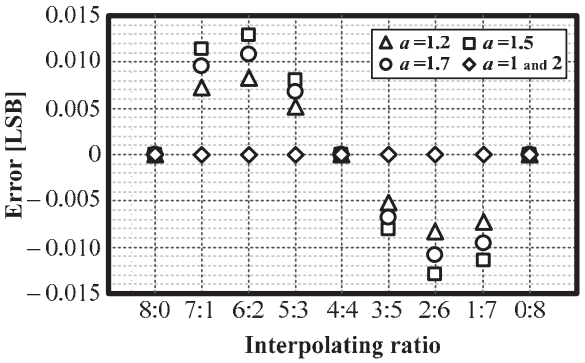

Fig. 13 Errors of the non-dynamic gate interpolation (calculation).

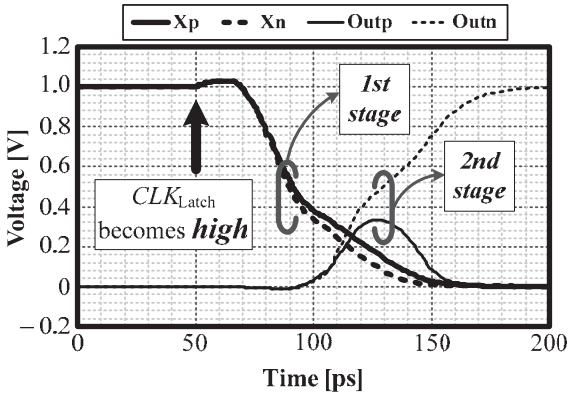

Fig. 14 Dynamic performance of the proposed comparator (simulation).

lated points are accurate. And when the α equals 2, induced current errors on the both sides, $\mathrm{Out_p}$ and $\mathrm{Out_n}$ in Fig. 12, are the same at the compared points, therefore the interpolated results are accurate. Although other α values cause errors, the amount is under 0.015 LSB. However, conventional interpolating technique dissipates powers unnecessarily, because comparison is only performed when the latching clock is high. Therefore, to realize more power-efficient gate IP, propose a gate interpolating dynamic comparator shown in Fig. 7. Power dissipation of the proposed 8-bit comparator was reduced 69% to 10.0 mW at 1 GSps and 1.0 V supply in the simulation, compared to 32.6 mW in the conventional non-dynamic performance. From this result, the dynamic comparator is more power-efficient than the non-dynamic type until conversion frequency reaches about 3 GSps.

The conventional dynamic gate IP [5] uses drain resistance of triode region. Accordingly, gate width of the interpolating MOS transistors should be wide, so as not to be saturated by dynamic current when latching clock is high. Input parasitic capacitance of the comparators and power dissipation of the amplifiers driving the parasitic capacitors will increase with gate widths. Moreover, high input signal level is also required to guarantee proper interpolating performances. However, in deep sub-micron process, this condition is impractical.

3.2.2 Input Signal Sensitivity of the Proposed Comparator

In the proposed one, IP accuracy may decrease compared with the non-dynamic gate IP due to dynamic characteristic inducing errors.

Before explaining the input signal sensitivity of the proposed comparator, we describe the dynamic performance of the proposed comparator briefly. As shown in Fig. 7, when CLK_{Latch} is low, $\mathrm{M_7}$ and $\mathrm{M_8}$ are on while $\mathrm{M_5}$ and $\mathrm{M_6}$ are off. Then parasitic capacitors on nodes $\mathrm{X_P}$ and $\mathrm{X_N}$ are charged to supply voltage. The second stage is turned off, because $\mathrm{M_{17}}$ and $\mathrm{M_{18}}$ are off. After CLK_{Latch} becomes high, $\mathrm{M_5}$ and $\mathrm{M_6}$ are on while $\mathrm{M_7}$ and $\mathrm{M_8}$ are off. Accordingly, electric charge on the node $\mathrm{X_P}$ and $\mathrm{X_N}$ flows into *gnd*. Drain currents of $\mathrm{M_5}$ and $\mathrm{M_6}$ are determined by input signals of $\mathrm{M_1}$–$\mathrm{M_4}$. Differences of flowing electric charge per time at the nodes $\mathrm{X_P}$ and $\mathrm{X_N}$ induces a voltage difference at the nodes, and the voltage difference becomes larger as time passes. This means that effect of the drain current difference is accumulated in dynamic comparators as time passes, while the effect of the drain current difference is maintained in non-dynamic comparators. If voltage on the node $\mathrm{X_P}$ and $\mathrm{X_N}$ drops sufficiently, then the second stage regenerates the voltage difference of node $\mathrm{X_P}$ and $\mathrm{X_N}$.

Next, we will explain input signal sensitivity of the proposed comparator. When the $\mathrm{X_P}$ and $\mathrm{X_N}$ reach specific voltages which are about 0.2 V under the 1.0-V supply voltage in the simulation as shown in Fig. 14, the second stage conducts regeneration. If the voltage difference is large, the regenerated result is more correct, because the second stage has large offsets. When the differential signal is inputted into the front-end of the comparator, output, $\mathrm{X_P}$ and $\mathrm{X_N}$ in Fig. 15, voltage difference of the low input dc level is larger than high input dc level. Because the difference on drain current, I_{p} and I_{n}, is decided by input signal components, and this is not changed distinctly rather than total current where input dc level is high or low. However, total current is large when the input dc level is high. Accordingly, output current signal proportion in the front-end becomes small. This decreases voltage difference of the output, $\mathrm{X_P}$ and $\mathrm{X_N}$ in Fig. 14, because output current signal accumulates voltage difference on the output parasitic capacitor, C_{PL} in Fig. 15. After the output voltages reach the specific voltage, the second stage regenerates this difference. As a result, it is that low dc level's front-end gain, ratio of output difference voltage to input differential voltage, is higher than high dc level's one. Consequently, the front-end gain of the proposed comparator is changed with the input signal magnitudes. This limits IP accuracy of the dynamic comparator.

The input signal sensitivity is briefly quantified. For simplicity, input signals of $\mathrm{In_{p1}}$ and $\mathrm{In_{p2}}$, in Fig. 7, are the same (same thing at $\mathrm{In_{n1}}$ and $\mathrm{In_{n2}}$ in Fig. 7). An output voltage of the front-end is expressed as

$$V_{\mathrm{out}}(t) = V_{\mathrm{dd}} - \frac{1}{C_{\mathrm{PL}}} \int I_{\mathrm{DS}}(t)\, dt$$
$$\xrightarrow{\text{if } I_{\mathrm{DS}} \text{ is constant}} V_{\mathrm{out}}(t) = V_{\mathrm{dd}} - \frac{I_{\mathrm{DS}} \cdot t}{C_{\mathrm{PL}}}. \quad (12)$$

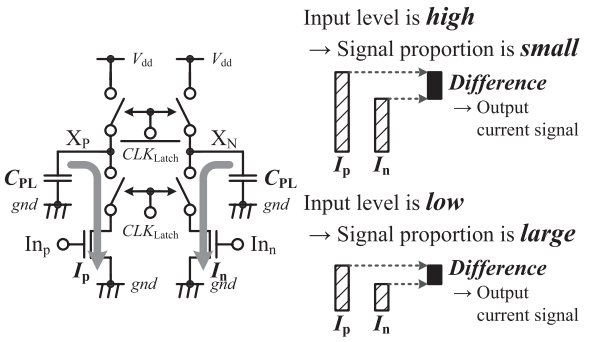

Fig. 15 Simplified schematic of the proposed comparator's front-end and drain current variation of input MOS transistors by input signals.

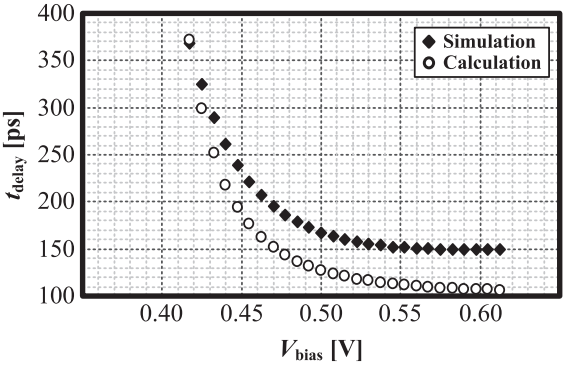

Fig. 16 Time delay caused by V_{bias} in the double-tail latched comparator. (V_{dd} = 1.0 V, ΔV = 0.9 V, v_{in} = 0.5 mV)

When an input common-mode voltage is V_{bias} and input signal is v_{in}, output voltage difference is expressed as

$$\Delta v_{out} = -2 \cdot \mu C_{OX} \frac{W}{L} (V_{bias} - V_{th}) \times \frac{v_{in} \cdot t}{C_{PL}} \tag{13}$$

where the gradual channel approximation is used for simplicity. Dividing Eq. (13) by t/C_{PL}, the differential output current signal is expressed as

$$\Delta i_{out} = -2 \cdot \mu C_{OX} \frac{W}{L} (V_{bias} - V_{th}) \times v_{in}. \tag{14}$$

When the input common-mode voltage, V_{bias}, reduces, total current of the front-end quadratically decreases, whereas signal current decreases linearly. Signal proportion of the drain current is consequently increased by decreasing the input common-mode voltage.

However, decreasing the input common-mode voltage increases time delay for the comparison. Using the gradual channel approximation and assuming the input signal, v_{in}, is small enough, tendency of the time delay, t_{delay}, is roughly calculated;

$$t_{delay} = \frac{2 \cdot (V_{dd} - V_{th}) \cdot C_{PL}}{\mu C_{OX} \frac{W}{L} (V_{bias} - V_{th})^2} + \frac{\tau}{A_{inv} - 1} \times \ln\left(\frac{\Delta V}{g_{m,M11}(t_1) \times r_{out,2nd}} \times \frac{(V_{bias} - V_{th})}{4 (V_{dd} - V_{th}) \times v_{in}} \right) \tag{15}$$

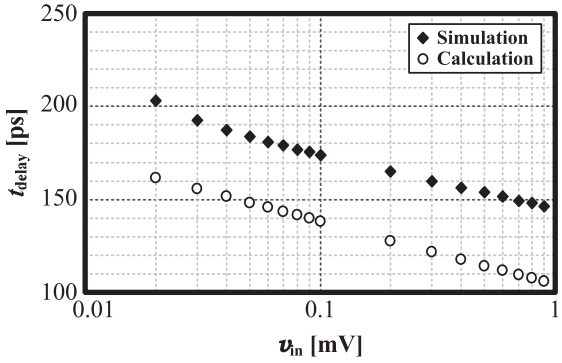

Fig. 17 Time delay caused by v_{in} in the double-tail latched comparator. (V_{dd} = 1.0 V, ΔV = 0.9 V, V_{bias} = 0.5 V)

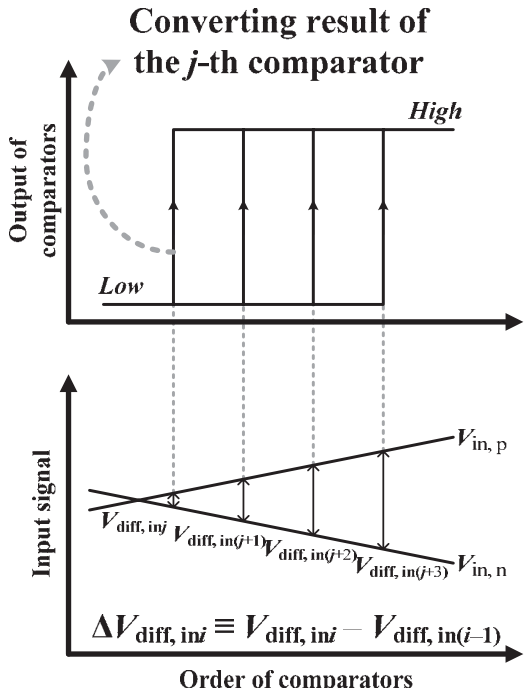

Fig. 18 Simulation method for confirmation of the dynamic conversion accuracy.

where ΔV is the voltage difference between the output voltages of the second stage, A_{inv} is the low-frequency gain of each inverter implemented in the second stage, τ is the time constant at the output node of each inverter, $g_{m,M11}$ is an transconductance of M_{11}(or M_{12}) in Fig. 7, $r_{out,2nd}$ is an output resistance of the second stage, and t_1 is time delay caused by the first stage. In Eq. (15), the first term indicates time delay in the first stage of the comparator, and the second term means time delay in the second stage of the comparator. From Eq. (15), as the input common-mode voltage, V_{bias}, decreases, the time delay increases to satisfy certain ΔV which may be threshold voltage of an SR-latch circuit. And as the input signal, v_{in}, decreases, the time delay also increases. Figures 16 and 17 compare Eq. (15) with the sim-

ulation results.

As shown in Fig. 18, the bit number of the dynamic gate IP is determined such that a difference of $V_{\mathrm{diff,in}i}$ and $V_{\mathrm{diff,in}(i-1)}$,

$$\Delta V_{\mathrm{diff,in}i} \equiv V_{\mathrm{diff,in}i} - V_{\mathrm{diff,in}(i-1)}, \tag{16}$$

does not change from ideal value while the dynamic gate IP induces no error.

From simulation results shown in Figs. 19, 20 and 21, a 3-bit dynamic gate IP induces error below 0.25 LSB over the PTV variation. However, simulation results indicate the IP does not satisfy 4-bit accuracy. Therefore, a 3-bit dynamic gate IP is used to satisfy the accuracy.

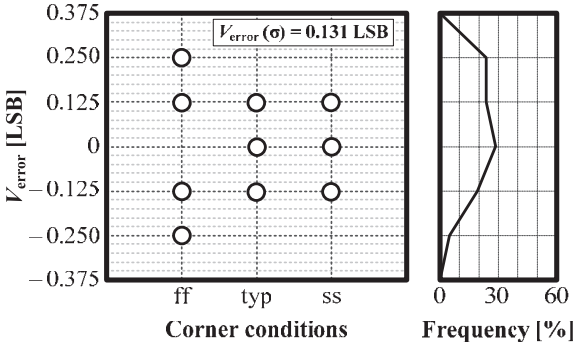

Fig. 19 Effects of process on the dynamic conversion accuracy (3-bit IP simulation when an input signal range is 64 mV).

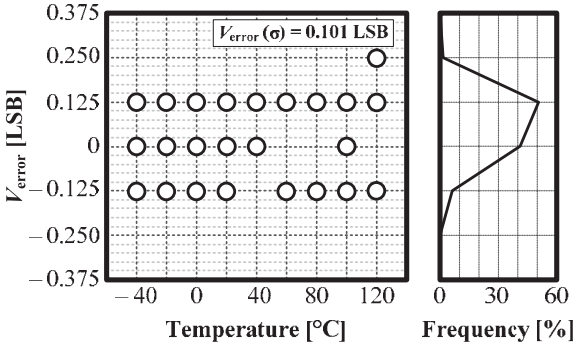

Fig. 20 Effects of temperature on the dynamic conversion accuracy (3-bit IP simulation when an input signal range is 64 mV).

3.2.3 Kick-Back Noise

The proposed comparator gives weight on gate width (W_1 and W_2 in Fig. 7) of the difference differential input MOS transistors in the comparators. The schematic of the comparator is basically based on [6], only the position of latching MOS transistors, M_5 and M_6 in Fig. 7, are changed. If the latching MOS transistors are implemented on the source of the input MOS transistors, $M_1 \sim M_4$, kick-back noise will deteriorate the output signals of the amplifiers.

When CLK_{Latch} is low, conventional front-end [6], shown in Fig. 22, charges parasitic capacitors, C_{P1} and C_{P2}, until the drain current of M_1 becomes almost 0. At that time, the threshold voltage of MOS, V_{th}, is charged between both terminals of C_{P2}, and upper plate of the C_{P1} becomes $V_{\mathrm{in}} - V_{\mathrm{th}}$. When latch signal goes high, electric charge on C_{P1} and the bottom plate of the C_{P2} is pulled down to *gnd*. Because of this, negative electric charge on the bottom plate of the C_{P2} increases. Increased negative charge drags the positive charge from the output of the amplifiers implemented in front of the comparators, and input nodes of the comparators are forced to be V_{th} whether the input signals are high or low. This mechanism induces kick-back noise. Kick-back noise is dependent upon the input signals, therefore it should be suppressed. From Fig. 23, influence on the input signal of the comparators can be expressed as the following equation:

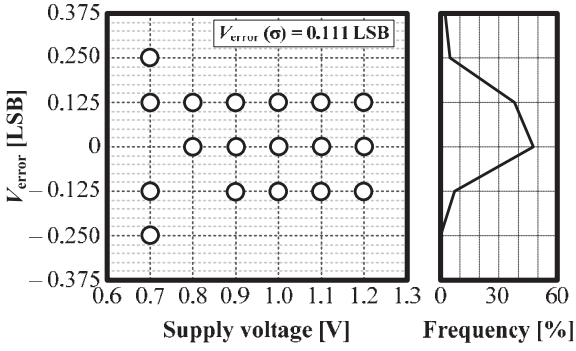

Fig. 21 Effects of supply voltage on the dynamic conversion accuracy (3-bit IP simulation when an input signal range is 64 mV).

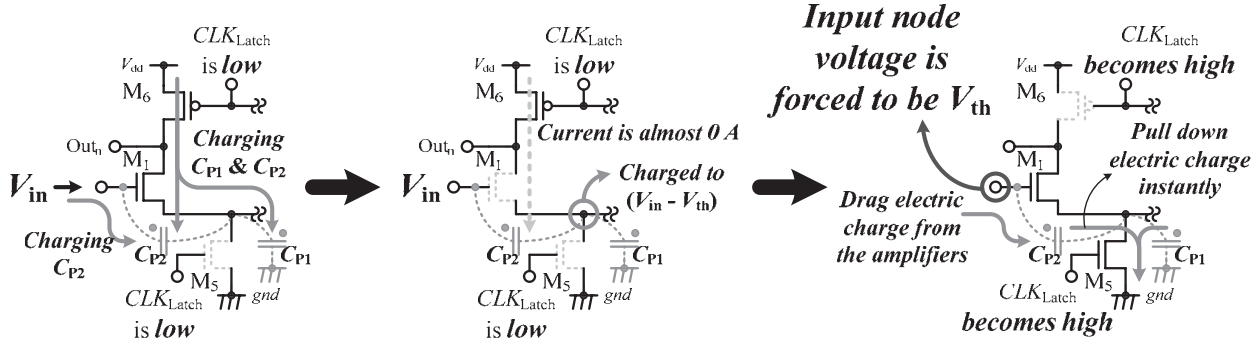

Fig. 22 Mechanism of the kick-back noise occurrence in the conventional front-end [6] (M_2, M_3, M_4, and M_7 are omitted).

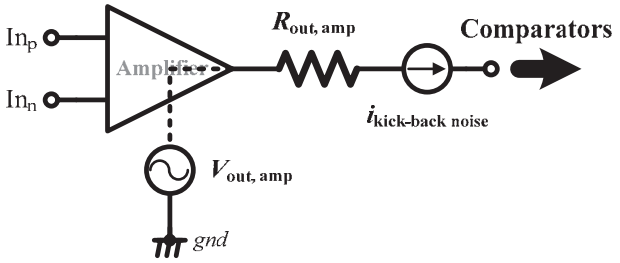

Fig. 23 Kick-back current and output resistance of an amplifier.

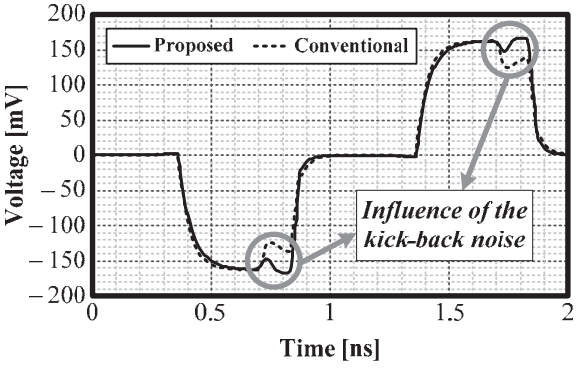

Fig. 24 Influence of the kick-back noise on differential signals (simulation).

$$V_{\text{out}} = V_{\text{out,amp}} - R_{\text{out,amp}} \times i_{\text{kick-back noise}} \tag{17}$$

where V_{out} is the input signal of the comparators, $V_{\text{out,amp}}$ is output signal of the amplifiers, $R_{\text{out,amp}}$ is output resistance of the amplifiers, and $i_{\text{kick-back noise}}$ is kick-back current from the comparators. Equation (17) shows that kick-back noise can be suppressed by reducing output resistance of the amplifiers or kick-back current. Therefore, we shift the latching MOS transistors to the drain of the input MOS transistors. Because the drain voltage is equal to the source voltage before CLK_{Latch} is high, the kick-back noise is suppressed to less than 15 mV in simulation. On the contrary, simulated kick-back noise reaches almost 40 mV in the conventional front-end type. The influence of kick-back noise on the proposed and conventional front-end is shown in Fig. 24.

4. Capacitor Interpolation and Amplifier

4.1 Capacitor Interpolation

Capacitors can average two output signals from the amplifiers [4]. This mitigates input range condition and decreases input parasitic capacitance of the comparators. Expected output signal voltage of the amplifiers is about 150 mV, and mismatch of the threshold voltage is the range of dozens mV. Therefore the input bias of the comparators is needed to be over hundreds of mV from the threshold voltage, if a 4-bit gate IP is selected. This is because input MOS transistors are required to perform in the saturation region. As shown in Fig. 25, the offsets of the comparators from thermal noise are become larger, when the input bias is increased. Therefore, excessive large gate interpolating bits degrade the noise performance of the comparators by its minimum allowable input bias point.

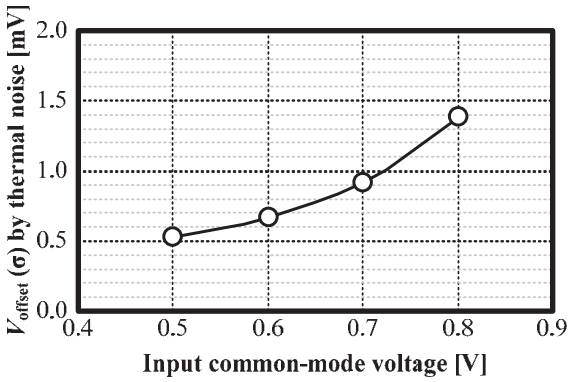

Fig. 25 Effects of input common-mode voltage on the thermal noise offset in the comparator (simulation).

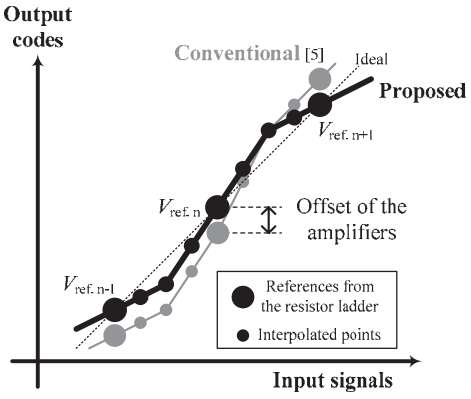

Fig. 26 Effects of the proposed interpolating architecture.

Furthermore, capacitors can remove the offsets of the amplifiers by using an output offset cancelling technique. In [5], the comparator is directly connected to the amplifier, as a result the comparator is sensitive to the offset of the amplifier. It is considered that magnitude of 1 LSB is large enough to neglect offset under a 7-bit resolution and 1.8-V supply. However, in this research, the offsets of the amplifier cannot be ignored. Therefore, by an output offset cancelling technique, we can suppress the offsets effectively. In simulation, V_{offset} (σ) is suppressed from 3.03 LSB to 0.0250 LSB.

Output voltage of the amplifiers and the desired input voltage of the comparators are not always equal. With the capacitors, two bias points can be separated successfully, therefore the input bias voltage of the comparators can be adjusted to their best performance point.

Figure 26 shows the effects of the proposed interpolating architecture. Let's consider compensating the offsets of the comparators successively, and then only distorted signals from the amplifiers cause converting errors. By using interpolating techniques, the distortion is distributed to the all 4-bit interpolated points, so that the differential nonlinearity (DNL) error is decreased. In contrast to [5], the

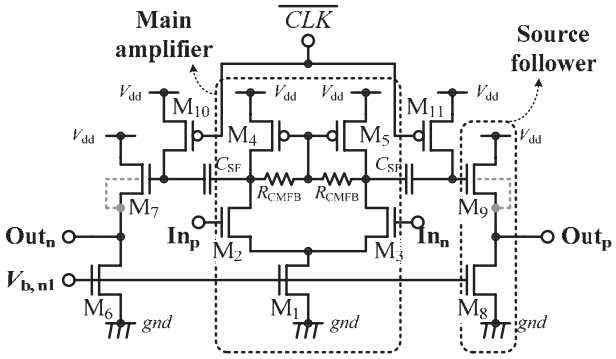

Fig. 27 Schematic of an amplifier.

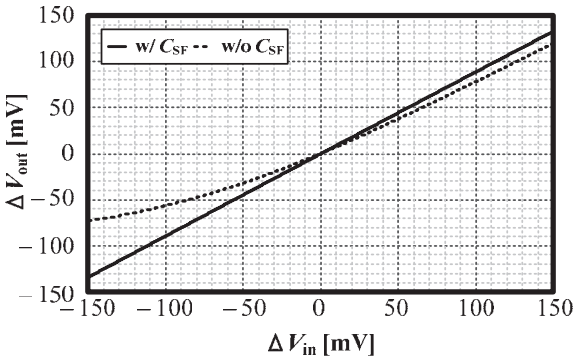

Fig. 28 Level shift effect of C_{SF} in a source follower.

offset of the amplifier is suppressed successfully in this research. Because of this, compared points of the references are fixed. Consequently, the integral non-linearity (INL) error is also suppressed.

4.2 Amplifier

From the simulation results shown in Fig. 11, the offset voltage (V_{offset} (σ)) of the comparator is 2.4 mV. Three sigma offset voltage is lager than 1 LSB ($\sim$ 4 mV), accordingly pre-amplifiers should be implemented.

As shown in Fig. 27, the basic topology of the amplifier is a cascade connection of a main amplifier and a source follower. The main amplifier is high gain with narrow bandwidth and the source follower is low gain with wide bandwidth, if static power dissipation and load capacitance are the same. The load capacitance of the entire amplifier is larger than input parasitic capacitance of the source follower. Therefore, more power is consumed, compared to the amplifier without the source follower. Furthermore, by using a source follower, input capacitance of the amplifier can be reduced. Since, input capacitance attenuates sampled signals, and attenuation is almost proportional to the power dissipation of the main amplifier, large load capacitance on the main amplifier deteriorates SNR.

Additionally, the small output resistance, $1/g_m$, of the source follower, will reduce the kick-back noise from the comparators.

In Fig. 27, a capacitor, C_{SF} is introduced between the main amplifier and the source follower. This separates the input bias of the source follower and the output bias of the main amplifier. The input node of the source follower is biased to be V_{dd} by M_{10} (or M_{11}) during the sampling period which means *CLK* in Fig. 27 is high. Therefore, the output signal linearity of the source follower is guaranteed. The output bias of the main amplifier is determined by resistor-typed common-mode feedback with a value of $V_{dd} - V_{GS,PMOS}$. Here, $V_{GS,PMOS}$ indicates gate-source voltage of the PMOS. And output bias of the source follower is $V_{in,SF} - V_{GS,NMOS}$, where $V_{in,SF}$ is the input voltage of the source follower and $V_{GS,NMOS}$ is the gate-source voltage of the NMOS. If the source follower is directly connected to the output of the main amplifier, output bias point, which value equals $V_{dd} - (V_{GS,PMOS} + V_{GS,NMOS})$, of the source follower becomes unacceptably low. This is because supply voltage is very low in a deep sub-micron process. Consequently, linearity of the source follower is deteriorated. Figure 28 shows linearity of the source follower with and without C_{SF}.

To reduce power dissipation of the amplifiers, an open loop circuit is selected. The open loop gain, G_{amp}, is sensitive to the mismatches of the MOS transistors. Without IP, gain mismatches between neighboring amplifiers occur no converting error. In this case, on the other hand, power dissipation of the total amplifiers is increased, because of the thermal noise requirement. To reduce power consumption, IP is adopted. However, the use of the interpolating technique mitigates the required gain accuracy. This is because if distorted gain ratios of neighboring amplifiers are the same, there is no error on interpolated points is caused. Mitigation of the gain mismatch is quantified under the condition that the output signal is linearly proportional to the input signal. This assumption is allowable because coefficients of above second-order terms are less than a thousandth of the coefficient of the first term, which indicates linear coefficient between the input signals and the output signals. Output signals of two interpolating amplifiers are expressed as

$$\begin{cases} v_{outp,A} = G_{amp}\,(v_{in} - i \cdot V_{ref}) \\ v_{outn,A} = -G_{amp}\,(v_{in} - i \cdot V_{ref}) \end{cases}, \quad \text{and} \tag{18}$$

$$\begin{cases} v_{outp,B} = G_{amp}\,(v_{in} - (i+1)\,V_{ref}) \\ v_{outn,B} = -G_{amp}\,(v_{in} - (i+1)\,V_{ref}) \end{cases} \tag{19}$$

where $i \cdot V_{ref}$ and $(i+1)V_{ref}$ are their reference voltages, and G_{amp} means a low-frequency gain of the amplifiers. Using Eqs. (18) and (19), error is calculated at $x{:}(2^n - x)$ interpolated point between $i \cdot V_{ref}$ and $(i+1)V_{ref}$, when G_{amp} is varied. $x{:}(2^n - x)$ IP is ideally performed when input signal becomes

$$v_{in} = i \cdot V_{ref} + \frac{x}{2^n} V_{ref}. \tag{20}$$

And the error, v_{error}, is expressed as

$$v_{error} = \frac{(2^n - x) \cdot v_{outp,A} + x \cdot v_{outp,B}}{2^n}$$

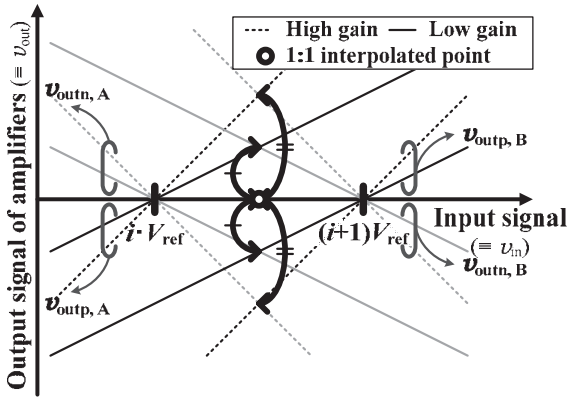

Fig. 29 Mitigating effect of the IP on gain accuracy.

$$-\frac{(2^n - x)\cdot v_{\text{outn,A}} + x \cdot v_{\text{outn,B}}}{2^n}. \tag{21}$$

Substituting Eqs. (18), (19) and (20) into Eq. (21), the error, v_{error}, is zero. Consequently, when mismatched low-frequency gains between neighboring amplifiers are the same, there is no error. Figure 29 describes this effect. However, when mismatched low-frequency gains of neighboring amplifiers are not the same, errors are occurred. To suppress the maximum error of the interpolated points to less than 0.25 LSB, three sigma of the low-frequency gain mismatch is required to satisfy

$$\frac{\Delta G_{\text{amp}}}{G_{\text{amp}}}(3\sigma) \le 2^{-n} \tag{22}$$

where n means the bit number of the IP.

5. Experimental Results

The 8-bit ADC was fabricated in 90-nm CMOS. Figure 30 shows a chip micrograph of the ADC which occupies 0.87 mm^2.

Figure 31 shows the measured ENOB with the background calibration. The ENOB reaches 7.0 bits, however as sampling frequency increases, the ENOB is decreased. At 662 MSps, the maximum ENOB is 6.36 bits with 10-MHz input frequency. The measured effective resolution bandwidth (ERBW) reaches 600 MHz. Shown in Fig. 32, the calibration increases SNDR by 4 dB. The FoM = *Power dissipation*/(2^{ENOB} × min(2× *ERBW*, *Sampling frequency*)) is 1.54 pJ/conversion-step at 600 MSps. The measured results as shown in Fig. 32 indicate that SNDR is not limited by SFDR. Distortion restricting SNDR may be caused by noise. The noise is related to the sampling capacitance, the CP, and background calibrating logic. Insufficient sampling capacitance may induce larger thermal noise and signal attenuation than the expected. And the CP may not be robust over noise. The background calibrating logic may yield noise during its performance.

The performance results of ADCs, whose designed resolution is above 7 bits, sampling frequency is higher than 600 MSps, and power dissipation is less than 100 mW, are

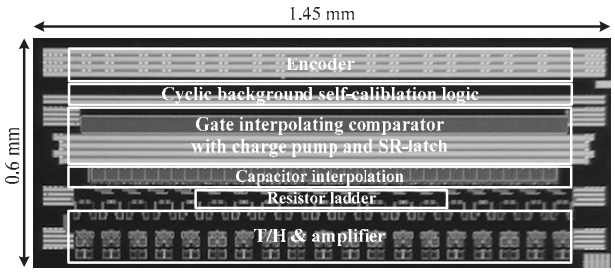

Fig. 30 Chip micrograph of the proposed ADC.

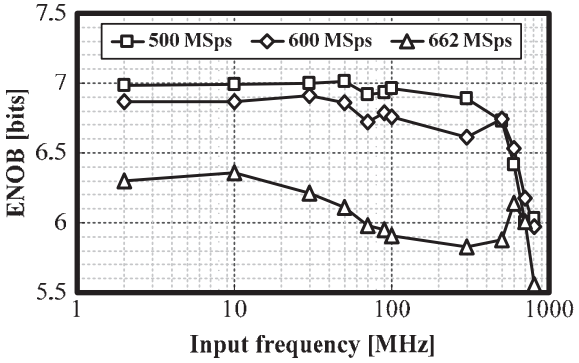

Fig. 31 Measured ENOB vs. input frequency (with calibration).

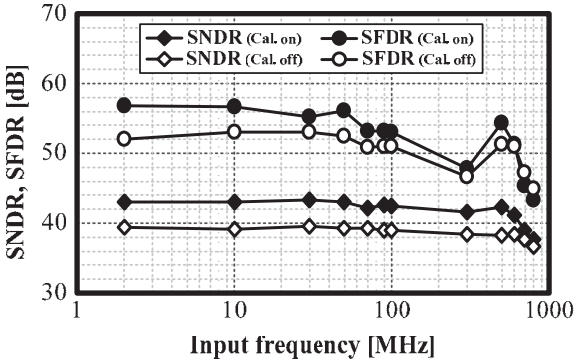

Fig. 32 Measured SNDR and SFDR vs. input frequency at 600 MSps.

summarized in Table 1. As shown in Table 1, an interleaving technique is mainly used over 600 MSps, however, [15], [18] and this work do not use interleave. Compared to [18], [18] outstrips the fabricated ADC except sampling frequency. In [15], the architecture is a sub-range and it is consist of coarse 4 bits and fine 4 bits, and the number of required comparators is 2^5. We use a flash-typed ADC, therefore the number of required comparators is 2^8 in this work. Accordingly, it is expected that power consumption of this work is 8 (=2^{8-5}) times larger than [15]. However, shown in Table 1, power consumption of this work is only 1.4 times larger than [15]. Consequently, the proposed interpolating technique decreases power dissipation effectively.

Table 1 ADC performance summary.

Reference	Process [nm]	Designed resolution [bits]	Sampling frequency [MSps]	Power dissipation [mW]	ENOB (DC/Nyquist) [bits]	FoM [fJ/conv.]	Area [mm^2]	Supply voltage [V]	Interleave
[13]	90	7	1100	46	6.52 / 5.52	910	0.19	1.3	used
[14]	65	8	800	30	7.65 / 7.05	280	0.12	1.2	used
[15]	90	8	770	70	7.18 / 6.67	940	0.605	1.2	unused
[16]	45	7	2500	50	5.85 / 5.40	480	1	1.1	used
[17]	130		600	30	7.47 / 7.02	340	1.1	1.2	used
[18]	90	10	500	55	8.99 / 8.49	300	0.49		unused
This work	90	8	600	98.6	6.87 / 6.74	1540	0.87	1.2	unused

6. Conclusions

This work proposes cyclic background self-calibration. The measurement results show an increase of SNDR by 4 dB with the calibration and a deterioration of ENOB caused by the background calibration, although negligibly small. Furthermore, proposed calibrating technique for a gate interpolating comparator can reduce the number of reference voltages to only one. In the comparator, we modify the position of the latching MOS transistors, which suppresses the kickback noise from 40 mV to 15 mV. Furthermore, the proposed interpolating topology, a cascade combination of the capacitor IP and the gate IP, suppresses DNL and INL errors, reduces power consumption, and decreases occupied area.

The fabricated ADC occupies 0.87-mm^2 die size, and has a maximum 7.0-bit ENOB at 500 MSps. The measured effective resolution bandwidth (ERBW) reaches 600 MHz. With calibration, SNDR is 4 dB higher than SNDR without calibration. The FoM attains 1.54 pJ/conversion-step at 600 MSps.

Acknowledgments

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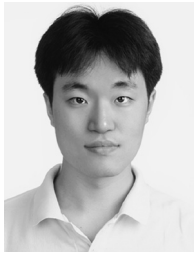

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