PAPER Special Section on Analog Circuit Techniques and Related Topics

Evaluation of a Multi-Line De-Embedding Technique up to 110 GHz for Millimeter-Wave CMOS Circuit Design

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SUMMARY An L-2L through-line de-embedding method has been verified up to millimeter wave frequency. The parasitics of the pad can be modeled from the L-2L through-line. Measurement results of the transmission lines and transistors can be de-embedded by subtracting the parasitic matrix of the pad. Therefore, the de-embedding patterns, which is used for modeling active and passive devices, decrease greatly and the chip area also decreases. A one-stage amplifier is firstly implemented for helping verifying the de-embedding results. After that a four-stage 60 GHz amplifier has been fabricated in CMOS 65 nm process. Experimental results show that the four-stage amplifier realizes an input matching better than −10.5 dB and an output matching better than −13 dB at 61 GHz. A small signal power gain of 16.4 dB and a 1 dB output compression point of 4.6 dBm are obtained with a DC current consumption of 128 mA from a 1.2 V power supply. The chip size is 1.5 mm × 0.85 mm.

key words: *CMOS amplifier, transmission line, millimeter wave, de-embedding, 60 GHz*

1. Introduction

Nowadays many publications about millimeter wave (MMW) transceivers and its building blocks have been published both from academia and industry [1]–[9]. According to IEEE 802.15.3c a 9 GHz wide-band at 60 GHz can be used without license for Gbps wireless applications such as wireless personal area network (WPAN), wireless high definition multimedia interface (HDMI), point to point links and so on. Accompanying with the scaling down of the CMOS technology, f_T and f_{max} of transistors are achieved above 100 GHz, making an all-CMOS solution at 60 GHz feasible. The merits of low cost compared with other technology such as GaAs and SiGe, and high integration of CMOS process make it a good candidate for the 60 GHz applications [10].

At MMW frequency device modeling becomes very important since the model provided by foundries are not accurate any more. Test elementary group (TEG) of passive and active devices including pads and interconnects for measurement have been implemented before circuits design. Transmission lines (T-line) are usually employed in matching network for firstly designing MMW circuits since it is scalable and can be easily modeled. The model of the T-lines will affect the simulation accuracy of the circuit therefore it is very important to model the T-line accurately.

To obtain the characteristics of the device under test (DUT), a proper de-embedding method is required to eliminate the parasitics. Open-short (OS) and open-short-through (OST) method have been often used and the accuracy has been proved at low frequency [11], [12]. But it becomes very difficult to realize an ideal short circuit at MMW frequency. Through-only de-embedding method is simple and has been verified up to 110 GHz [13]. In this method a through-pattern is implemented and measured. By using the measured S-parameter the parasitics of the pad can be calculated which is modeled as a π-type lumped constant circuit. However, in through-only method, the length of the through-line is required to be very short to match with the π-type lumped model. The isolation between the probes becomes a problem due to the coupling at MMW frequency, which makes the measurement becomes very difficult, especially for passive devices. A method by using two T-lines with different length has been explained in [14]. It has been proved to be a very accurate method for de-embedding the T-lines. But large chip area is required by using this method to de-embed different types of the T-lines because two lines with different length are needed for de-embedding each type of the T-lines. Cost becomes a severe problem especially for advanced CMOS process such as 65 nm process. An ideal through can be generated by an L-2L through-line method [15]. Therefore the parasitics of the pad can be calculated and modeled by using the π-type lumped model. And there is no requirement for the length of the through-line to be short. The isolation between the probes is not a problem any more by using this method. Although this method has been reported to de-embed interconnects under 10 GHz in [15]. The validity up to 110 GHz and applicability to other DUTs has been proved in this paper.

The structure of this paper is as follows: The detail of the de-embedding method is discussed in Sect. 2. Section 3 firstly describes the de-embedding results of the T-lines and the transistors, then a one-stage amplifier which is employed to verify the model. The implementation and measurement results of a four-stage amplifier are given in Sect. 4. Section 5 presents the final conclusion.

2. L-2L Through-Line De-Embedding Method

As shown in Fig. 1, two through-lines with a length of L and $2L$ have been utilized. The T-line can be decomposed into

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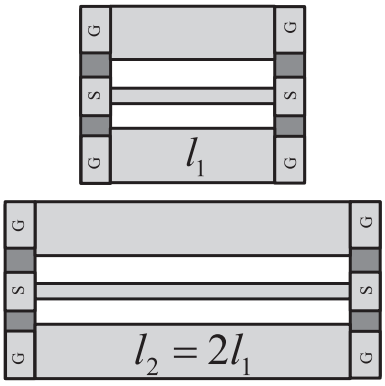


Fig. 1 L-2L through-line test structures.

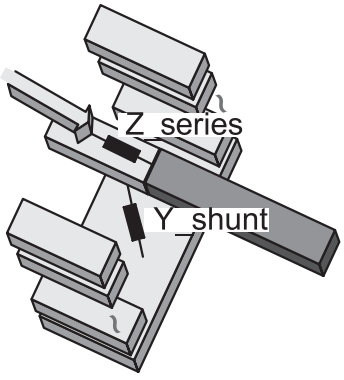


Fig. 2 Model of the PAD.

a cascade of five two-port networks consisting of the shunt parasitics of the pad, the intrinsic device and the series part of the pad as shown in Fig. 2. Therefore, the ABCD matrix of the T-line with a length of l_i can be represented as the following product:

$$T_{m_i} = T_{\rm pl} T_{\rm sl} T_{l_i} T_{\rm sr} T_{\rm pr} \tag{1}$$

where

T_{l_i} represents the intrinsic line segment of structure i;
$T_{\rm pl}$ represents the parallel parasitics of the left pad;
$T_{\rm sl}$ represents the serial parasitics of the left pad;
$T_{\rm sr}$ represents the serial parasitics of the right pad;
$T_{\rm pr}$ represents the parallel parasitics of the right pad.

Let $T_{\rm lpad} = T_{\rm pl} T_{\rm sl}$ and $T_{\rm rpad} = T_{\rm pr} T_{\rm sr}$ represent the parasitic matrix of the left pad and the right pad, respectively. With $l_2 = 2l_1$, we can have

$$T_{m_1} = T_{\rm lpad} T_{l_1} T_{\rm rpad} \tag{2}$$

$$T_{m_2} = T_{\rm lpad} T_{l_1} T_{l_1} T_{\rm rpad} \tag{3}$$

$$T_{\rm lpad} T_{\rm rpad} = T_{m_1} T_{m_2}^{-1} T_{m_1} = T_{\rm thru} \tag{4}$$

Converting $T_{\rm thru}$ to Y-parameter $Y_{\rm thru}$, the shunt parasitic and series parasitic can be expressed by

$$Y_{\rm shunt} = Y_{\rm pad}(1,1) + Y_{\rm pad}(1,2) \tag{5}$$

$$Z_{\rm series} = \frac{-1}{2Y_{\rm pad}(1,2)} \tag{6}$$

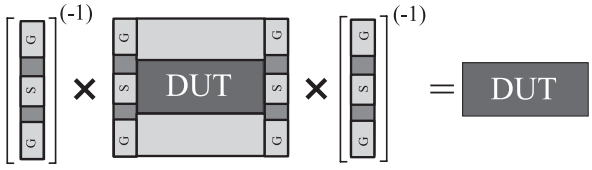


Fig. 3 L-2L De-embedding procedure.

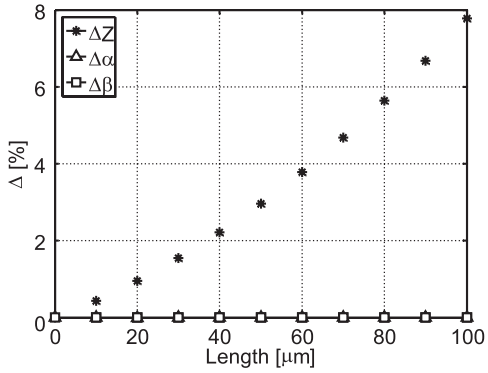


Fig. 4 Calculated results by using through-only method.

So the ABDC matrix of $T_{\rm p}$ and $T_{\rm s}$ is given by

$$\mathbf{T}_{\rm p} = \begin{pmatrix} 1 & 0 \\ Y_{\rm shunt} & 1 \end{pmatrix} \tag{7}$$

$$\mathbf{T}_{\rm s} = \begin{pmatrix} 1 & Z_{\rm series} \\ 0 & 1 \end{pmatrix} \tag{8}$$

and

$$\mathbf{T}_{\rm lpad} = T_{\rm p} T_{\rm s} = \begin{pmatrix} 1 & Z_{\rm series} \\ Y_{\rm shunt} & Y_{\rm shunt} Z_{\rm series} + 1 \end{pmatrix} \tag{9}$$

$$\mathbf{T}_{\rm rpad} = T_{\rm s} T_{\rm p} = \begin{pmatrix} Y_{\rm shunt} Z_{\rm series} + 1 & Z_{\rm series} \\ Y_{\rm shunt} & 1 \end{pmatrix} \tag{10}$$

$$\mathbf{T}_{\rm thru} = \begin{pmatrix} 2Y_{\rm shunt} Z_{\rm series} + 1 & 2Z_{\rm series} \\ 2Y_{\rm shunt}(Y_{\rm shunt} Z_{\rm series} + 1) & 2Y_{\rm shunt} Z_{\rm series} + 1 \end{pmatrix} \tag{11}$$

Therefore, the ABCD matrix of the DUT can be obtained by

$$T_{\rm dut} = T_{\rm lpad}^{-1} T_{\rm meas} T_{\rm rpad}^{-1} \tag{12}$$

Figure 3 shows the de-embedding procedure.

Through-only de-embedding method also models the parasitics of the pad by using lumped components. When the length of the through-line is zero for the ideal case, the result of through-only de-embedding method is the same as that of the L-2L through-line de-embedding method. However as the length becomes longer the error becomes remarkable to treat the through-line as a lumped component. A T-line is de-embedded to evaluate the accuracy of the through-only de-embedding method. The characteristic impedance $Z_{\rm c}$, attenuation constant α and phase constant β of the T-line have been calculated with the length change of the through-line. The calculation result is shown in Fig. 4. The error term Δ is given by

$$\Delta = \left| \frac{X^{L-2l} - X^L}{X^L} \right| \tag{13}$$

where L is the length of the de-embedded T-line and l half of the length of the through-line. X^L is the de-embedded results when $l = 0$. Term X represents the characteristics impedance Z_c, attenuation constant α and phase constant β of a T-line. The value of L, Z_c^L, α^L and β^L are 400 μm, 45 Ω, 1 dB/mm and 114.5 deg/mm, respectively. Figure 4 shows that $\Delta\alpha$ and $\Delta\beta$ is zero while the error term ΔZ_c increases as l increasing and has a 3% difference when l is 50 μm. The detail of the calculation is given in the Appendix.

3. De-Embedding Experimental Results

3.1 Transmission Lines De-Embedding

Two kinds of T-lines have been implemented in CMOS 65 nm process. The structure of the T-lines is shown in Fig. 5. Slow-wave coplanar waveguide (SWCPW) T-lines use Metal 1 as shield. Due to the design rule Metal 1 can not shield the substrate totally. CPWs with two-metal ground T-lines use Metal 1 and Metal 2 as shield. Metal 1 and Metal 2 are interleaved in parallel with the waveguide metal and connected in the direction perpendicular to the waveguide metal, which shield the substrate totally. SWCPW T-lines are employed to extract the parasitics of the pad by using the L-2L through-line method. After the pad is modeled, CPWs with two-metal ground have been de-embedded by eliminating the parasitics of the pad. The chip micrograph of the T-lines is shown in Fig. 6. De-embedding has been carried out in different ways for comparing. By using the method specified in [16] the characteristics of the CPWs with two-metal ground can be calculated from the S-parameters. Figure 7 shows the de-embedded result by using the OS de-embedding method. As can be seen, the characteristic impedance Z_0 has a large difference at high frequency which are supposed to be identical. The de-embedding results by using through-only method are given in Fig. 8. As shown that the characteristic impedance and phase constant are matched very well for 200-μm and 400-μm CPWs with two-metal ground. However, the attenuation have large difference beyond 20 GHz. The reason is considered as the coupling between the probes since the length of the through pattern is only 40 μm. Figure 9 gives the de-embedded results by using the L-2L through-line method. Although there is little difference when the frequency is beyond 80 GHz, good matches have been realized for the 200-μm and 400-μm T-lines. Therefore the T-lines can be modeled accurately based on the de-embedding results.

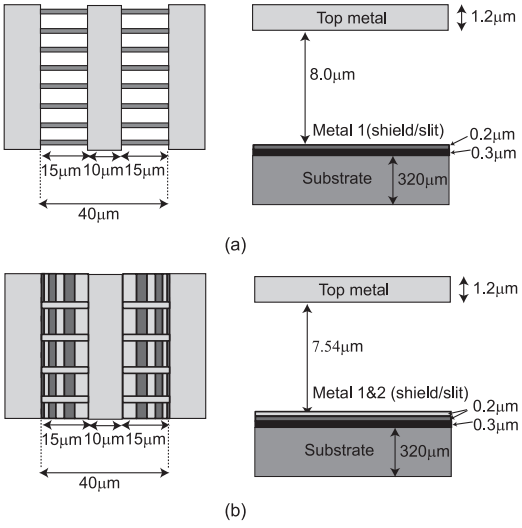


Fig. 5 Cross section of the transmission line. (a) Slow-wave coplanar waveguide (SWCPW). (b) CPW with two-metal ground.

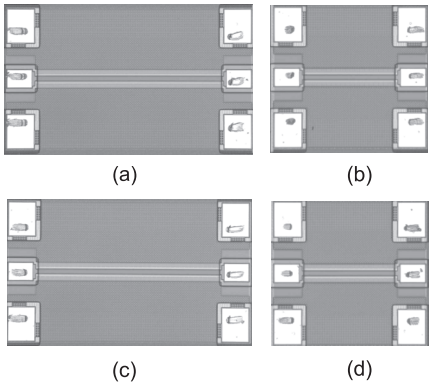


Fig. 6 Micrograph of the transmission lines. (a) 400-μm Slow-wave coplanar waveguide (SWCPW). (b) 200-μm SWCPW. (c) 400-μm CPW with two-metal ground. (d) 200-μm CPW with two-metal ground.

3.2 Transistor De-Embedding

Transistors have also been implemented in CMOS 65 nm process. T-Lines are employed for the access lines of the transistors which can be de-embedded after modeling the T-lines. The micrograph are shown in Fig. 10. The Y-matrix and Z-matrix of the pad are subtracted from the measured matrix of the transistors. The access T-lines are also de-embedded. The maximum stable gain (MSG) and maximum available gain (MAG) of a transistor after de-embedding is given in Fig. 11. The finger width of the transistor is 2 μm and the total width 40 μm.

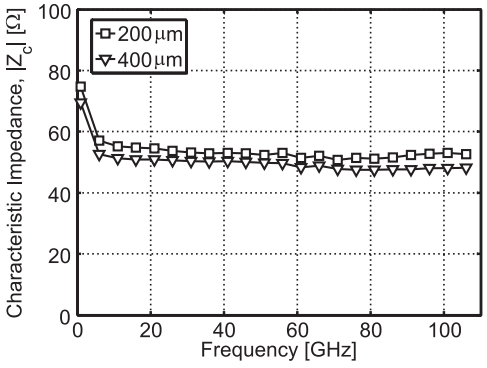


Fig. 7 Open-short de-embedding method for the characteristic impedance of 200-μm and 400-μm CPWs with two-metal ground.

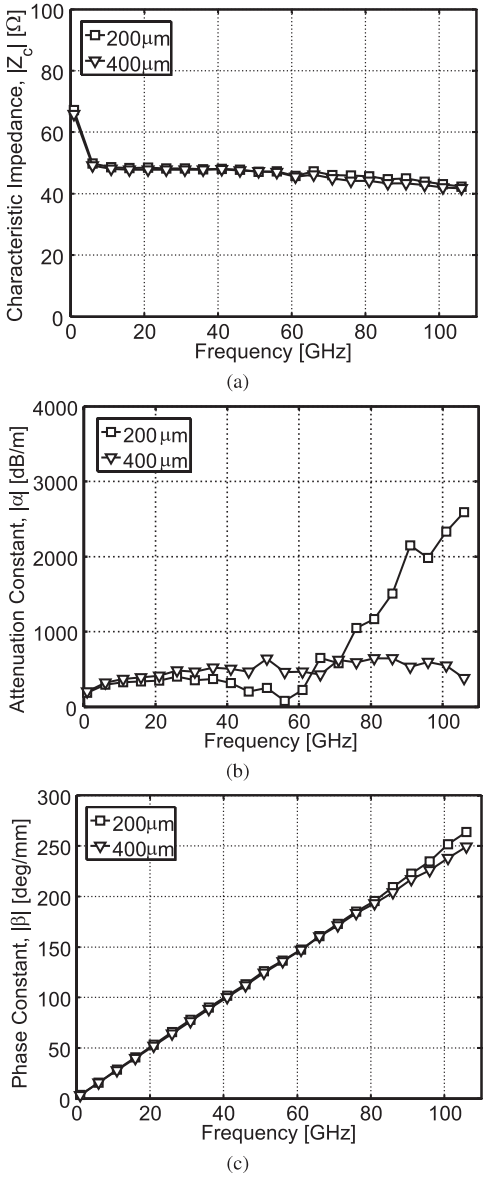


Fig. 8 Through-only de-embedding method for 200-μm and 400-μm CPWs with two-metal ground. (a) Characteristic impedance. (b) Attenuation constant. (c) Phase constant.

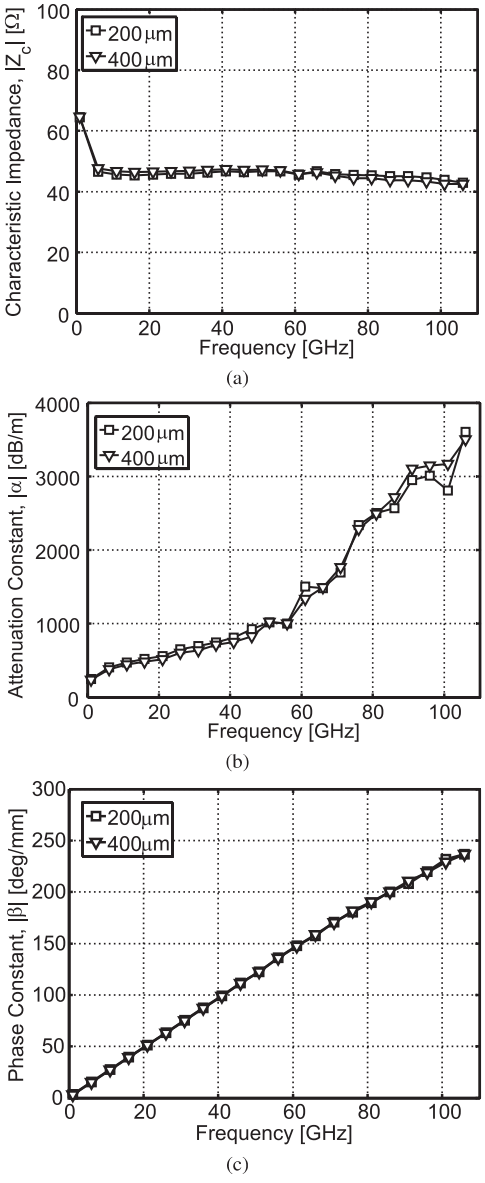


Fig. 9 L-2L through-line de-embedding method for 200-μm and 400-μm CPWs with two-metal ground. (a) Characteristic impedance. (b) Attenuation constant. (c) Phase constant.

3.3 One-stage Amplifier

To verify the precision of the de-embedding method and the model of the T-line, a one-stage amplifier has been fabricated in CMOS 65 nm process. The schematic and micrograph are shown in Fig. 12. A 5.4 dB power gain at 67 GHz has been realized at a V_{gs} of 0.8 V and a V_{ds} of 1.2 V. The measured MSG of the transistor is about 9.4 dB as shown in Fig. 11. Therefore the loss of the matching network is about 4 dB. The measured and simulated results including pads are compared in Fig. 13. As can be seen that the simulation results before de-embedding does not match with the measurement results. However, the simulation results after de-embedding match with the measurement results very well

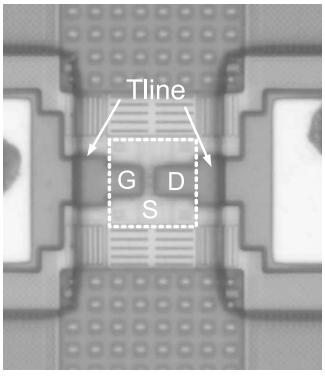


Fig. 10 Micrograph of the transistor.

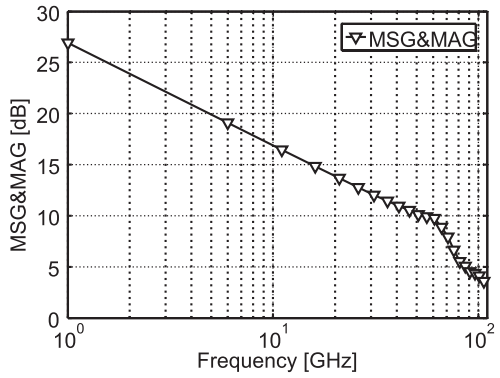
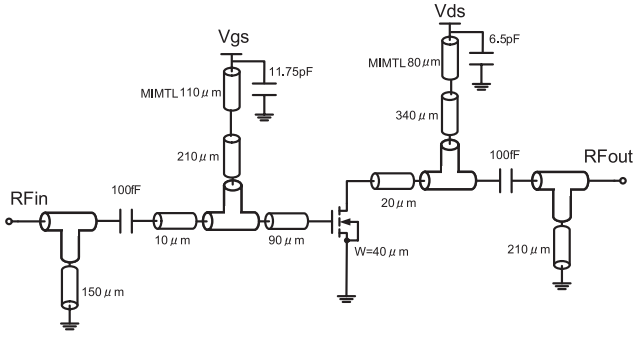
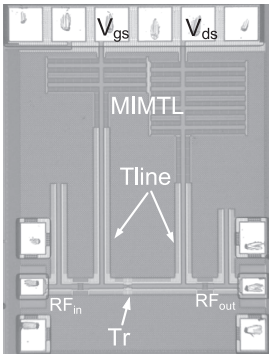


Fig. 11 Measured maximum stable gain or maximum available gain of a transistor at a V_{gs} of 0.8 V and a V_{ds} 1.2 V.



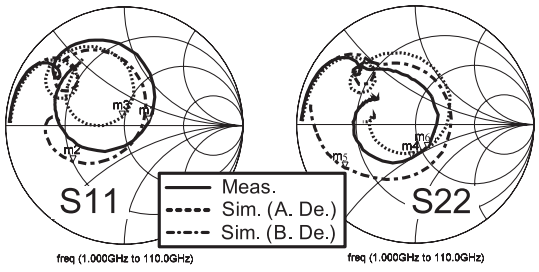
(a)



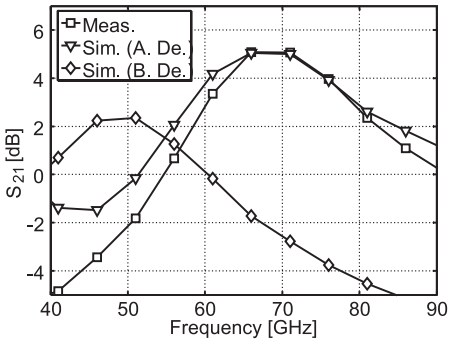
(b)

Fig. 12 Schematic and micrograph of the one-stage amplifier.

even though the peak of S_{11} and S_{22} shifts about 2~3 GHz. There are several reasons which are considered responsible for that: (1) Inaccuracy of the DC supply impedance; (2) Modeling error related to the Tee junction and the de-coupling MIM model; (3) Variation of the DC-cut capacitance. Because to model the Tee-junction accurately, a three-port test element is needed. However, due to the lack of measurement instruments, we can not measured it up to 110 GHz. Therefore, a two-port test element is utilized. As to the de-coupling MIM model, because the characteristic impedance are very low, it is very sensitive to the measurement.



(a)



(b)

Fig. 13 Comparison between the measured and simulated results of the one-stage amplifier at a V_{gs} of 0.8 V and a V_{ds} of 1.2 V. (a) S_{11} and S_{22} with markers at 67 GHz. (b) S_{21}.

4. Design and Measurement Results of 4-Stage CMOS PA

By using the built models in Sect. 3 a four-stage amplifier has been designed and fabricated in CMOS 65 nm process. The measured T-lines are employed for the matching blocks. The first three stages are designed to realize a better gain matching, whereas the final output stage is optimized for a power matching. The load impedance is obtained from a load-pull analysis.

The circuit schematic of the 4-stage CMOS power amplifier is given in Fig. 14 and Fig. 15 shows the micrograph. The chip size is 1.5 mm × 0.85 mm. Figures 16 shows the measured and simulated S-parameters. A measured small signal power gain of 16.4 dB is obtained which is about 1.1 dB smaller than the simulated one. The reason is considered as that the non-ideal ground degenerates the source of the transistors and therefore decreases the power gain. The large signal measurement results are shown in Fig. 17. The simulation results are about 0.6 dB larger than the measurement ones. The difference can be generated from the large signal (DC) model of the transistor. And the 1 dB output compression point of 4.6 dBm at 61.5 GHz with a DC current consumption of 128 mA at a VDD of 1.2 V.

Table 1 shows the summary of the presented and conventional 60 GHz CMOS power amplifiers. The MMW CMOS power amplifier reported in this paper achieves state-of-the-art performance.

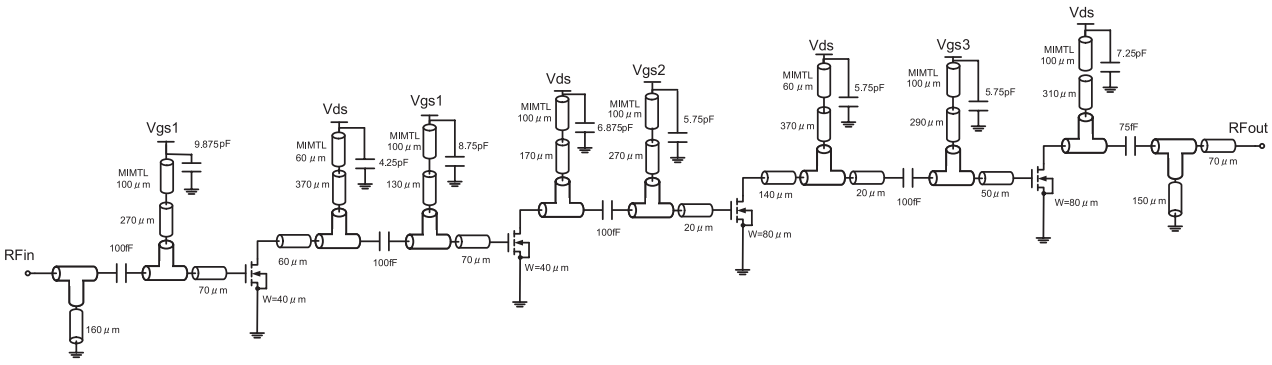


Fig. 14 Circuit schematic of the four-stage power amplifier.

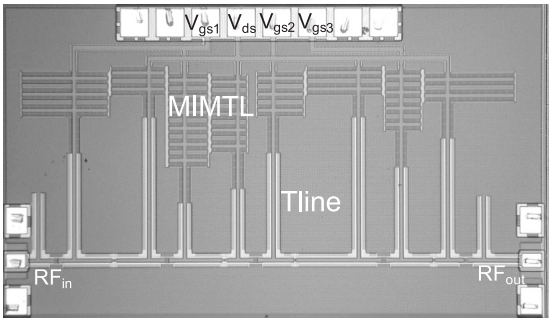
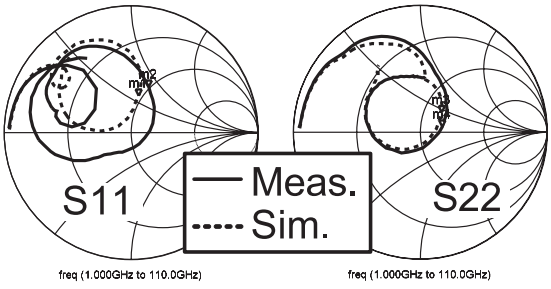
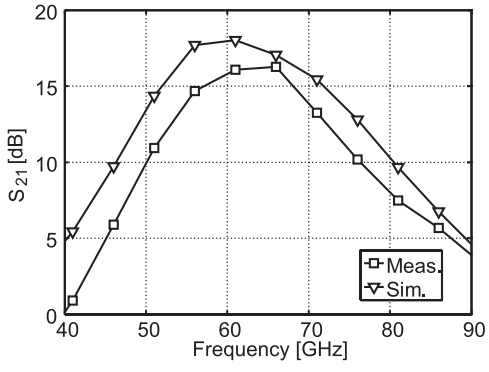


Fig. 15 Micrograph of the four-stage PA.

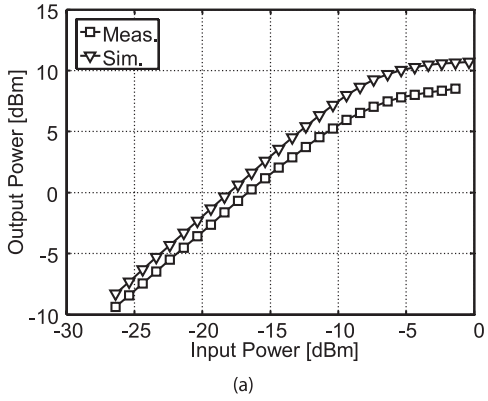


(a)

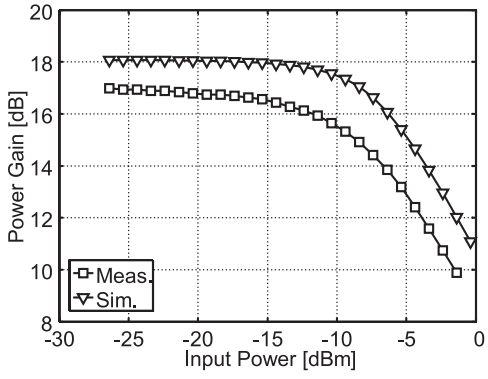


(b)

Fig. 16 Measured and simulated S-parameters results of the four-stage amplifier. (a) S_{11} and S_{22} with markers at 61 GHz. (b) S_{21}.



(a)



(b)

Fig. 17 Large signal characteristics of the four-stage PA. (a) Output power versus input power. (b) Large signal power gain versus input power.

5. Conclusion

An L-2L through-line de-embedding method has been verified up to millimeter wave frequency. The parasitics of the pad can be modeled from the L-2L through-line. Measurement results of the transmission lines and transistors can be de-embedded by subtracting the parasitic matrix of the pad. Therefore, the de-embedding patterns decrease greatly and the chip area also decreases which is used for modeling active and passive devices. A one-stage amplifier is firstly implemented for helping verifying the de-embedding results.

Table 1 Performance summary.

Reference	Technology	Freq. [GHz]	Gain [dB]	P_{1dB} [dBm]	PAE@P_{1dB} [%]	P_{DC} [mW]	V_{DD} [V]
[2] JSSCC 2007	90 nm CMOS	61	5.2	6.4	7.4	21	1.5
[3] ISSCC 2008	90 nm CMOS	60	8.2	8.2	2.4	229	1.2
[4] RFIC 2008	90 nm CMOS	63	14	11	15	81	1.2
[5] ISSCC 2008	90 nm CMOS	60	5.5	9	6	80	1
[6] ISSCC 2008	90 nm CMOS	60	13.3	10.5	8	150	1
[7] ISSCC 2009	65 nm CMOS	60	15.8	2.5	3.95	43.5	1
[8] ISSCC 2009	45 nm CMOS	60	13.8	11	–	–	1.1
[9] MWCL 2009	90 nm CMOS	60	30	10.3	6	178	1.8
This work	65 nm CMOS	61.5	16.4	4.6	2.3	128	1.2

After that a four-stage 60 GHz amplifier has been fabricated in CMOS 65 nm process. Experimental results show that the four-stage amplifier realizes an input matching better than −10.5 dB and an output matching better than −13 dB at 61 GHz. A small signal power gain of 16.4 dB and a 1 dB output compression point of 4.6 dBm are obtained with a DC current consumption of 128 mA from a 1.2 V power supply. The chip size is 1.5 mm × 0.85 mm.

Acknowledgments

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Appendix

As shown in Fig. A· 1, the ABCD matrix of the through-only pattern can be expressed by

$$\mathbf{T}_{\text{thru}}^{\mathbf{TO}} = T_{\text{lpad}} T_{\text{line}} T_{\text{line}} T_{\text{rpad}} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \quad \text{(A·1)}$$

where T_{thru}^{TO} is the measured through-only pattern ABCD matrix and l is the half length of the through-line.

$$\mathbf{T}_{\text{lpad}} = T_{\text{p}} T_{\text{s}} = \begin{pmatrix} 1 & Z_{\text{series}} \\ Y_{\text{shunt}} & Y_{\text{shunt}} Z_{\text{series}} + 1 \end{pmatrix} \quad \text{(A·2)}$$

$$\mathbf{T}_{\text{rpad}} = T_{\text{s}} T_{\text{p}} = \begin{pmatrix} Y_{\text{shunt}} Z_{\text{series}} + 1 & Z_{\text{series}} \\ Y_{\text{shunt}} & 1 \end{pmatrix} \quad \text{(A·3)}$$

$$\mathbf{T}_{\text{line}} = \begin{pmatrix} \cosh(\gamma l) & Z_{\text{c}} \sinh(\gamma l) \\ \frac{\sinh(\gamma l)}{Z_{\text{c}}} & \cosh(\gamma l) \end{pmatrix} \quad \text{(A·4)}$$

$$\begin{aligned} A = {} & (2Y_{\text{shunt}} Z_{\text{series}} + 1)(\cosh^2(\gamma l) + \sinh^2(\gamma l))^2 \\ & + 2Y_{\text{shunt}} Z_{\text{series}} \sinh(\gamma l) \cosh(\gamma l) \\ & + \frac{2Z_{\text{series}}(Y_{\text{shunt}} Z_{\text{series}} + 1)}{Z_{\text{c}}} \sinh(\gamma l) \cosh(\gamma l) \end{aligned} \quad \text{(A·5)}$$

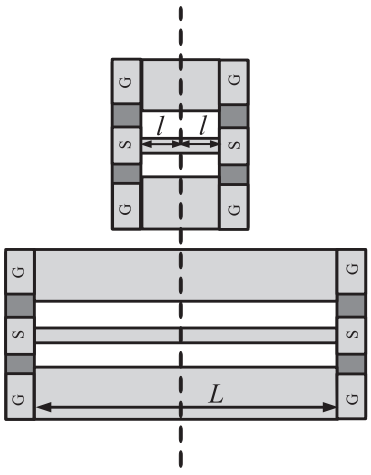


Fig. A· 1 Through-only de-embedding.

$$B = 2Z_{\text{series}}(\cosh^2(\gamma l) + \sinh^2(\gamma l))^2 + 2\left(Z_c + \frac{Z_{\text{series}}^2}{Z_c}\right)\sinh(\gamma l)\cosh(\gamma l) \quad (A\cdot 6)$$

$$C = 2Y_{\text{shunt}}(Y_{\text{shunt}}Z_{\text{series}} + 1)(\cosh^2(\gamma l) + \sinh^2(\gamma l))^2 + 2\frac{(Y_{\text{shunt}}Z_{\text{series}} + 1)^2}{Z_c}\sinh(\gamma l)\cosh(\gamma l) + 2Y_{\text{shunt}}^2 Z_c \sinh(\gamma l)\cosh(\gamma l) \quad (A\cdot 7)$$

$$D = A \quad (A\cdot 8)$$

Y_{shunt} is the shunt admittance of the pad and Z_{series} the series impedance. Z_c is the characteristic impedance of the through-line and γ the propagation constant. When $l = 0$,

$$A = D = 2Y_{\text{shunt}}Z_{\text{series}} + 1 \quad (A\cdot 9)$$

$$B = 2Z_{\text{series}} \quad (A\cdot 10)$$

$$C = 2Y_{\text{shunt}}Y_{\text{shunt}}Z_{\text{series}} + 1 \quad (A\cdot 11)$$

and

$$\mathbf{T}_{\text{thru}}^{\mathbf{TO}} = \begin{pmatrix} 2Y_{\text{shunt}}Z_{\text{series}}+1 & 2Z_{\text{series}} \\ 2Y_{\text{shunt}}(Y_{\text{shunt}}Z_{\text{series}}+1) & 2Y_{\text{shunt}}Z_{\text{series}}+1 \end{pmatrix} \quad (A\cdot 12)$$

which is the same as T_{thru} in the L-2L de-embedding method.

By using the following functions,

$$Y_{11} = \frac{D}{B} \quad (A\cdot 13)$$

$$Y_{12} = \frac{BC - AD}{B} \quad (A\cdot 14)$$

$$Y_{21} = \frac{-1}{B} \quad (A\cdot 15)$$

$$Y_{22} = \frac{A}{B} \quad (A\cdot 16)$$

The Y matrix of the through-only pattern can be obtained from the ABCD matrix

$$\mathbf{Y}_{\text{thru}}^{\mathbf{TO}} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \quad (A\cdot 17)$$

So the shunt admittance and series impedance calculated by using the through-only method is expressed as

$$Y'_{\text{shunt}} = Y_{11} + Y_{12}, \quad (A\cdot 18)$$

$$Z'_{\text{series}} = \frac{-1}{Y_{12}}. \quad (A\cdot 19)$$

Therefore the ABCD matrix of the pad calculated by using the through-only method is given by

$$\mathbf{T}'_{\text{lpad}} = \begin{pmatrix} 1 & Z'_{\text{series}} \\ Y'_{\text{shunt}} & Y'_{\text{shunt}}Z'_{\text{series}} + 1 \end{pmatrix}, \quad (A\cdot 20)$$

$$\mathbf{T}'_{\text{rpad}} = \begin{pmatrix} Y'_{\text{shunt}}Z'_{\text{series}} + 1 & Z'_{\text{series}} \\ Y'_{\text{shunt}} & 1 \end{pmatrix}. \quad (A\cdot 21)$$

The DUT can be de-embedded by using the following expression.

$$T_{\text{dut}} = T'^{(-1)}_{\text{lpad}} T_{\text{meas}} T'^{(-1)}_{\text{rpad}} \quad (A\cdot 22)$$

Transferring the ABCD matrix to S matrix and using the method specified in [16] the characteristics of the T-line can be calculated from the S-parameters.

$$\gamma = \alpha + j\beta \quad (A\cdot 23)$$

$$e^{-\gamma(L-2l)} = \left\{\frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K\right\}^{-1} \quad (A\cdot 24)$$

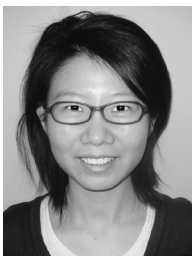
where L is the length of the T-line,

$$K = \left\{\frac{(S_{11}^2 - S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2}\right\}^{\frac{1}{2}} \quad (A\cdot 25)$$

$$Z = Z_0\left\{\frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}\right\}^{\frac{1}{2}} \quad (A\cdot 26)$$

where Z_0 is 50 Ω.

Changing the length of the through-only pattern, the characteristic impedance, attenuation constant and phase constant have been calculated. The calculated results is shown in Fig. 4 in Sect. 2.



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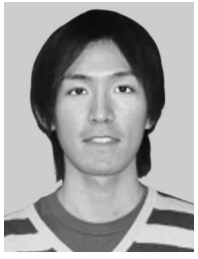

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