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PAPER Special Section on Analog Circuit Techniques and Related Topics

The Optimum Design Methodology of Low-Phase-Noise LC-VCO Using Multiple-Divide Technique

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SUMMARY The multiple-divide technique, using the multi-ratio frequency divider, has a possibility to improve FoM of VCO. This paper proposes a design optimization of LC-VCO using the multiple-divide technique. In the simulated results using 90-nm CMOS model parameters, the optimum frequency range, achieving better than −187.0 dBc/Hz of FoM, can be extended from 6.5–12.5 GHz to 1.5–12.5 GHz. The proposed multiple-divide technique can provide a lower phase-noise, lower power consumption, smaller layout area of LC-VCO.

key words: *CMOS, VCO, divider, inductor*

1. Introduction

Due to the miniaturization, Si CMOS technology has obtained higher f_T and f_{max}. Many kinds of RF applications have been realized by CMOS technology because of high-density integration, mixed-signal implementation, and lower fabrication cost. On the other hand, one of the biggest problems is that on-chip inductors have only 15 of quality factor at most because of thin metal thickness and Si substrate loss, which limits performances of CMOS RF circuits. Especially, LC-VCO (Voltage-Controlled Oscillator) has a poor performance due to the low-Q on-chip inductor even if it is one of the most important key components of wireless communication circuits.

There are several circuit techniques to improve phase noise of VCOs, e.g., applying a filtering technique to NMOS and PMOS tail node [1], [2], the class-C CMOS VCO [3], [4], the amplitude-redistribution technique [5].

Recentry, the optimization technique of low phase noise LC-VCO has been reported [6], which optimizes the inductor geometry and VCO parameter at the desired frequency.

However, the phase noise is basically limited by quality factor of inductors. The quality factor of on-chip inductor depends on spiral topology, metal resistivity, substrate conductivity, dielectric characteristics of interlayer dielectrics (ILDs), and the optimum structure is unique in each frequency and each process [7]. It is experimentally known that higher-Q inductors can be realized at higher frequencies. For example, it is a common technique to use a doubled-frequency VCO with a divide-by-2 frequency divider to avoid the local leakage. In some cases, better phase-noise characteristics can be obtained by such the dividing architecture at the cost of larger power consumption. However, the effect of the improvement has still not been unclear, and there is a trade-off in phase noise and power consumption.

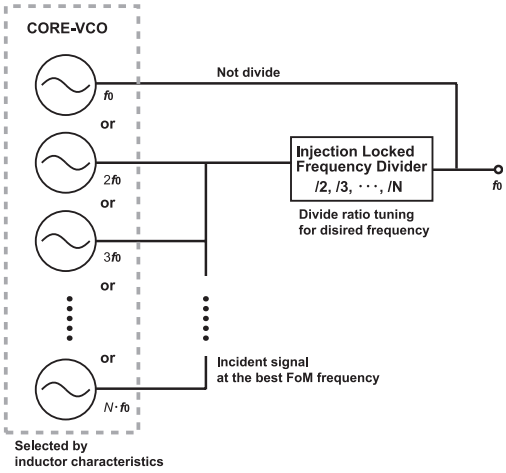

Fig. 1 The proposed system diagram.

In this paper, we propose a multiple-divide technique using a divide-by-N frequency divider, which expands design space of low-phase noise VCO. In the proposed method, oscillation frequency of incident VCO is chosen according to characteristics of on-chip inductors, which is N-times higher than the required frequency as shown in Fig. 1. The higher-frequency oscillation provides a possibility to improve the phase-noise performance considering power consumption. Moreover, VCO and frequency divider can, fortunately, operate at higher frequency with reasonable power consumption due to the recent miniaturization of CMOS process, which also expands the design space of the proposed method.

This paper presents a design optimization methodology to optimize the phase-noise performance by using the proposed multiple-divide technique. In this paper, simulated results using 90-nm CMOS model parameters are presented, and it is also shown that the optimum frequency range achieving better phase noise can be expanded by the proposed multiple-divide technique.

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2. Design of VCO Using Frequency Divider

This section explains design consideration of LC-VCO using a multiple-divide frequency divider to achieve lower phase-noise and smaller power dissipation.

Phase noise is deeply linked to power consumption of VCO, and the total power consumption of the proposed circuit is increased by higher oscillation frequency and additional power dissipation of frequency divider while lower phase-noise might be obtained.

There are several trade-offs to choose a circuit topology according to the required frequency. Therefore, in this section, power consumption and phase noise are theoretically discussed independently of the circuit topology, and it is shown that the design space of LC-VCO can be expanded by using the multiple-divide technique.

2.1 Trade-Offs in On-Chip Spiral Inductors

In this section, it is analytically shown that quality factor of on-chip spiral inductors becomes higher at higher frequency.

In general, it is quite difficult to realize high-Q, e.g., more than 50, inductors at the present CMOS processes, because there are several trade-offs in designing on-chip spiral inductors. Quality factor of spiral inductors on Si substrate is limited by metal resistivity and substrate loss. Basically, to obtain the highest quality factor, the optimal structure is unique for each frequency due to limited design parameters in CMOS processes. On the other hand, at higher frequencies, higher-Q inductors can be obtained.

From the aspect of layout design, diameter, line width, line space and a number of turns are the most common design parameters of on-chip spiral inductors. In addition, there are several options, e.g., symmetrical/asymmetrical, patterned ground shield, multi-layer, etc. From the aspect of fabrication process, the following conditions have influence on inductor characteristics; metal thickness, metal resistivity, dielectric thickness, dielectric permittivity/loss, substrate structure, substrate conductivity/permittivity, permeability of each material, etc.

The number of turns of spiral inductor has a trade-off between layout area and mutual inductances of segments. In CMOS chips, huge layout of spiral inductors, e.g., 500 μm $\times$ 500 μm is not preferable from the viewpoint of fabrication cost. On the other hands, inner spiral trace degrades average inductance per line length because magnetic flux penetrating the metal trace is counteracted by eddy current as known as Lenz's law. Thus, many numbers of turns are not preferable. In addition, the diameter also has a trade-off, and it is determined by the number of turns and required inductance.

The line space of spiral inductor should be minimized to reduce mutual inductances of segments. Line-to-line capacitance is usually small because of thin metal thickness. Wider metal can improve resistive loss of spiral metal while it has larger parasitic capacitance between metal and substrate. The parasitic capacitance lowers self-resonance frequency, which also degrades peak quality factor. The wider metal also causes degradation of average inductance per line length. Quality factor of peak frequency can be simply obtained by the following equation.

$$Q_{\text{peak}} = \frac{\omega_{\text{peak}} L(\omega_{\text{peak}})}{R} \tag{1}$$

Q_{peak} is the peak quality factor. ω_{peak} is the peak frequency where quality factor has the highest value. $L(\omega_{\text{peak}})$ is inductance at the peak frequency, and R is series resistance of inductor. When smaller inductance is used, the peak frequency ω_{peak} becomes higher, and the peak frequency ω_{peak} can be approximately calculated by the following equation.

$$\omega_{\text{peak}} = \frac{1}{\sqrt{3LC_L}} \tag{2}$$

where C_L is parasitic capacitance of inductor, and C_L is almost proportional to L because it is also proportional to line length ℓ. This relationship can be expressed by the following equations.

$$L = k_{\text{L}} \ell^{\alpha} \tag{3}$$

$$C_L = k_{\text{C}} \ell = k_{\text{C}} \left(\frac{L}{k_{\text{L}}} \right)^{\frac{1}{\alpha}} \tag{4}$$

$$R = k_{\text{R}} \ell = k_{\text{R}} \left(\frac{L}{k_{\text{L}}} \right)^{\frac{1}{\alpha}} \tag{5}$$

$$0 < \alpha < 3 \tag{6}$$

where k_L, k_C, and k_R are proportional constants of inductance, capacitance, and resistance per unit length, respectively. The following equation can be derived.

$$Q_{\text{peak}} = \frac{1}{R} \sqrt{\frac{L}{3C_L}} \tag{7}$$

$$= k_{\text{R}}^{-1} (3k_{\text{C}})^{-\frac{1}{2}} k_{\text{L}}^{\frac{3}{2\alpha}} L^{\frac{\alpha-3}{2\alpha}} \tag{8}$$

At higher frequency, smaller inductance is utilized, and line length ℓ of inductor becomes shorter. Therefore, quality factor can be improved at higher frequency according to Eq. (8), which is also explained by the following equation.

$$Q_{\text{peak}} = {k_R}^{-1} (3k_{\text{C}})^{\frac{1-\alpha}{1+\alpha}} k_{\text{L}}^{\frac{2}{1+\alpha}} \omega_{\text{peak}}^{\frac{3-\alpha}{1+\alpha}} \tag{9}$$

k_L depends on the layout structure. At higher frequencies, k_L can be improved due to less numbers of turns, and k_R is increased at higher frequency because of the skin effect [8], [9]. Therefore, there is an optimum frequency range to obtain higher-Q inductors, which is quantitatively presented in Sect. 3.1.

2.2 VCO Analysis with Frequency Divider

In this section, VCO performances, i.e., phase noise, power consumption, etc, are discussed in consideration of a frequency divider. Phase noise at output of a divide-by-2 frequency divider is 6 dBc/Hz better than that of VCO. In general, divide-by-N dividers can improve phase noise by

$20\log N$ [dBc/Hz], because the frequency divider narrows side-lobe of phase noise as carrier frequency becomes small.

On the other hand, phase noise depends on oscillating frequency, oscillation amplitude, and quality factor of LC tank. Phase noise $\mathcal{L}$ can be estimated by the following model [10].

$$\mathcal{L}(f_{\text{offset}}) = 10\log\left[\frac{2\text{k}T}{P_{\text{sig}}}\left(\frac{f_0}{2Q_L f_{\text{offset}}}\right)^2\right] \tag{10}$$

where k is Boltzmann's constant and T is temperature, P_{sig} is the average power dissipated in the resistive part of the tank, f_0 is the oscillation frequency, and f_{offset} is the offset frequency. Q_L is quality factor of inductor, which is almost equal to the effective quality factor of LC-tank. Q_L and P_{sig} are calculated as follows.

$$Q_L = \frac{R_{\text{p}}}{\omega L}\frac{\omega L}{R} \tag{11}$$

$$P_{\text{sig}} = I_{\text{bias}}^2 R_{\text{p}} = I_{\text{bias}}^2 Q_L \omega L \tag{12}$$

where L is inductance, R_{p} is parallel resistance of LC-tank, and I_{bias} is bias current. Therefore, the following equation can be derived.

$$\mathcal{L}(f_{\text{offset}}) = 10\log\left[\frac{\text{k}T f_0}{4\pi I_{\text{bias}}^2 {Q_L}^3 L f_{\text{offset}}^2}\right] \tag{13}$$

$$\mathcal{L}'(f_{\text{offset}}) = 10\log\left[\frac{\text{k}T f_0'}{4\pi I_{\text{bias}}'^2 {Q_L'}^3 L' f_{\text{offset}}'^2}\right] - 20\log N \tag{14}$$

where $\mathcal{L}'(f_{\text{offset}})$ is the phase noise of output of divide-by-N divider with the VCO oscillating at N-times higer frequency. According to Eq. (10), phase noise depends on oscillation frequency, offset frequency, and signal amplitude, so the following FoM (Figure of Merit) is employed to evaluate the total performance.

$$\text{FoM} = \mathcal{L}(f_{\text{offset}}) - 20\log\left(\frac{f_0}{f_{\text{offset}}}\right) + 10\log\left(\frac{P_{\text{total}}}{1\,\text{mW}}\right) \tag{15}$$

where P_{total} is the total power consumption considering both VCO and divider. FoM and FoM' can be derived as follows.

$$\text{FoM} = 10\log\left[\frac{\text{k}T f_0}{4\pi I_{\text{bias}}^2 {Q_L}^3 L f_{\text{offset}}^2}\right] - 20\log\left(\frac{f_0}{f_{\text{offset}}}\right) + 10\log\left(\frac{P_{\text{total}}}{1\,\text{mW}}\right) \tag{16}$$

$$\text{FoM}' = 10\log\left[\frac{\text{k}T f_0'}{4\pi I_{\text{bias}}'^2 {Q_L'}^3 L' f_{\text{offset}}'^2}\right] - 20\log N - 20\log\left(\frac{f_0'/N}{f_{\text{offset}}'}\right) + 10\log\left(\frac{P_{\text{total}}'}{1\,\text{mW}}\right) \tag{17}$$

where FoM is figure of merit of VCO without a divider, and FoM' is figure of merit of VCO using a divider. Therefore, the following relationship can be obtained.

$$f_0' = N f_0 \tag{18}$$

$$P_{\text{total}} = P_{\text{VCO}} \tag{19}$$

$$P_{\text{total}}' = P_{\text{VCO}}' + P_{\text{div}} \tag{20}$$

where P_{div} is the power consumption of frequency divider, P_{VCO} is the power consumption of VCO, and P_{VCO}' is the power consumption of VCO oscillating at N-times higher frequency. To obtain a better FoM circuit, the following condition has to be satisfied.

$$\text{FoM}' < \text{FoM} \tag{21}$$

$$\frac{P_{\text{total}}'}{N I_{\text{bias}}'^2 {Q_L'}^3 L'} < \frac{P_{\text{total}}}{I_{\text{bias}}^2 {Q_L}^3 L} \tag{22}$$

I_{bias}', Q_L' and L' are bias current, quality factor, and inductance of VCO using the multiple-divide technique. Equation (22) still has a design parameter I_{bias}, which can be determined by resonator's impedance. Here, it is supposed that there is an optimum signal amplitude to achieve better FoM because too large signal amplitude causes degradation of g_{m} and small signal amplitude causes worse power efficiency. Thus, bias current can be determined by the following equation with the optimum signal amplitude V_{sig}.

$$I_{\text{sig}} = \frac{2}{\pi} I_{\text{bias}} \tag{23}$$

$$V_{\text{sig}} = I_{\text{sig}} R_{\text{p}} = I_{\text{sig}}' R_{\text{p}}', \tag{24}$$

and

$$I_{\text{bias}} = \frac{\pi}{2}\frac{V_{\text{sig}}}{Q_L \omega L} \tag{25}$$

$$I_{\text{bias}}' = \frac{\pi}{2}\frac{V_{\text{sig}}}{Q_L' N \omega L'}. \tag{26}$$

where the optimum voltage amplitude V_{sig} depends on VCO topology and supply voltage, and it does not depend on bias current I_{bias}. Equation (23) can be derived by Fourier analysis of current waveform [3]. The transistors are in conduction for half of each oscillation period, and the tank current resembles a square wave with 50% duty cycle. I_{bias} and I_{sig} are related to spectra at DC and ω of frequency, respectively.

Finally, we can obtain the following condition from Eqs. (22) and (26).

$$\frac{P_{\text{VCO}}' + P_{\text{div}}}{P_{\text{VCO}}} < \frac{1}{N}\cdot\frac{Q_L'/L'}{Q_L/L} \tag{27}$$

Equation (27) provides a condition to obtain better FoM by using the multiple-divide technique. The right term is simply determined by inductance and quality factor of inductors, which means that circuit designers can choose inductor structure independent of VCO topology and parameters. The right term also expresses a margin for power consumption of frequency divider. The margin becomes larger at higher frequency because Q_L becomes larger and smaller L can be used. Basically, smaller L is preferable for the multiple-division VCO because larger P_{sig} can be obtained by the smaller L under the limitted voltage amplitude condition.

Here, the design procedure is summarized.

(1) Estimate phase noise and power consumption at required frequency.
(2) Estimate power consumption of frequency divider (P_{div}) at N-times higher frequency.
(3) Choose higher-Q inductors to achieve better FoM at N-times higher frequency. There are usually several choises of high-Q inductors. In such cases, smaller L can be employed for the larger power margin.
(4) Determine the optimum N according to Eq. (27).
(5) Design detailed circuits.

Smaller impedance causes larger power consumption, so L has to be determined in consideration of power consumption requirement.

3. Simulation Results

3.1 Optimization of Inductors

Figure 2(a) shows quality factors at various structural configurations, which are derived from a commercial PDK for a 90-nm CMOS process. Agilent ADS is utilized for harmonic-balance simulations to evaluate VCO performances. The result reveals the optimum structure for each frequency. Figure 2(b) shows inductance corresponding to each structure in Fig. 2(a). The configurations of spiral inductors are 9 or 15 μm line width and 50 or 80 μm inner diameter. The number of turns is varied according to the required inductance. As shown in Fig. 2(a), the maximum quality factor becomes higher at higher frequencies, and improvement of phase noise can be expected. Figure 2(c) shows the relationship between quality factor and inductance at the maximum Q frequency. To achieve better FoM, quality factor has to be increased, and inductance has to be decreased so that Q_{L}/L is maximized as explained in Eq. (27). Thus, there is a suitable inductance for each frequency.

3.2 Performance of Frequency Divider

This section explains phase noise and power consumption of the frequency divider. Figures 3 and 4 show a VCO and a frequency divider. In this work, a 3-stage ring-type injection-locked frequency divider (ILFD) is employed as shown in Fig. 4.

The ILFD can operate as a multiple frequency divider. Output frequency of the ILFD is locked by injected signal from the incident VCO, and the ILFD, oscillating at f_{div} of frequency, can be locked by $N \times f_{\mathrm{div}}$ of input frequency. Ring-type ILFDs have wider locking range, and the range can be tuned by bias current. The designed ILFD can operate from 1.5 GHz to 8 GHz, and locking sensitivity can be also tuned by bias current.

Figure 5 shows phase noise of the ILFD output. Phase noise of ring-type ILFD in free-run state is not desirable for wireless applications. However, the phase noise in the injection-locked state can be considerably improved, and it

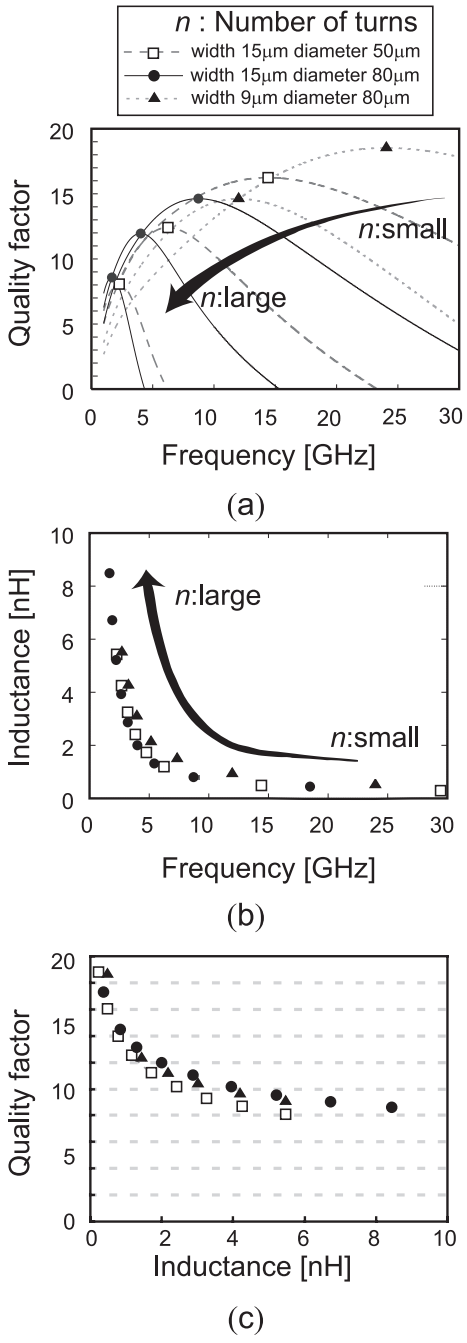

Fig. 2 (a) Quality factor. (b) Inductance corresponding to the structure in Fig. 2(a). (c) The relationship between quality factor and inductance.

is basically determined by the phase noise performance of the incident VCO. Phase noise of ILFD in divide-by-2 state can provide 6 dBc/Hz lower phase noise than that of the incident VCO. In general, a divide-by-N frequency divider can, theoretically, improve phase noise by 20log N [dBc/Hz], because the frequency divider narrows side-lobe of phase noise as carrier frequency becomes small.

Figure 6 shows the power consumption of the ILFD. The power consumption of the ILFD is determined by oscillation frequency of the frequency divider, and it does not

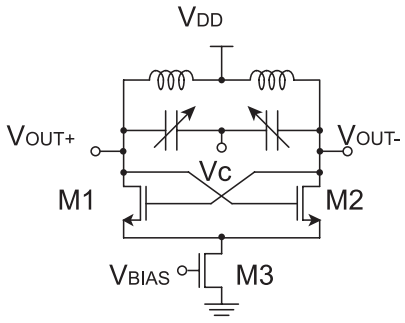

Fig. 3 VCO topology.

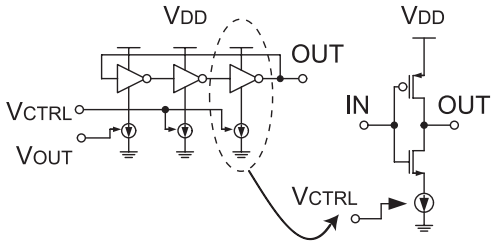

Fig. 4 3-stage injection-locked frequency divider.

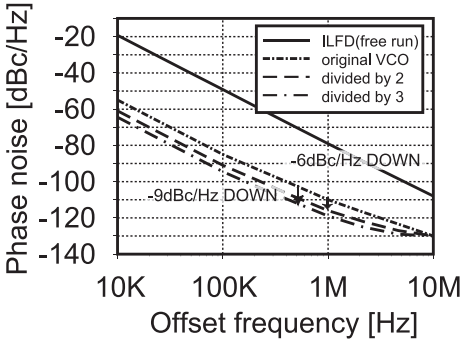

Fig. 5 ILFD phase noise.

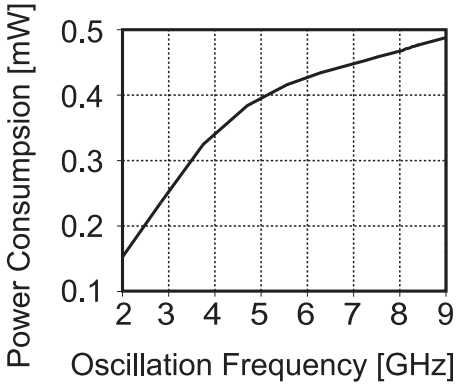

Fig. 6 ILFD power consumption.

depend on input frequency, so power consumption can be kept small as compared with VCO.

In this simulation, a differential-output ILFD is utilized to simplify the discussion. However, the proposed technique can easily be applied to a quadrature-output ILFD.

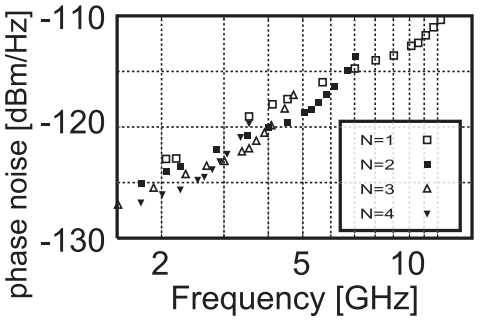

Fig. 7 Phase noise at 1-MHz offset.

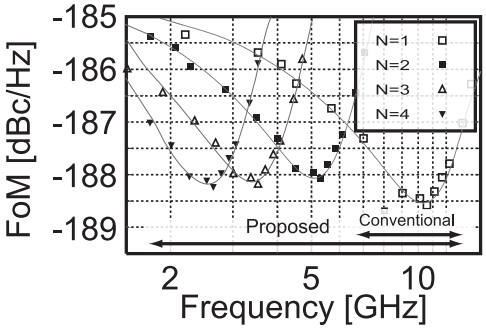

Fig. 8 Comparison of FoM.

3.3 VCO Optimization

Next, simulated VCO performances are explained. In this simulation, VCO consisting of NMOS cross-coupled pair and NMOS current source is utilized as shown in Fig. 3, because of requirement for less parasitic capacitance at higer frequency. NMOS transistors have high gain characteristic and decrease parasitic capacitance when the transistor size is dicided on required gain for oscilation.

Figures 7 and 8 show phase noise and FoM of VCOs using the multiple-divide frequency divider. In Fig. 7, oscillation frequency of VCO is N-times higher than divided frequency. VCO and divider are optimally designed for each frequency.

Figure 8 is a normalized result, which shows intrinsic performance as a synthesizer. There is the optimum frequency range, which achieves better phase noise characteristics. In Fig. 8, non-divided oscillation, $N = 1$, has the optimum frequency range of 6.5–12.5 GHz, achieving better than −187.0 dBc/Hz of FoM. The range can be expanded by the proposed multiple-divide technique, and it becomes 1.5–12.5 GHz as shown in Fig. 8.

Figure 9 shows a phase-noise comparison between the conventional non-divided oscillation at 3.5 GHz, divide-by-3 oscillation at 3.5 GHz, and base oscillation at 10.5 GHz. Theoretically, the base oscillation at 10.5 GHz has 9 dB higher phase noise than the divide-by-3 oscillation at 3.5 GHz. At lower offset frequencies, phase noise can be

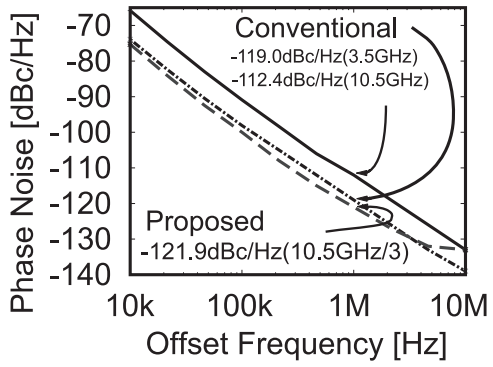

Fig. 9 Phase noise at 3.5 GHz frequency.

Table 1 Summary of design results.

divide-by-#	not-divided	2	3	4
oscillation frequency f_0 [GHz]	3.5	7	10.5	14
phase noise at f_0 [dBc/Hz]	−119.0	−114.7	−112.4	−107.6
phase noise at 3.5 GHz [dBc/Hz]	−119.0	−120.7	−121.9	−119.6
$20 \log N$ [dBc/Hz]	+0	+6.0	+9.5	+12.0
P_{VCO} [mW]	2.7	2.7	2.7	2.7
P_{divider} [mW]	–	0.26	0.26	0.26
FoM [dBc/Hz]	−185.7	−186.9	−188.2	−185.9

considerably improved as compared with the conventional approach. Table 1 shows the summary of simulated results at 3.5 GHz of output. Phase noises at 1-MHz offset are listed in Table 1. According to the result, divide-by-3 is the best choice to realize low-phase-noise VCO in this case.

4. Conclusions

This paper proposes the multiple-divide technique using the multiple frequency dividers to realize a lower phase-noise LC-VCO. The simulated results, using 90-nm CMOS model parameters, reveals the design space of multiple-divide VCOs. In the results, the optimum frequency range, achieving better than −187.0 dBc/Hz of FoM, can be extended from 6.5–12.5 GHz to 1.5–12.5 GHz. The proposed multiple-divide technique can provide a lower phase-noise, lower power consumption, smaller layout area LC-VCO.

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