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Analysis of Phase Noise Degradation Considering Switch Transistor Capacitances for CMOS Voltage Controlled Oscillators

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SUMMARY In this paper we present a study on the design optimization of voltage-controlled oscillators. The phase noise of LC-type oscillators is basically limited by the quality factor of inductors. It has been experimentally shown that higher-Q inductors can be achieved at higher frequencies while the oscillation frequency is limited by parasitic capacitances. In this paper, the minimum transistor size and the degradation of the quality factor caused by a switched-capacitor array are analytically estimated, and the maximum oscillation frequency of VCOs is also derived from an equivalent circuit by considering parasitic capacitances. According to the analytical evaluation, the phase noise of a VCO using a 65 nm CMOS is 2 dB better than that of a 180 nm CMOS.

key words: *CMOS, VCO, inductor, phase noise, quality factor, multiple divide, switched capacitor*

1. Introduction

Owing to miniaturization, Si CMOS technology has achieved higher value of f_T and f_{max}. Many types of RF applications have been realized by CMOS technology because of high-density integration, mixed-signal implementation, and the lower fabrication cost.

On the other hand, one of the main problems of CMOS technology is that on-chip inductors only have a quality factor of at most 15 because of the low metal thickness and the Si substrate loss, which limits the performance of CMOS RF circuits. In particular the LC voltage-controlled oscillator(LC-VCO) has poor performance due to the low-Q on-chip inductor even though it is one of the most important key components of wireless communication circuits.

There are several circuit techniques for improving the phase noise of VCOs, e.g., applying a filtering technique to the NMOS and PMOS tail nodes [1], [2], the class-C CMOS VCO [3], and the amplitude-redistribution technique [4]. However, the phase noise is basically limited by the quality factor of the inductors. The quality factor of an on-chip inductor depends on the spiral topology, metal resistivity, substrate conductivity, and the characteristics of the interlayer dielectric (ILD). Moreover, the optimum structure is unique for each frequency and each process. It has been experimentally shown that higher-Q inductors can be realized at higher frequencies [5]. Moreover, the quality factor of capacitors becomes nonnegligible higher frequencies such as above 5 GHz. The switched-capacitor array, in particular, becomes critical. However, this has not been discussed analyticall in detail.

In this paper, the effect of parasitic capacitances on oscillation frequency and phase noise will be evaluated analytically [6].

2. Design of VCO

In this section we explain the design considerations of an LC-VCO with parasitic capacitances to achieve lower phase noise and smaller power dissipation.

The phase noise is obtained by the following equation [7]:

$$\mathcal{L}(f_{\mathrm{offset}}) = 10\log\left[\frac{2\mathrm{k}T}{P_{\mathrm{sig}}}\left(\frac{f_0}{2Q_{\mathrm{tank}}f_{\mathrm{offset}}}\right)^2\right], \quad (1)$$

where k is Boltzmann's constant, T is the absolute temperature, P_{sig} is the output power, f_0 is the oscillation frequency, f_{offset} is the offset frequency, and Q_{tank} is the quality factor of the resonators. Equation (1) shows that the value of Q_{tank} is very important for determining the performance of VCOs. Figure 1 shows a standard VCO consisting of NMOS cross-coupled transistors. Q_{tank} is determined by the characteristic of the components in the VCOs, e.g., inductor, MIM capacitor, varactor, and transistor. In this section, it is explained how to derive the quality factor considering the parasitics as a function of frequency.

2.1 Trade-Offs in On-Chip Spiral Inductors

On-chip spiral inductors tend to have a higher quality factor at higher frequencies. On the other hand, the skin effect and eddy current degrade the quality factor at higher frequencies thus, there is an optimum frequency range. In this section, this is explained along analytical and experimental results.

In general, it is difficult to realize a high-Q, for example, more than 50, for on-chip inductors using the present CMOS processes, because there are several trade-offs in the design of on-chip spiral inductors. The quality factor of spiral inductors on a Si substrate is limited by the low metal resistivity and substrate loss. Basically, to obtain a higher quality factor, the optimal structure is unique for each frequency owing to the limited design parameters in CMOS

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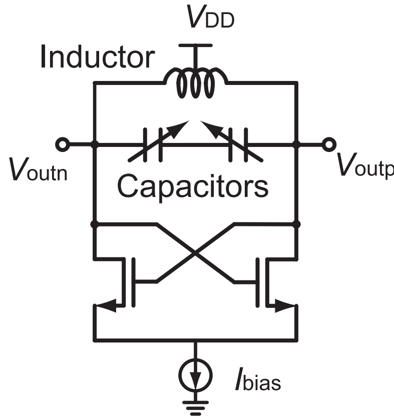


Fig. 1 Schematic of VCO circuit.

processes. On the other hand, at higher frequencies, higher-Q inductors can be obtained.

From the viewpoint of layout design, the diameter, linewidth, line space, and number of turns are the most common design parameters of on-chip spiral inductors. In addition, there are several options, e.g., symmetrical/asymmetrical, and use of a patterned ground shield or multilayer. From the viewpoint of the fabrication process, the following conditions affect the inductor characteristics; metal thickness, metal resistivity, dielectric thickness, dielectric permittivity/loss, substrate structure, substrate conductivity/permittivity, and the permeability of each material.

The number of turns of the spiral inductor has a trade-off relationship with the layout area and mutual inductance. In CMOS chips, a very large layout for the spiral inductors, e.g., $500\,\mu\text{m} \times 500\,\mu\text{m}$, is not preferable from the viewpoint of fabrication cost. On the other hand, an inner spiral trace degrades the average inductance per line length because magnetic flux penetrating the metal trace is counteracted by the eddy current, known as Lenz's law. Thus, a large number of turns is not preferable. In addition, the diameter also has a trade-off relationship with the number of turns and the required inductance.

The line space of a spiral inductor should be minimized to reduce mutual inductance. The line-to-line capacitance is usually small because of the low metal thickness. A wider metal layer can reduce the resistive loss of the spiral metal, although it results in a larger parasitic capacitance between the metal and the substrate. The parasitic capacitance reduces the self-resonance frequency, which also degrades the peak quality factor. A wider metal layers also causes the degradation of the mutual inductance per length.

On-chip inductor models can be simplified as shown in Fig. 2. The quality factor of an inductor is calculated by the following equation:

$$Q(\omega) = \frac{\text{Im(Z)}}{\text{Re(Z)}} = \frac{\omega L}{R}\left(1 - \frac{C_L R^2}{L} - \omega^2 L C_L\right), \quad (2)$$

where L is the series inductance, R is the series resistance, and C_L is the parasitic capacitance of the inductor. The quality factors of inductance Q_L and capacitance Q_C are simply

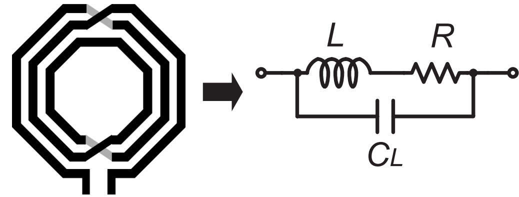


Fig. 2 Simplified model of on-chip inductor.

expressed by the following equations.

$$Q_L = \frac{\omega L}{R} \quad (3)$$

$$Q_C = \frac{1}{\omega C R} \quad (4)$$

In general, Q_L is about 10 and Q_C is about 100 for the Si CMOS process. Therefore, the following approximation can be derived.

$$1 - \frac{C_L R^2}{L} = 1 - \left(\frac{R}{\omega L}\right)(\omega C_L R) \simeq 1 \quad (5)$$

Using Eq. (5), Eq. (2) can be rewritten as

$$Q(\omega) \simeq \frac{\omega L}{R}\left(1 - \omega^2 L C_L\right) = \frac{\omega L(\omega)}{R}. \quad (6)$$

From Eq. (6), the peak quality factor can be easily obtained by the following equation.

$$Q_{\text{peak}} = \frac{\omega_{\text{peak}} L(\omega_{\text{peak}})}{R} \quad (7)$$

Q_{peak} is the peak quality factor. ω_{peak} is the peak frequency at which the quality factor has the highest value. $L(\omega_{\text{peak}})$ is the inductance at the peak frequency. When a smaller inductance is used, the peak frequency ω_{peak} becomes higher. When $\frac{dQ}{d\omega} = 0$, ω_{peak} is obtained as

$$\omega_{\text{peak}} = \sqrt{\frac{1 - \frac{C_L R^2}{L}}{3 L C_L}} \simeq \frac{1}{\sqrt{3 L C_L}}. \quad (8)$$

C_L is almost proportional to L because it is also proportional to the line length ℓ. This relationship can be expressed by the following equations [8].

$$L = k_{\text{L}} \ell^{\alpha} \quad (9)$$

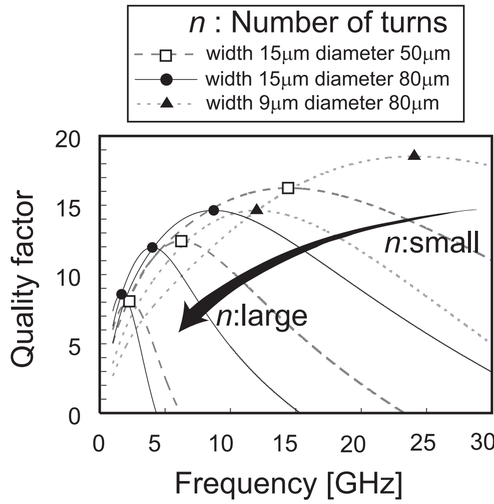
$$C_L = k_{\text{C}} \ell = k_{\text{C}} \left(\frac{L}{k_{\text{L}}}\right)^{\frac{1}{\alpha}} \quad (10)$$

$$R = k_{\text{R}} \ell = k_{\text{R}} \left(\frac{L}{k_{\text{L}}}\right)^{\frac{1}{\alpha}} \quad (11)$$

$$0 < \alpha < 3 \quad (12)$$

where k_L, k_C, and k_R are constants of proportionality for inductance, capacitance, and resistance per unit length, respectively. In this paper, the constant of proportionality α is assumed to be 1. The following equation can be derived.

$$Q_{\text{peak}} = \frac{2}{3R} \sqrt{\frac{L}{3 C_L}} \quad (13)$$



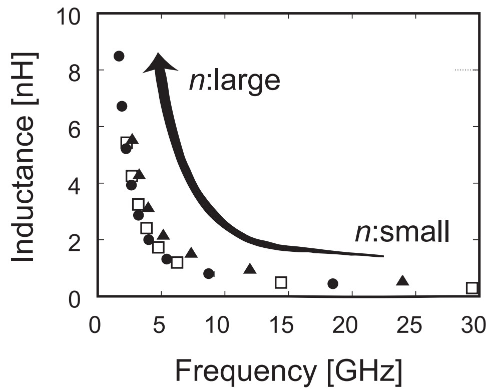


Fig. 3 (a) Quality factor. (b) Inductance corresponding to the structure in (a).

$$= \frac{2k_{\mathrm{L}}}{3k_{\mathrm{R}}L}\sqrt{\frac{k_{\mathrm{L}}}{3k_{\mathrm{C}}}} \tag{14}$$

At a higher frequency, a smaller inductance is utilized, and the line length ℓ of the inductor becomes shorter. Therefore, the quality factor can be improved at a higher frequency in accordance with Eq. (14), which is also indicated by the following equation.

$$Q_{\mathrm{peak}} = \frac{2k_L}{3k_R}\omega_{\mathrm{peak}} \tag{15}$$

Here k_L depends on the layout structure. At higher frequencies, k_L can be improved owing to the lower number of turns, and k_R is increased at a higher frequency because of the skin effect. Therefore, there is an optimum frequency range for obtaining higher-Q inductors.

Figure 3(a) shows the quality factors of various structural configurations, which are derived from a commercial PDK for a CMOS process. The figure reveals the optimum structure for each frequency. Figure 3(b) shows the inductance corresponding to each structure in Fig. 3(a). The spiral inductors have a 9 or 15 μm linewidth and a 50 or 80 μm inner diameter. The number of turns is varied according to the required inductance. As shown in Fig. 3(a), the maximum quality factor becomes higher at higher frequencies, and an improvement of phase noise can be expected.

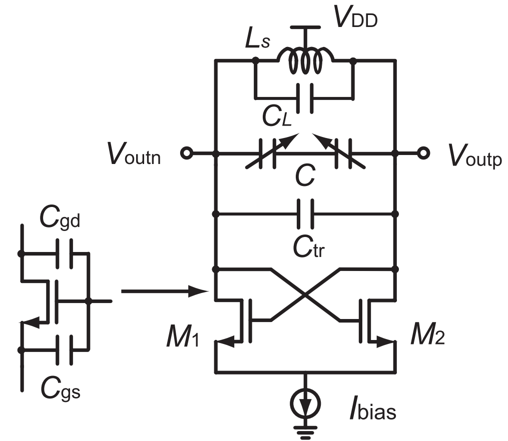


Fig. 4 Equivalent circuit of VCO in consideration of parasitic capacitances.

2.2 Parasitic Capacitances in Cross-Coupled Transistors

In this section we explain the effect of parasitic capacitance in cross-coupled transistors.

As previously noted, an inductor with a higher Q can be obtained at higher frequencies. The performance of VCOs, e.g., phase noise and power consumption, is expected to be better at a higher oscillation frequency than at a lower oscillation frequency [5]. The oscillation frequency depends on the inductance and capacitance in the resonator. However, parasitic capacitances exist at each node, e.g., gate capacitance, substrate junction capacitance, fringing capacitance, line-to-line capacitance in the inductor, and substrate capacitance with the inductor trace. The maximum oscillation frequency of VCOs is affected by these parasitic capacitances. In this section, the maximum oscillation frequency will be expressed by a formula.

Figure 4 shows an equivalent circuit of a VCO with NMOS cross-coupled transistors considering parasitic capacitances. In this case, the oscillation frequency ω is expressed by the following equation.

$$\omega = \frac{1}{\sqrt{L_{\mathrm{s}}(C + C_{\mathrm{L}} + C_{\mathrm{tr}})}} \tag{16}$$

Here L_s and C_L are the inductance and capacitance of the inductor, respectively, and C is the capacitance of the varactor. The effective capacitance of the cross-coupled transistor is

$$C_{\mathrm{tr}} = \frac{1}{2}C_{\mathrm{gs}} + 2C_{\mathrm{gd}}, \tag{17}$$

where

$$C_{\mathrm{gs}} = \frac{2}{3}LC_{\mathrm{ox}}W, \tag{18}$$

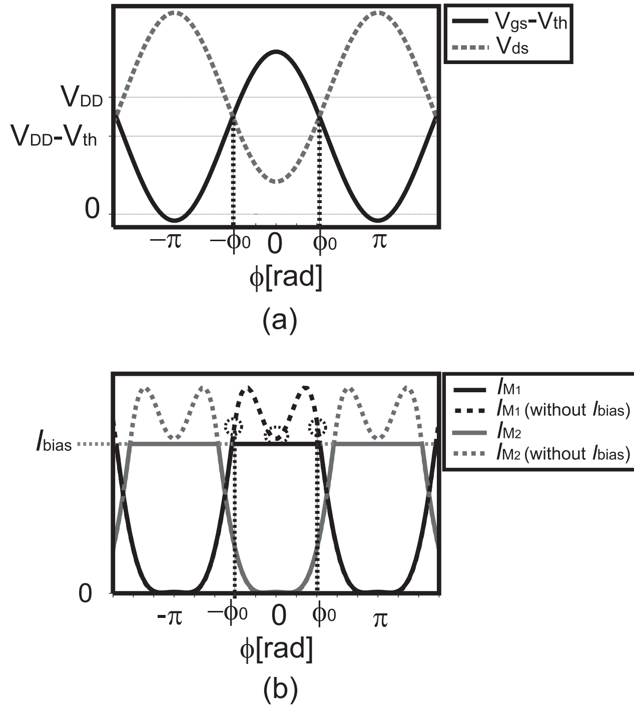


Fig. 5 (a) Vgs-Vds at M_1. (b) Waveform of current at M_1 and M_2.

$$C_{\mathrm{gd}} = 2C_{\mathrm{SW}}W, \tag{19}$$

where C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, C_{ox} is the unit gate capacitance, C_{SW} is the overlap capacitance, and W and L are the width and length of NMOS transistors, respectively. Using Eq. (17) to Eq. (19), C_{tr} can be expressed by the following equation:

$$C_{\mathrm{tr}} = C_{\mathrm{ox}}W\left(\frac{1}{3}L + 2k_{\mathrm{tr}}\right), \tag{20}$$

where

$$k_{tr} = C_{\mathrm{SW}}/C_{\mathrm{ox}}. \tag{21}$$

Here, the voltage waveform is assumed to be sinusoidal. V_{outp} and V_{outn} are expressed as

$$V_{\mathrm{outp}} = V_{\mathrm{DD}} - A\cos(\phi) \tag{22}$$

$$V_{\mathrm{outn}} = V_{\mathrm{DD}} + A\cos(\phi), \tag{23}$$

where $\phi = \omega t$ and the amplitude A is given by

$$A = \frac{2}{\pi}R_{\mathrm{p}}I_{\mathrm{bias}}, \tag{24}$$

where R_{p} is the parallel resistance of the resonator and is expressed by the following equation.

$$R_p = \omega L_s Q_L \tag{25}$$

Figure 5(a) shows the voltage waveforms of V_{ds} and $V_{\mathrm{gs}} - V_{\mathrm{th}}$ at M_1. The intersection indicated by ϕ_0 represents the boundary between the saturation region and the linear region. ϕ_0 is derived by the following equations.

$$\left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)\Big|_{\phi=\phi_0} = V_{\mathrm{ds}}|_{\phi=\phi_0} \tag{26}$$

$$V_{\mathrm{DD}} - A\cos(\phi_0) - V_{\mathrm{th}} = V_{\mathrm{DD}} + A\cos(\phi_0) \tag{27}$$

$$\cos(\phi_0) = \frac{V_{\mathrm{th}}}{2A} \tag{28}$$

Figure 5(b) shows the waveform of the current at M_1 and M_2. If a VCO does not have a tail current source, then it has a large signal amplitude and the cross-coupled transistors enter the linear region. In this case, the current at ϕ=0 is decreased as shown in Fig. 5(b), and the impulse sensitivity function (ISF) deteriorate [7]. To avoid the linear region, the current should be limited by a current source I_{bias}. The current waveform at the cross-coupled transistors has a shape similar to that of a square wave with the current source I_{bias}, and I_{M_1} must satisfy the following condition.

$$I_{\mathrm{bias}} < I_{\mathrm{M_1}}(0), I_{\mathrm{M_1}}(\phi_0) \tag{29}$$

The transistor is in the saturation region when $\phi = \phi_0$, so $I_{tr}(\phi_0)$ is calculated as follows:

$$I_{\mathrm{M_1}}(\phi_0) = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W}{L}\left(V_{\mathrm{DD}} - \frac{V_{\mathrm{th}}}{2}\right)^2, \tag{30}$$

where μ is the electron mobility. When $\phi = 0$, M_2 is in the linear region. $I_{tr}(0)$ is expressed by the following equation.

$$I_{\mathrm{M_1}}(0) = \mu C_{\mathrm{ox}}\frac{W}{L}\left((V_{\mathrm{DD}}+A-V_{\mathrm{th}})(V_{\mathrm{DD}}-A)-\frac{1}{2}(V_{\mathrm{DD}}-A)^2\right) \tag{31}$$

Using Eqs. (20), (24), and (29)–(31), we can obtain the following conditions:

$$C_{\mathrm{tr}} > \frac{\beta_{\phi_0}}{R_{\mathrm{p}}} or \frac{\beta_0}{R_{\mathrm{p}}}, \tag{32}$$

where

$$\beta_{\phi_0} = \frac{\pi AL(L/3 + 2k_{\mathrm{tr}})}{\mu(V_{\mathrm{DD}} - V_{\mathrm{th}}/2)^2}, \tag{33}$$

$$\beta_0 = \frac{\pi AL(L/3 + 2k_{\mathrm{tr}})}{\mu\left((V_{\mathrm{DD}} + A - V_{\mathrm{th}})(V_{\mathrm{DD}} - A) - (V_{\mathrm{DD}} - A)^2/2\right)}. \tag{34}$$

In Eq. (32), larger one is dominant in β_{ϕ_0} and β_0. This condition gives the minimum value of the parasitic capacitances in the cross-coupled transistors required to oscillate the VCO.

Using Eqs. (16) and (32), the oscillation frequency of a VCO ω must satisfy

$$\omega < \frac{1}{\sqrt{L_{\mathrm{s}}\left(C + C_{\mathrm{L}} + \beta_{\mathrm{n}}/R_{\mathrm{p}}\right)}}, \tag{35}$$

where n is ϕ_0 or 0. Using Eq. (25), the relationship between ω and Q_L can be expressed by

$$Q_{\mathrm{L}} > \frac{\beta_{\mathrm{n}}\omega}{1 - \left(\frac{\omega}{\omega_0}\right)^2} \equiv f(\omega), \tag{36}$$

where $\omega_0(= 1/\sqrt{L_s C_L})$ is the self-resonance frequency of the inductors.

2.3 Switched-Capacitor Array

In this section, the effect of a switched-capacitor array on the oscillation frequency and the quality factor is derived. Basically, a switched-capacitor array is used to obtain a wider frequency tuning range (FTR) for the required VCO gain K_{VCO}. If teh parasitic capacitance of a switch is too large, it is unable to turn off at a high frequency. However, when the size of the switch is too small, the quality factor of the resonator becomes small owing to the series resistance of the transistor. Therefore, there is a trade-off between the tuning range and the quality factor. FTR is defined by the following equation.

$$FTR = \frac{\omega_{\max} - \omega_{\min}}{\omega_{\mathrm{center}}} = \frac{\omega_{\max} - \omega_{\min}}{\frac{1}{2}(\omega_{\max} + \omega_{\min})} \equiv \gamma \qquad (37)$$

$\omega_{\max}$ and $\omega_{\min}$ are the angle frequencies when the switch is turned off and on. The parasitic capacitance of the switch can be defined by WC_{SW}, where C_{SW} is the capacitance per channel width. Actually, drain and source nodes have parasitic capacitances along with the substrate. However, these capacitances have series resistances, so their effect is not large. Thus, the capacitances are approximately included in the drain-gate and source-gate capacitances in Fig. 6. Here, α is defined as

$$\alpha C_{\mathrm{mim}} = WC_{\mathrm{SW}}, \qquad (38)$$

where α is usually less than 1/10. $\omega_{\max}$ and $\omega_{\min}$ are obtained by the following equations.

$$\omega_{\max} = \frac{1}{\sqrt{L_s(C_L + C_{\mathrm{tr}} + WC_{\mathrm{SW}}/2)}} \qquad (39)$$

$$\omega_{\min} = \frac{1}{\sqrt{L_s(C_L + C_{\mathrm{tr}} + C_{\mathrm{mim}}/2)}} \qquad (40)$$

Using Eqs. (37)–(40), C_{mim} is expressed by the following equation.

$$C_{\mathrm{mim}} = \frac{16(C_L + C_{\mathrm{tr}})\gamma}{(1-\alpha)\gamma^2 - 4(1+\alpha)\gamma + 4(1-\alpha)} \qquad (41)$$

R_{on} is expressed by the following well-known equation:

$$R_{\mathrm{on}} = \frac{L}{\mu C_{ox} W(V_{gs} - V_{th})} = \frac{K_R}{W}. \qquad (42)$$

Here, K_R is a constant of proportionality. Basically, the switched capacitor is split into a binary array, and the channel width W of the switched transistor is proportional to the MIM capacitance for each stage. Thus, the quality factor of the switched capacitor is constant for each stage; thus, the total quality factor and capacitance can be estimated from taht of a single switched capacitor as shown in Figs. 5 and 6.

The following equation can be derived from Eqs. (38)–(42).

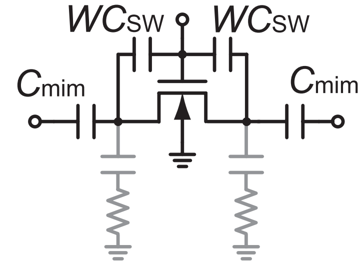


Fig. 6 Switched capacitor.

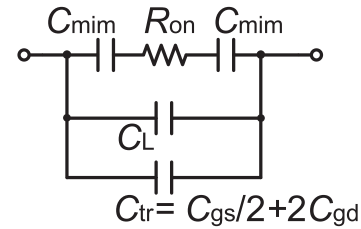


Fig. 7 Equivalent circuit of switched capacitor.

$$C_{\mathrm{mim}} R_{\mathrm{on}} = \frac{K_R C_{\mathrm{SW}}}{\alpha} \qquad (43)$$

Figure 7 shows an equivalent circuit of the switched capacitors when the switch is turned on. In this case, the quality factor of the capacitors is calculated by the following equation.

$$\begin{aligned} Q_C &= \frac{\mathrm{Im(Y)}}{\mathrm{Re(Y)}} \\ &= \frac{2}{\omega C_{\mathrm{mim}} R_{\mathrm{on}}} + \frac{(C_L + C_{\mathrm{tr}})}{\omega C_{\mathrm{mim}}^2 R_{\mathrm{on}}}[4 + (\omega C_{\mathrm{mim}} R_{\mathrm{on}})^2] \end{aligned} \qquad (44)$$

Using Eqs. (41), (43), and (44), Q_C is expressed by the equation

$$\begin{aligned} Q_C = &\frac{2\alpha}{\omega K_R C_{\mathrm{SW}}} + \frac{\alpha}{\omega K_R C_{\mathrm{SW}}}\left[4 + \left(\frac{\omega K_R C_{\mathrm{SW}}}{\alpha}\right)^2\right] \\ &\frac{(1-\alpha)\gamma^2 - 4(1+\alpha)\gamma + 4(1-\alpha)}{16\gamma}, \end{aligned} \qquad (45)$$

where K_R and C_{SW} depend on the CMOS process. Here, the feedthrough capacitance shown in Fig. 6 is neglected in the equivalent circuit in Fig. 7.

3. Calculation and Simulation Results

3.1 Maximum Oscillation Frequency

Figure 8 shows the calculation result obtained using Eq. (36). The parameters of the inductor and transistor used in this calculation are derived from a commercial PDK for a 180 nm CMOS process. Table 1 shows the configuration of this inductor. The intersection of Q_L and $f(\omega)$ gives the maximum oscillation frequency. This result is obtained by

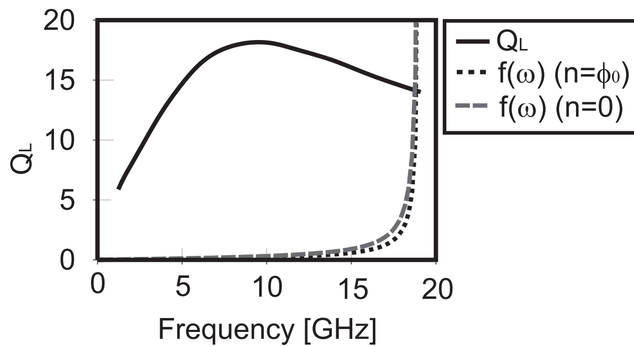


Fig. 8 Relationship between the Q_L and oscillation frequency.

Table 1 Configuration of on-chip inductor.

Number of turns	Inner diameter	L_s	C_L	Self-resonance
3	50 μm	1.7 nH	40 fF	19.1 GHz

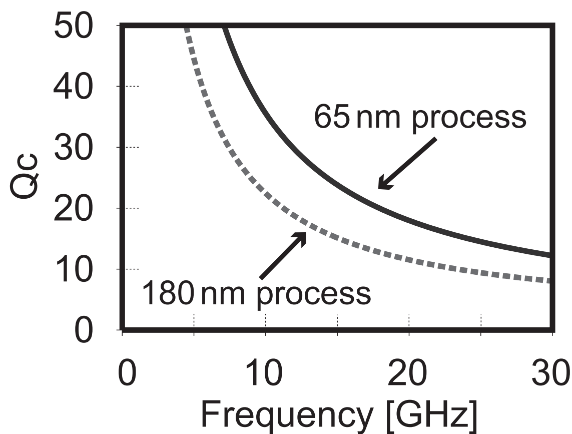


Fig. 9 Quality factor of capacitors.

calculating A to be 1.3 V and C to be 0. In this case, β_0 is dominant; therefore, the maximum oscillation frequency calculated by Eq. (36) is 18.8 GHz. This result, considering the self-resonance frequency of the inductor, shows that the effect of the parasitic capacitances in cross-coupled transistors on the oscillation frequency is not large.

3.2 Optimization of Switched Capacitors

Figure 9 shows the calculation results obtained using Eq. (45) for 65 nm and 180 nm CMOS process parameters with $\alpha = \gamma = 0.1$. This result shows that the quality factor of capacitors will be improved by the use of a more advanced process. The quality factor of resonators Q_{tank} is obtained by the following equation.

$$Q_{\text{tank}} = \frac{Q_L Q_C}{Q_L + Q_C} \tag{46}$$

Figure 10 shows the calculation and simulation results for the quality factor of resonators. In this figure, the lines show the result of the calculation using a Eq. (46) and the ploted

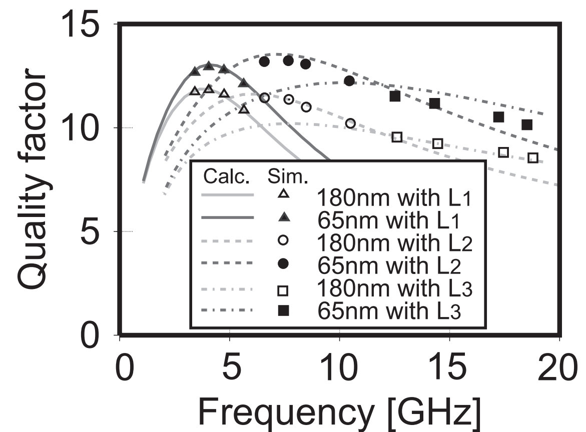


Fig. 10 Quality factor of resonators.

Table 2 Configuration of inductors.

	Number of turns	Inner diameter	L_s	C_L	Self-resonance
L_1	3	100 μm	3.44 nH	68.6 fF	10.4 GHz
L_2	2	80 μm	1.26 nH	30.5 fF	25.7 GHz
L_3	1	120 μm	0.643 nH	12.2 fF	56.8 GHz

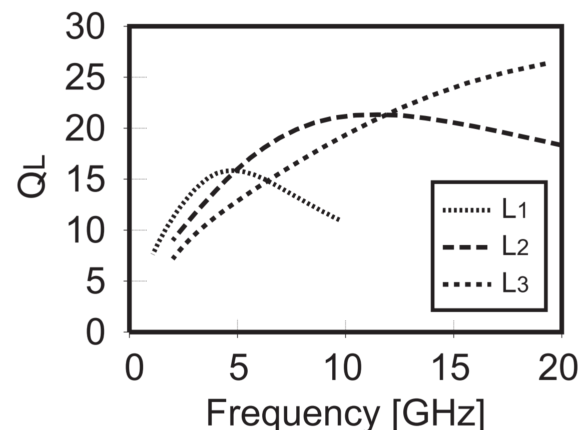


Fig. 11 Quality factor of three types of inductor.

points express the simulation result for the resonators. These two results are in good agreement. The calculation is performed using the results shown in Fig. 9 for the three types of inductors specified in Table 2, the quality factors of which are shown in Fig. 11. In this simulation, the switched capacitor is designed to obtain 10% of FTR using a single switched capacitor, and the ratio between the capacitance C_{mim} and the parasitic capacitance of the switch is equal to 10:1. The capacitance of the MIM capacitor is derived from Eq. (41), where $\alpha = \gamma = 0.1$, and the size of the switch is derived from Eq. (38). This result shows that the simulation result for the quality factor is in good agreement with the calculated result. The difference between the calculation and simulation results in Fig. 10 is caused by the feedthrough capacitance of the on-state as shown in Fig. 6.

In general, the figure of merit (FoM) is used to evaluate the performance of VCOs. FoM is the phase noise nor-

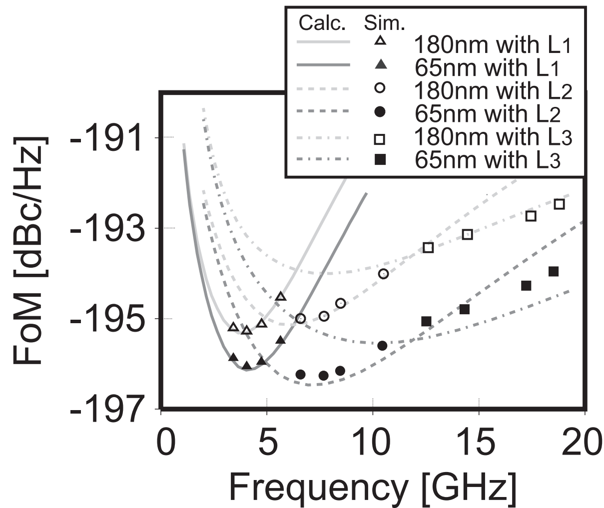


Fig. 12 FoM calculated using the results in Fig. 10.

malized by the oscillation frequency, offset frequency and power consumption, and can be defined by the following equation [9].

$$FoM = 10\log\left(\frac{\mathrm{k}TV_{\mathrm{DD}}}{2AQ_{\mathrm{tank}}{}^{2}\times 1\,\mathrm{mW}}\right) \tag{47}$$

Figure 12 shows the calculated FoM using the results in Fig. 10 and Eq. (47). It is assumed that the ratio of V_{DD} to A is 2:1. FoM was improved by using a 65 nm CMOS process that obtained using the with 180 nm process, and the difference in the FoM for the two processes was 2 dB at 10 GHz.

4. Conclusions

In this paper, the minimum transistor size and the degradation of the quality factor caused by a switched-capacitor array are analytically estimated, and the maximum oscillation frequency of VCOs is also derived from an equivalent circuit considering parasitic capacitances. The minimum transistor size is derived from the oscillation amplitude, and the design parameters of the switched-capacitor array can be determined by the frequency-tuning range.

According to an experiment using 180 nm and 65 nm CMOS process parameters, the parasitic capacitances of transistors have less effect than that of the switched-capacitor array, and the quality factor of the switched-capacitor array can be improved by the use of more advanced process owing to the higher f_{T}. The calculated FoM of the VCO assuming a 65 nm CMOS process is 2 dB better than that of the VCO with a 180 nm process, it corresponding to a 2 dB improvement in the phase noise for the same power consumption.

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