PAPER Special Section on Analog Circuits and Related SoC Integration Technologies

# A Wide-Tunable LC-Based Voltage-Controlled Oscillator Using a Divide-by-N Injection-Locked Frequency Divider

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**SUMMARY** This paper proposes a novel wideband voltage-controlled oscillator (VCO) for multi-band transceivers. The proposed oscillator has a core VCO and a tuning-range extension circuit, which consists of an injection-locked frequency divider (ILFD) and flip flop dividers. The two-stage differential ILFD generates quadrature outputs and realizes two, three, four, and six of divide ratio with very wide output frequency range. The proposed circuit is implemented by using a 90 nm CMOS process, and the chip area is $250 \times 200\,\mu m^2$. The measured result achieves continuous frequency tuning range of 9.3 MHz-to-5.7 GHz (199%) with −210 dBc/Hz of figure-of-merit ($FoM_T$).

***key words:*** *CMOS, VCO, divider, inductor*

## 1. Introduction

Recently, Si CMOS technology has provided high-density integration, high frequency performance and low cost, and the technology also realizes CMOS RF wireless circuits even if more than 60 GHz transceivers. On the other hand, multi-band wireless circuits are required due to commercial demands. Recent wireless mobile terminals have to provide considerably-many wireless communications, e.g., cellular phone including GSM/UMTS/LTE/WiMAX, short-range data communication like WLAN a/b/g/n, Bluetooth, UWB, broadcasting services like GPS, DTV, etc. The frequency range utilized such the consumer wireless applications is very wide and spreading from 400 MHz to 10 GHz.

For mobile terminals, smaller size and lower power consumption are required. However, the present multi-standard RF front-end consists of several LNAs, VCOs, Mixers, and PAs for each frequency band. A multi-standard RF front-end implemented in a single chip is required for such smaller size, lower power, and more flexible wireless communication terminals. The software defined radio (SDR) has been studied [1], and the multi-standard RF front-end is also needed to realize the SDR with feasible power consumption. Several multi-standard RF front-ends have been proposed. As one of the multi-standard RF front-end, a reconfigurable RF circuit architecture have been proposed [2], which aims to realize dynamic reconfiguration for multi functions and self compensation of PVT with variable bias tuning and switches. Such the digital-assisted architectures are suitable for fragile CMOS circuits. The digital radio processor (DRP) for Bluetooth and GSM/EDGE [3] and the software-defined radio receiver [1] have been reported, which are promising as a multi-band down-converter. All of these RF front-ends require a wideband-tunable VCO, which is an indispensable component for the multi-band radio. This paper proposes such the wideband VCO as 9 MHz to 6 GHz. Lower frequency than 400 MHz is also important for clock generation as well as wireless applications.

To obtain wide frequency tuning range, varactor and switched-capacitor array are commonly utilized for CMOS VCOs [4], [5]. However, the varactor has smaller capacitance ratio, and the ratio of the maximum-to-minimum capacitance of a typical varactor in CMOS technology is around 4-6 [6]. It limits the frequency tuning range to a ratio of approximately 2-2.5. The switched-capacitor array also has limitation of quality factor. Too large switch causes larger parasitic capacitance even though it contributes to reduce on-resistance.

Switch-less dual-band transformer-based VCOs that covers a wide frequency range have been reported in [7], [8]. Another architecture that uses a similar mode switching concept, as shown in [9], reuses the internal turn of a single inductor to generate the second oscillation mode in a switch-less resonator. VCO using a variable MEMS inductor achieves wide-tuning range with superior phase noise characteristics [10]. However, it has still been difficult for these pure CMOS VCOs to obtain wide-tuning range with adequate phase noise.

Recently, several wideband VCOs have been reported for multi-standard transceivers. VCOs in [1], [11] uses LC-VCO and frequency dividers as shown in Fig. 1(a). The frequency divider can generate lower divided frequency range. If the VCO has ±33% of frequency tuning range, correspond to e.g., 1-to-2 GHz, the frequency divider can extend continuous frequency range such as 0.5-to-1 GHz. However, the tuning range of ±33% is very wide, and it causes the phase noise degradation. Actually, the frequency tuning of the VCO in [1] is not continuous even though it uses 2 LC-VCOs. The frequency synthesizer in [11] realizes continuous tuning. However, it uses 2 LC-VCOs and layout area is large.

Frequency-tuning-range extension techniques using mixers have been reported as shown in Fig. 1(b) [8], [12]–[16]. The mixer contributes to reduce a frequency tuning range required for LC-VCOs to ±20%.

The wideband VCO proposed in [12] uses a tuning-

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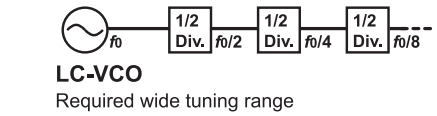
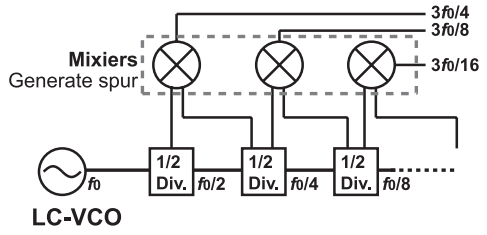



(a) Wideband VCO using divide-by-2 frequency dividers.




(b) Wideband VCO using frequency dividers and mixers.

**Fig. 1** The conventional wideband VCO architectures.

range extension technique using a differential VCO, a mixer, and dividers, which realizes very wide frequency range with good $FoM_T$. However, the VCO does not generate I/Q signals, and it has some spurious tones generated by the mixer. The VCO in [8] uses the transformer to obtain the wider tuning range, and it also uses the mixers to generate the divided frequencies. The mixer contributes to reduce the required frequency tuning range of the VCO. On the other hand, it also generates spurious tones. The spurious tone is a critical problem, especially for multiband transceivers. In addition, the continuous tuning is also not confirmed in the measurement.

This paper proposes a wideband LC-based VCO utilizing a novel frequency extension architecture, which realizes wider tuning range with lower power, smaller layout area, and lower phase noise. The proposed VCO consists of a differential LC-VCO and an injection-locked frequency divider (ILFD). The 2-stage differential ILFD can generate quadrature outputs without spurious tones, and divide ratio of the ILFD can be switched to 2, 3, 4, and 6 by the direct-injection topology. Thus, the proposed LC-based VCO achieves 9 MHz-to-6 GHz of continuous tuning range with the following FF frequency dividers [17].

## 2. Wideband VCO Architecture

Figure 2 shows the proposed VCO architecture, which consists of a differential LC-VCO, an injection-locked frequency divider (ILFD), and seven flip flop frequency dividers. The proposed architecture aims to achieve wider tuning-range with lower power consumption and lower phase noise, so a differential VCO and a novel compact frequency-extension circuit are employed. The conventional frequency extension technique using SSBM requires at least one QVCO. The phase noise of differential VCOs is usually better than that of QVCOs, and the frequency tuning range of differential VCOs is wider. Thus, the proposed architecture utilizes a differential VCO oscillating at 2 times higher frequency, and, in addition, layout area and power consumption can be saved.

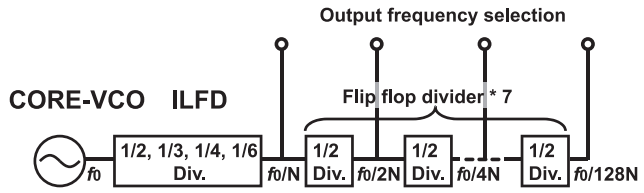



**Fig. 2** The proposed VCO architecture.

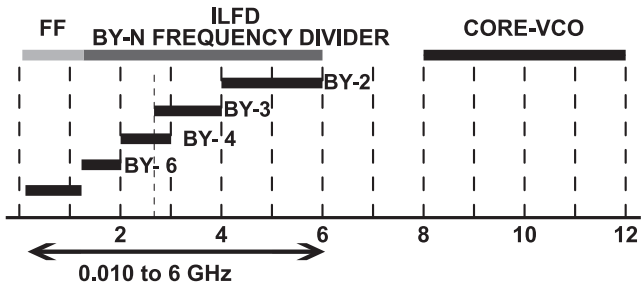



**Fig. 3** The frequency plan of the proposed architecture.

Figure 3 shows frequency plan of the proposed architecture, and 1/2 $f_0$, 1/3 $f_0$, 1/4 $f_0$, and 1/6 $f_0$ are generated by the injection-locked frequency divider. The incident frequency $f_0$ is generated by the core VCO, and it should have more than 40% of frequency tuning range. For example, if the LC-VCO has 8-to-12 GHz of frequency tuning range, the ILFD can generate 1.33-to-2 GHz, 2-to-3 GHz, 2.67-to-4 GHz, and 4-to-6 GHz with divide-by-6, -by-4, -by-3, and -by-2, respectively. Lower frequency range than the above can be generated by the flip-flop dividers as shown in Fig. 2. The divider consists of a static flip-flop provided as a standard logic cell. In this work, a divide-by-*N* ILFD is utilized instead of mixers, so wider output frequency range and spurious-less output can be obtained.

The proposed architecture has the following advantages: 1) only 40% of frequency tuning range is required for the core VCO, 2) higher frequency oscillation contributes to obtain higher-Q inductor, and 3) to reduce layout area of on-chip inductor. The ILFD utilized in the proposed VCO has multiple divide ratios, so only 40% of frequency tuning range is required to realize continuous frequency chain of the divided signals. In this case, 40% of frequency tuning range means that the upper-limit frequency is 1.5 times higher than the lower-limit, e.g., 8-to-12 GHz. Moreover, on-chip inductors tend to have higher Q around 10 GHz [18], and it also contributes to reduce the layout area.

### 2.1 Differential LC-VCO

A NMOS-cross-coupled LC-VCO is employed for the core VCO, which has feedback path to improve the phase noise. Figure 4 shows the schematic of the core VCO, and a switched capacitor array is utilized for coarse tuning to obtain more than 40% of frequency tuning range. $V_{ctrl}$ is a control voltage from the charge pump in PLL, and $V_{var}$ provides a DC bias voltage to varactors. Gate nodes of cross-coupled

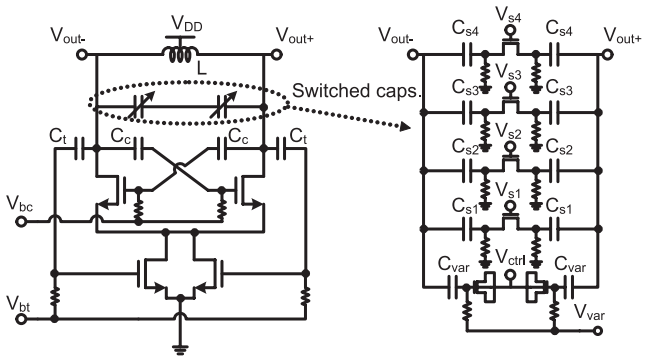



**Fig. 4** The core VCO schematic used in the proposed wideband VCO.

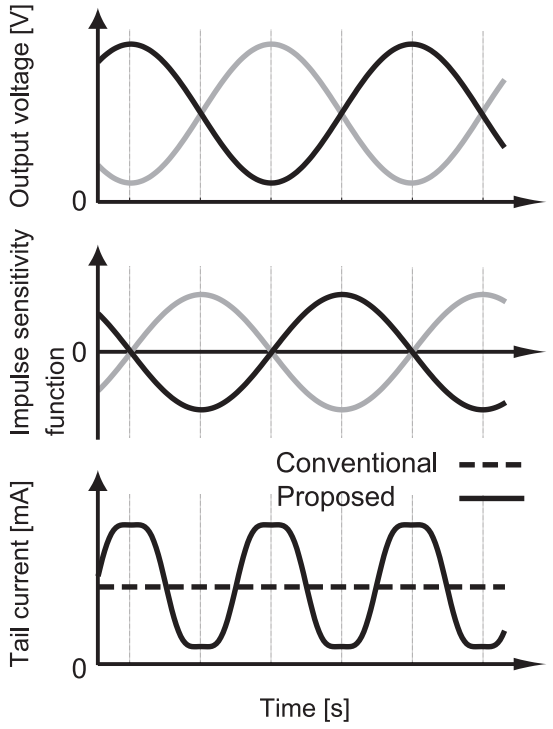



**Fig. 5** Tail current control considering *Impulse Sensitivity Function*.

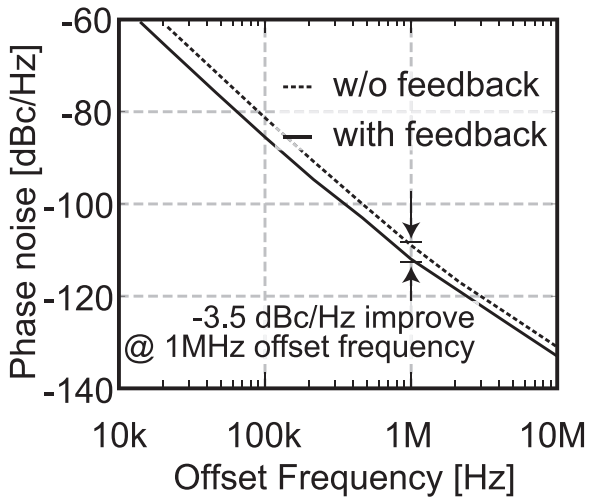



**Fig. 6** Phase noise comparison with or without the feedback.

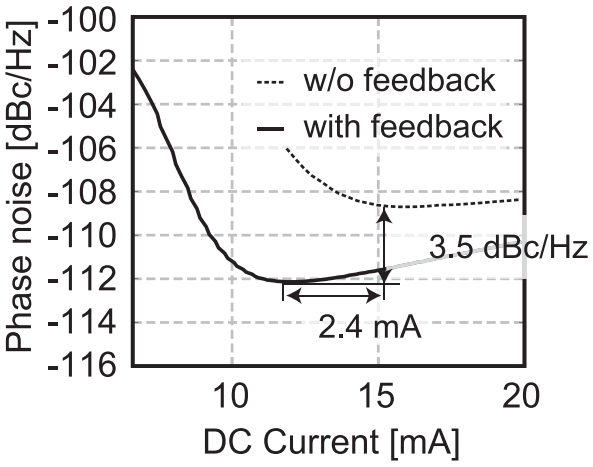



**Fig. 7** Phase noise versus tail current.

transistors are connected through capacitors $C_c$, and a gate bias voltage $V_{bc}$ is supplied through large resistance. The bias voltage $V_{bc}$ should be low from the view point of Impulse Sensitivity Function (ISF) [19].

A class-C VCO is proposed to improve the phase noise characteristics [20], which achieves very low phase noise with −196 dBc/Hz of FoM. Gate bias voltage of cross-coupled transistors is lower than threshold voltage for the class-C operation. It is, however, a little difficult to apply this technique to the wideband VCO because the class-C VCO needs larger-size cross-coupled transistors to obtain sufficient current with lower gate bias. The proposed VCO needs a higher-frequency and wider-tuning operation, so the VCO used in this paper has near class-C operation with above-threshold gate bias.

Instead of a deep-biased class-C operation, a switching-bias technique is employed [21], and 1/f noise can be reduced by swinging bias current. The technique has been utilized for ring oscillators, and it can also be applied to LC-VCOs. The switching of tail transistors forces releasing trapped electron, which contributes to reduce 1/f noise. The switching is realized by the tail feedback as shown in Fig. 4. The output signals are connected to the tail-transistor gates through the feedback capacitors $C_t$, and $V_{bt}$ supplies a bias voltage. The tail current is the sum of two tail transistors, and the current has $2f_0$ frequency as shown in Fig. 5. Figure 5 also shows the relationship between oscillation signal, ISF, and tail current. The modulation of tail current is effective from the view point of ISF, because the tail current flows at the timing which has smaller ISF values. Thus, the proposed VCO can reduce the channel noise as well as the 1/f noise.

Figure 6 shows a phase-noise comparison between the tail-feedback and non-tail-feedback VCOs, which are realized with or without the feedback capacitors $C_t$. In this simulation, channel width of tail transistors are 3 times larger

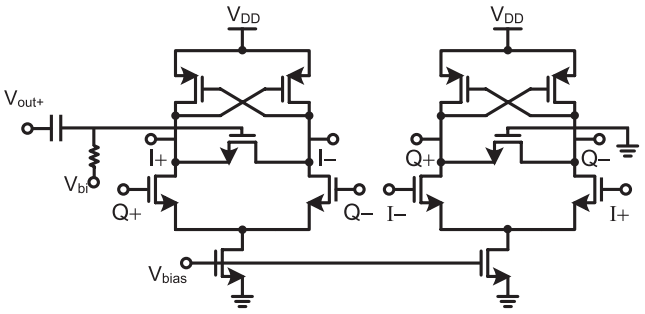



**Fig. 8** ILFD schematic used in the proposed wideband VCO.

than that of the non-feedback one. It is simulated by using CMOS 90-nm design parameters. In this comparison, the tail-feedback VCO has the feedback capacitor $C_t$ as shown in Fig. 4, and channel width of tail transistors are 3 times larger than that of the nonfeedback one. Figure 7 also shows the comparison as a function of tail current. The phase noise in Fig. 7 is at 1 MHz-offset. In this case, the tail-feedback VCO has 3.5 dB better phase noise at each bottom value, and FoM is 4.6 dB better.

### 2.2 Injection-Locked Frequency Divider

Figure 8 shows the schematic of the ILFD. A 2-stage ring-type differential frequency divider is employed to obtain I/Q outputs. The direct-injection technique is utilized for divide-by-$N$ operation. The core VCO output is injected from $V_{\text{out+}}$, and $V_{\text{bi}}$ is used to adjust the bias level of the injection signal. While programmable dividers using current-mode-logic FFs have large power consumption, the ILFD realizes smaller power consumption and higher frequency operation. In addition, the ILFD can realize very wide continuous frequency range like 1-to-6 GHz as free-run oscillation, and locking range and divide ratio can also be switched by the bias voltage $V_{\text{bias}}$.

To understand the multiple-modulus operation, the time-domain behavior is shown in Fig. 9. It shows the relationship between the divide ratio and the injection phase. The direct-injection ILFD has current injections at the crossing points as shown in Fig. 9. For the divide-by-2 operation, there are current injections at every crossing points. For the divide-by-3 operation, the incident signal can also synchronize ILFD waveform. However, only one of two injections meets the crossing point, and the locking range becomes half of the case of divide-by-2 operation. The divide-by-4 and -by-6 operations can also have injections at every crossing points while these operation modes have unnecessary injections as shown in Fig. 9. The unnecessary injection disturbs proportional waveform of ILFD outputs, which is considerable especially with large injection current. Thus, the unnecessary injection causes upper-limit of injection current even though large injection current contributes to obtain wider locking range for generic divide-by-2 ILFDs.

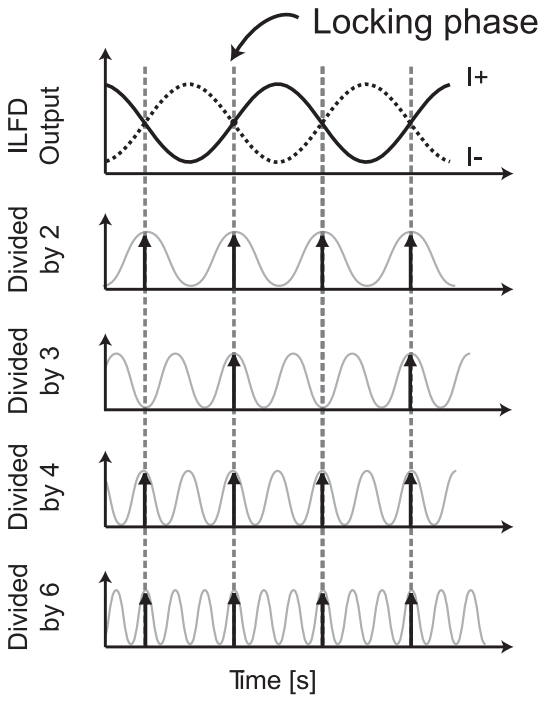



**Fig. 9** Injection of each divided ratio.

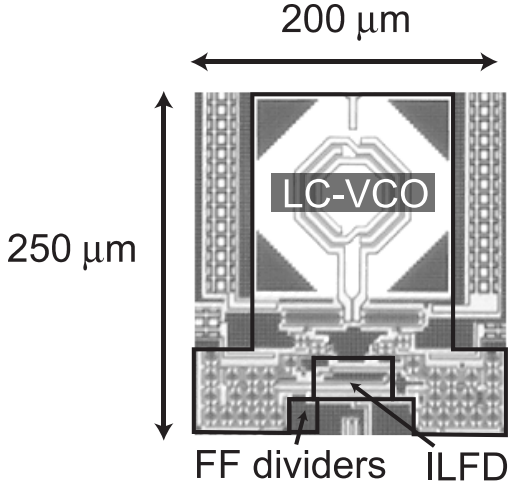



**Fig. 10** Chip micrograph of fabricated wideband VCO.

## 3. Measurement Results

Figure 10 shows a chip micrograph of the proposed wideband VCO, which is fabricated by using a 90 nm CMOS process. The core size is $250 \times 200\,\mu\text{m}^2$. The proposed circuit does not use a quadrature LC-oscillator, and the LC-resonance frequency of the proposed circuit is two times higher than the output frequency range of the ILFD, which contributes to reduce layout area. Signal Source Analyzer (Agilent E5052A) and Spectrum Analyzer (Agilent E4448A) were used for measurement. Table 1 summarizes the measured results.

Figure 11 shows the output spectrum of the ILFD for

divide-by-6 operation, which has the 2nd and the 3rd harmonics without spurious tones. The spectrum is measured at a single side of differential signal, and the 2nd harmonic can be canceled. Table 1 summarizes the measured results, Table 2 also shows measured phase noise and FoM for each divide ratio of ILFD. The proposed VCO achieves −184 dBc/Hz of FoM at 5.60 GHz, and 9.3 MHz-to-5.7 GHz output is obtained by the divide-by-$N$ ILFD and FF dividers in the measurement result. The total power consumption is 5.9–11.2 mW depending on output frequency. In the measurement, the oscillation frequency range is from 7.7 GHz to 11.4 GHz while it is from 8.7 GHz to 12.8 GHz in the simulation. The difference may be caused by paracitic inductances, which are not considered in the simulation. The frequency range of the ILFD is from 1.3 GHz to 6.1 GHz in the measurement, while the range is from 1.4 GHz to 6.6 GHz in the simulation. The free-running freuqency of the ILFD is adjusted by the bias voltage $V_{\mathrm{bias}}$. In this paper, FoM and $\mathrm{FoM_T}$ are utilized to evaluate frequency tuning range as well as the phase noise. FoM and $\mathrm{FoM_T}$ are defined by the following equations [22].

$$FoM = \mathcal{L}\{f_{\mathrm{offset}}\} - 20\log\left(\frac{f_{\mathrm{o}}}{f_{\mathrm{offset}}}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}}\right) \quad (1)$$

$$FoM_{\mathrm{T}} = \mathcal{L}\{f_{\mathrm{offset}}\} - 20\log\left(\frac{f_{\mathrm{o}}}{f_{\mathrm{offset}}} \cdot \frac{FTR}{10}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\ \mathrm{mW}}\right) \quad (2)$$

$$= FoM - 20\log\left(\frac{FTR}{10}\right) \quad (3)$$

where $\mathcal{L}\{f_{\mathrm{offset}}\}$ is phase noise, $f_{\mathrm{offset}}$ is offset frequency, $f_{\mathrm{o}}$ is center frequency, and $P_{\mathrm{DC}}$ is power consumption. FTR is frequency tuning range, which is defined as $(f_{\max} - f_{\min})/\frac{(f_{\max}+f_{\min})}{2}$ in percent figures. In this paper, table 2 shows $\mathrm{FoM_T}$, and the proposed VCO achieves −210 dBc/Hz of $\mathrm{FoM_T}$ with 9.3 MHz-to-5.7 GHz of continuous frequency tuning range.

Table 3 compares FoM and FTR of wide-FTR LC-VCOs reported in literature. The VCOs in [8], [11] and the proposed one can generate quadrature signals. The VCO in [11] uses 2 LC-VCOs, so the layout area is larger than the others. The VCO in [8] use a QVCO. However, it consists of two resonators using transformers, so the layout area is still large. The proposed VCO achieves the widest continuous tuning range and the best $\mathrm{FoM_T}$ simultaneously.

**Table 1** Measured VCO performance summary.

| | |
|---|---|
| Technology | FUJITSU 90 nm CMOS process |
| Supply voltage $V_{\mathrm{DD}}$ | 1.2 V |
| Power consumption of VCO core | 4.8–10.2 mW |
| Power consumption of ILFD | 1.0–1.3 mW |
| Power consumption of FF dividers | ∼ 0.1 mW |
| Total power consumption | 5.9–11.2 mW |
| Tuning range | 9.3 MHz–5.7 GHz<br>199% |
| Chip area | 250 $\mu$m × 200 $\mu$m |

## 4. Conclusion

This paper has proposed a novel wideband LC-VCO for multi-band applications. The VCO has the core VCO and

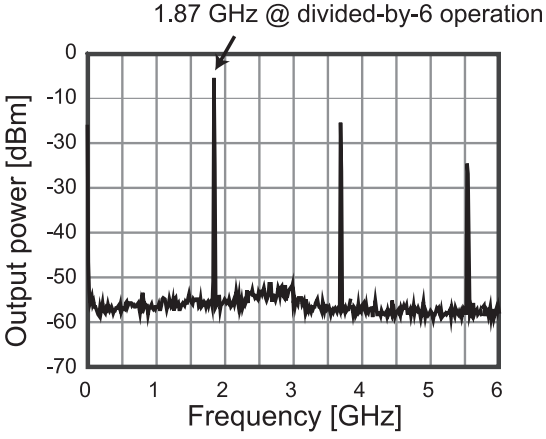



**Fig. 11** Measured ILFD output spectrum at 1/6 $f_0$.

**Table 2** Measured phase noise performances.

| Oscillation frequency | Phase noise @1 MHz offset | FoM | $\mathrm{FoM_T}$ |
|---|---|---|---|
| 5.6 GHz (1/2 $f_{\mathrm{o}}$) | −117 dBc/Hz | −184 dBc/Hz | −210 dBc/Hz |
| 3.7 GHz (1/3 $f_{\mathrm{o}}$) | −118 dBc/Hz | −182 dBc/Hz | −208 dBc/Hz |
| 2.8 GHz (1/4 $f_{\mathrm{o}}$) | −120 dBc/Hz | −181 dBc/Hz | −207 dBc/Hz |
| 1.9 GHz (1/6 $f_{\mathrm{o}}$) | −121 dBc/Hz | −179 dBc/Hz | −205 dBc/Hz |

**Table 3** Performance comparison.

| | This work | [8] | [11] | [12] |
|---|---|---|---|---|
| Architecture | VCO with ILFD | QVCO with mixers and dividers | 2 VCOs with divider | VCO with mixer and dividers |
| Divided ratio | 2, 3, 4, 6 | 2, 3, 4, 6, 8, 10 | 2, 4, 8, 16, … | 1/2, 2/3, 1, 4/3, 2 |
| Number of resonators | 1 | 2 | 2 | 1 |
| Technology | CMOS 90 nm | CMOS 90 nm | CMOS 45 nm | CMOS 0.18 $\mu$m |
| Output | Quadrature | Quadrature | Quadrature | Differential |
| Frequency range | 0.009–5.7 GHz | 1–10 GHz | 0.1–5.0 [GHz] | 0.98–6.6 [GHz] |
| Continuous | yes | — | yes | yes |
| Power consumption | 5.9–11.2 mW | 31 mW | 19.8 mW w/o dividers | 4.41–26.9 mW |
| $FoM$ | −184 dBc/Hz | −169 dBc/Hz | −183 dBc/Hz w/o dividers | −183 dBc/Hz |
| $FoM_{\mathrm{T}}$ | −210 dBc/Hz | −194 dBc/Hz | −209 dBc/Hz w/o dividers | −206 dBc/Hz |
| Layout area | 0.05 [ mm$^2$] | 0.29 [ mm$^2$] | 2.16 [mm$^2$] | 0.43 [ mm$^2$] |

the tuning-range extension circuit. A differential LC-VCO oscillates at two times higher frequency range than the output range, which contributes to reduce layout area of on-chip inductor. The upper-limit frequency of the core VCO is 1.5 times higher than the lower-limit. The injection-locked frequency divider and FF frequency dividers are utilized, and the ILFD can generate 1/2, 1/3, 1/4, and 1/6 of the core VCO frequency with quadrature outputs. In the measurement results, the proposed VCO performs 9.3 MHz-to-5.7 GHz continuous frequency tuning with −210 dBc/Hz of $\mathrm{FoM_T}$, which is fabricated by using a 90 nm CMOS process. The output spectrum has no spurious tones. The frequency tuning ratio (FTR) is 199%, and the chip area is $250 \times 200\,\mu\mathrm{m}^2$. The proposed VCO achieves the widest tuning range as a continuously-tunable LC-based VCO with the best $\mathrm{FoM_T}$.

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