A 2.4 GHz Fully Integrated CMOS Power Amplifier Using Capacitive Cross-Coupling

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Introduction

The 2.4GHz band is used for various wireless communications such as WiMAX, WLAN, Bluetooth, etc [3,5,7]. The band is one of the ISM bands, and we can use it without license and can realize relatively fast wireless communications. A power amplifier (PA) is one of key building blocks in RF transmitter. Conventionally, PA used to be implemented as an external component. Because of fabrication cost and small footprint size, a single-chip CMOS RFIC, including PA and the other building blocks, is demanded. Thus, this paper presents a fully integrated CMOS PA suitable for 2.4GHz band.

One of the headachy issues realizing an integrated PA is voltage stress on CMOS transistors. The impedance conversion using a transformer is a common technique to reduce voltage swing at the drain node. However, there is a trade-off between the voltage stress and the insertion loss of transformer. To overcome the problem, the proposed power amplifier has the following features. At first, a self-biased cascode topology is adopted [2]. The cascode topology can reduce effective gate-to-drain voltage, which contributes to relax the voltage-stress issue. On the other hand, the self-biased gate degrades gain, and layout area is enlarged by capacitors used in the bias part as demerits. Thus, the proposed PA employs a capacitive cross-coupling to solve the voltage-stress issue. The capacitive cross-couple also reduces the gate-drain capacitance, which contributes to improve reverse isolation. In addition, the bulky capacitors used in the bias part can be reduced.

Power Amplifier Design

Fig.1 shows a simplified circuit schematic of the proposed power amplifier. The PA employs a self-biased cascode topology with a capacitive cross-coupling, and thick gate-oxide transistors are utilized. A transformer is also used to obtain a large output power. Feedback resistances are used to improve a stability factor more than 1, and the output matching is optimized according to the load-pull simulation.

The proposed PA consists of two amplifier stages. The first stage is designed as a class-A cascode amplifier, and the second stage is implemented as a self-biased cascode amplifier with class-AB biasing.

The cascode configuration offers high stability and large knee voltage. Even if the drain voltage of the common-gate transistor varies, it keeps an almost constant voltage at both gate and source nodes. Thus, the common-source transistor also has an almost constant voltage at both drain and source nodes. Due to this feature, current flowing along the cascoded transistors does not vary so much. In other words, it realizes a high output impedance.

As one of the other considerations, the knee voltage has to be taken into account. The cascode configuration makes the knee voltage larger, and it reduces voltage operation region. On the other hand, the output voltage is separated to common-gate and common-source transistors. In terms of voltage stress, the cascode configuration accepts using a high supply voltage. As a result, the cascode configuration contributes to obtain higher output power.

In addition, thick gate oxide transistors are utilized due to the voltage-stress issue with a self-bias technique, which is explained as follows.

A. Self-Biased Cascode

Fig. 2 shows the self-biased cascode topology. As a feature of the self-biased cascode topology, v_{gd} can be reduced. When v_d arises to positive direction, v_g follows v_d. Thus, v_{gd} is reduced. When v_d decreases,

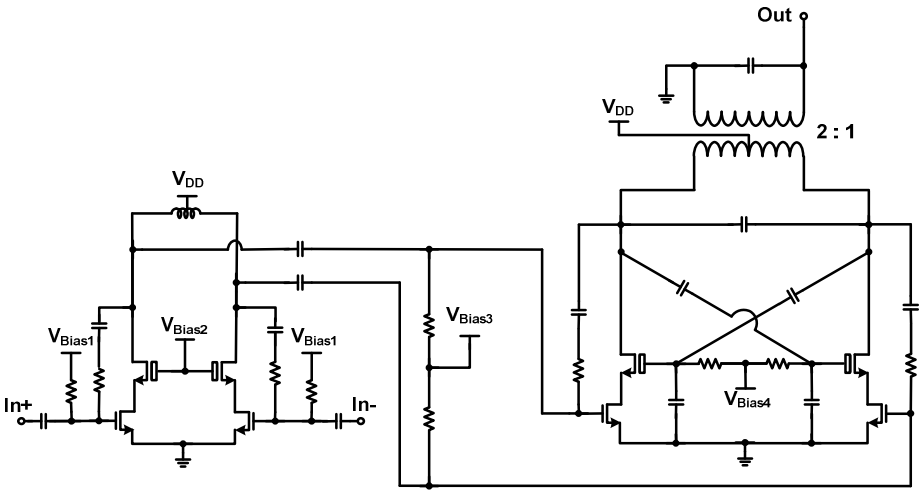

Fig. 1 Circuit schematic of the proposed CMOS power amplifier

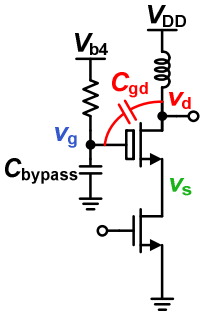

Fig. 2 Self-biased cascode

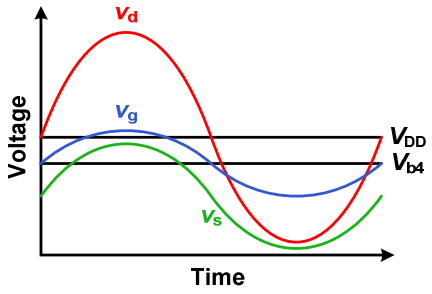

Fig. 3 Voltage waveforms vs. time

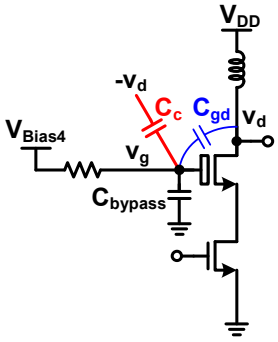

Fig. 4 Capacitive cross-coupling

the common-gate transistor enters the triode region. Fig. 3 shows the conceptual graph of voltage waveforms of the common-gate transistor terminals. If we neglected the gate-source capacitance, v_g would be expressed as follows.

$$v_g = \frac{C_{gd}}{C_{gd} + C_{bypass}} v_d \tag{1}$$

where C_{gd} is the gate-drain capacitance of the common-gate transistor, and C_{bypass} is the bypass capacitance. The self-biased cascode configuration has smaller gain as a drawback. Thus, it is used for only the second stage.

B. Capacitive Cross-Coupling

One of the most important issues for using a self-bias technique is layout size of capacitance. According to Eq.(1), the bypass capacitance C_{bypass} is determined by the gate-drain ca-pacitance C_{gd}. Transistors in the output stage are enormously large, so the gate-drain capacitance C_{gd} is also enormous, *e.g.*, several hundred pF. Thus, this paper proposes a capacitive cross-coupled topology. Conventionally, the capacitive cross-coupling is used for gain enhancement and impedance matching [1]. However, we use it in the PA to reduce the gate-drain capacitance.

Fig. 4 shows the half circuit of the capacitive cross-coupling. The cross-coupled capacitor C_c is connected to the opposite side of drain node, so it works as $-C_c$. Thus, Eq.(1) can be rewritten as follows.

$$v_g = \frac{(C_{gd} - C_c)}{C_{bypass} + (C_{gd} - C_c)} v_d \tag{2}$$

The comparison between Eqs.(1) and (2) shows that effective gate-drain capacitance can be reduced by the capacitive cross-coupling, which contributes to reduce the layout area of the bypass capacitance

(C_{bypass}). Though the layout area for inductor and transformer is dominant, the layout area for the bypass capacitor is not negligible. In addition, the reduction of feedback capacitance improves reverse isolation.

C. Transformer

The proposed power amplifier employs a transformer at output to obtain high output power and high PAE. The trans-former is implemented by using a 1P6M 0.18μm CMOS process. The top metal thickness is 4.6μm.

Fig. 5 shows the structural configuration of the transformer, and Fig. 6 shows Maximum Available Gain vs. frequency for both simulation and measurement. The turn ratio of trans-former is 2:1, so we can make the output impedance from 50Ω to 12.5Ω, ideally. A coupling coefficient is about 0.7. At 2.4 GHz, MAG is -1.05dB, and the conversion efficiency is 78.5%. The transformer is simulated by an electromagnetic field simulator (Ansoft HFSS). A TEG is measured by a 4-port network analyser, and the measured 4-port S-parameters are converted to mixed-mode ones. Open and short dummy pads are used for the de-embedding. The measurement and simulation results agree with each other.

Measurement Result

Fig. 7 shows the chip micrograph of the proposed power amplifier. It is fabricated in 0.18μm CMOS process using thick gate transistors and MIM capacitors. The total size of chip is 1.0×1.6 mm^2. The PA is evaluated with a 3.3-V power supply.

Fig. 8 shows the small signal S-parameters of the power amplifier. Red line is the simulation result, and blue line is the measurement result. It can be seen that the measurement result is slightly shifted to lower frequency due to model inaccuracy, but still there is very good correlation between the simulation and measurement results.

The CW large signal response is measured with an RF probe station. For differential measurement, an external 180-degree hybrid coupler is used at input side. Fig. 9 shows PAE_{max}, and P_{sat} vs. frequency, and Fig. 10 shows P_{out}, Gain, PAE(Power Added Efficiency) vs. P_{in}. PAE_{max} and P_{sat} are more than 31% and 27dBm, respectively, around 2.4GHz. In Fig. 10, the solid lines are the simulation results, and the dotted lines are the measurement results. The measured 1dB compression point is 25dBm. The measured PAE at P_{1dB} and PAE_{max}, P_{sat} are 26.8%, 34.3% and 27.7dBm, respectively. The power gain is 26.5dB.

Table I summarizes the performance of the 2.4GHz CMOS PA presented in this paper and shows the comparison with other 2.4GHz PAs.

Conclusion

The paper presented a 2.4GHz fully integrated CMOS power amplifier using capacitive cross-coupling, fabricated in 0.18μm CMOS. With a 3.3-V supply voltage, PAE_{max} and PAE at 1dB compression point are 34.3% and 26.8%. P_{1dB}, P_{sat}, and PG are 25.2dBm, 27.7dBm and 26.5dB, respectively. The advantages of the proposed capacitive-cross-coupled PA are the improvement of reverse isolation and the area saving.

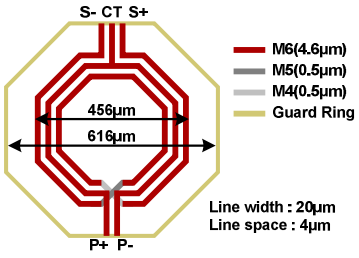

Fig. 5 Transformer

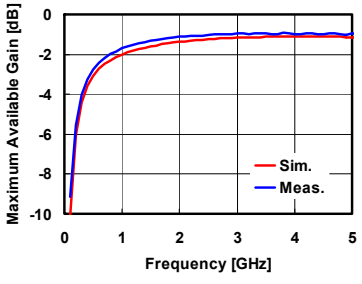

Fig. 6 Maximum Available Gain vs. frequency

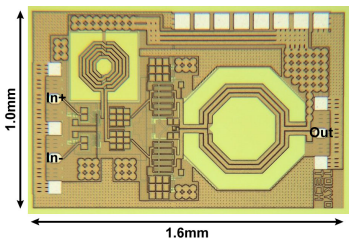

Fig. 7 Chip micrograph

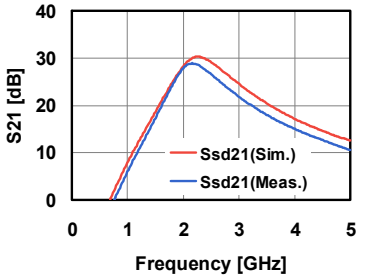

Fig. 8 S_{21} vs. frequency

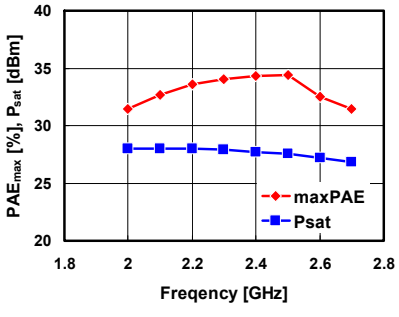

Fig. 9 PAE_{max}, P_{sat} vs. frequency

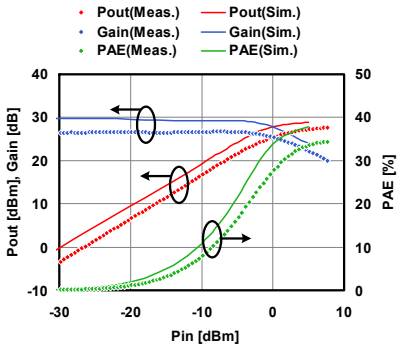

Fig. 10 P_{out}, Gain, PAE vs. P_{in}

Table I. Performance Comparison Of CMOS PAs

	Technology	**V_{DD}**	**Frequency**	**P_{1dB}**	**P_{sat}**	**PAE_{max}**	**Area**
[3]	65nm CMOS	3.3 V	2.4 GHz	26 dBm	28.3 dBm	35.3 %	0.31* mm^2
[4]	90nm CMOS	3.3 V	2.4 GHz	27.7 dBm	30.1 dBm	33 %	4.3 mm^2
[5]	90nm CMOS	3.3 V	2.3-2.7 GHz	31 dBm	32 dBm	48 %	2.3 mm^2
[6]	130nm CMOS	1.2 V	2.4 GHz	24 dBm	27 dBm	32** %	1.7 mm^2
[7]	180nm CMOS	3.3 V	2.4 GHz	24.5 dBm	-	31 % @1dB	1.7 mm^2
[8]	180nm CMOS	3.3 V	2.4 GHz	27 dBm	31 dBm	27 %	2.0 mm^2
This work	180nm CMOS	3.3 V	2.4 GHz	25.2 dBm	27.7 dBm	**34.3 %**	**1.6 mm^2**

* only output stage ** drain efficiency

Acknowledgement

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