A 2.4GHz Fully Integrated CMOS Power Amplifier Using Capacitive Cross-Coupling

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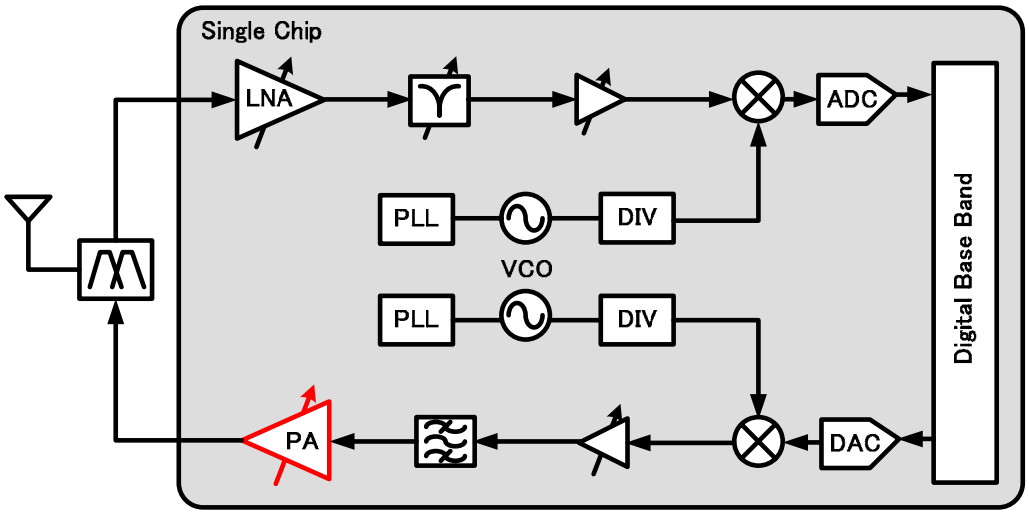
Introduction



- **PA (Power Amplifier)**

: A circuit used to convert a low-power RF signal into a larger signal of significant power at transmitter

- **2.4GHz**
  - **the frequency band which require no license**
  - **various wireless communication standards**
    : WiMAX, WLAN, Bluetooth, etc.

Introduction

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- **The reason for using capacitive cross-coupling**

High reliability of the voltage stress at output end

Using self-biased cascode topology

Area increase by bypass capacitor

Using Cross-coupling Capacitor

Reduce an area of bypass capacitor

Schematic

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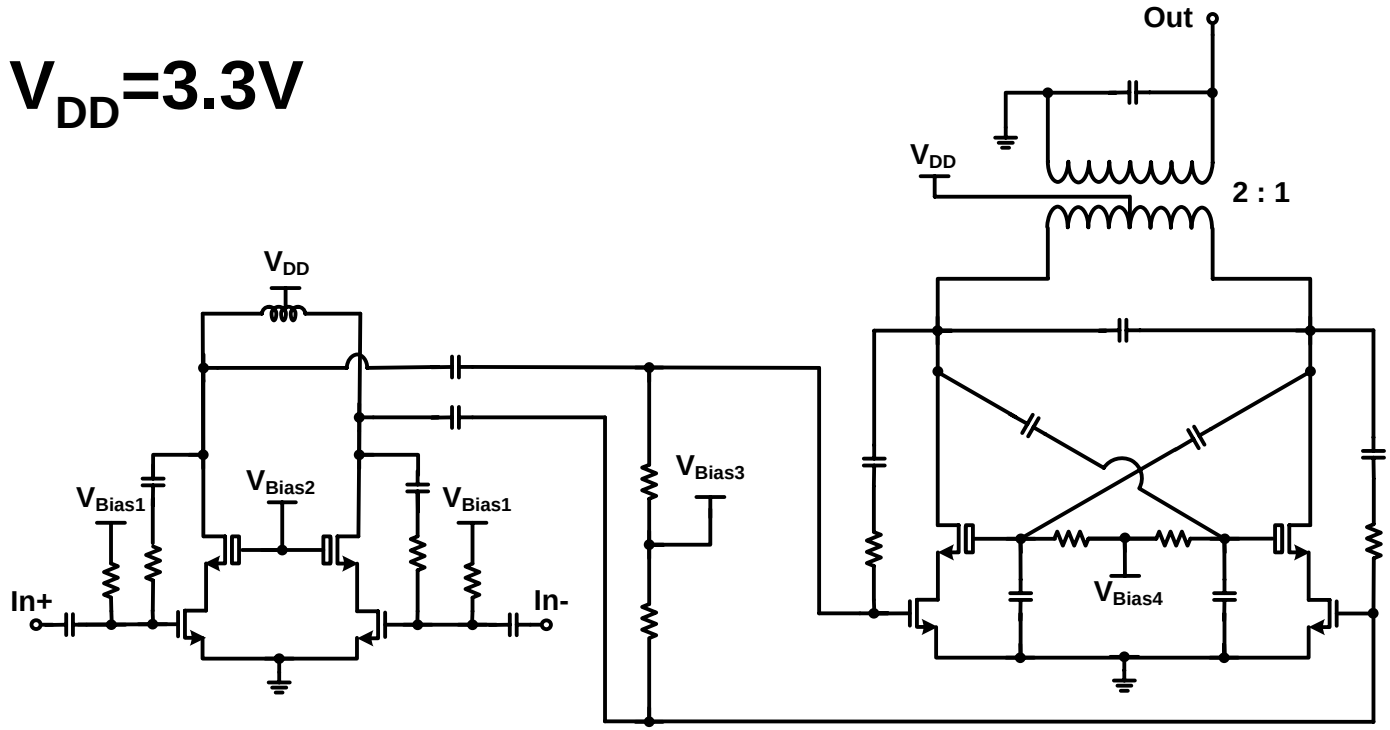
V_{DD}=3.3V



- Class-A bias(1st stage), Class-AB bias(2nd stage)
- Differential topology for achieving 3dB larger P_{out}
- Impedance matching by L, C, R

Proposed circuit

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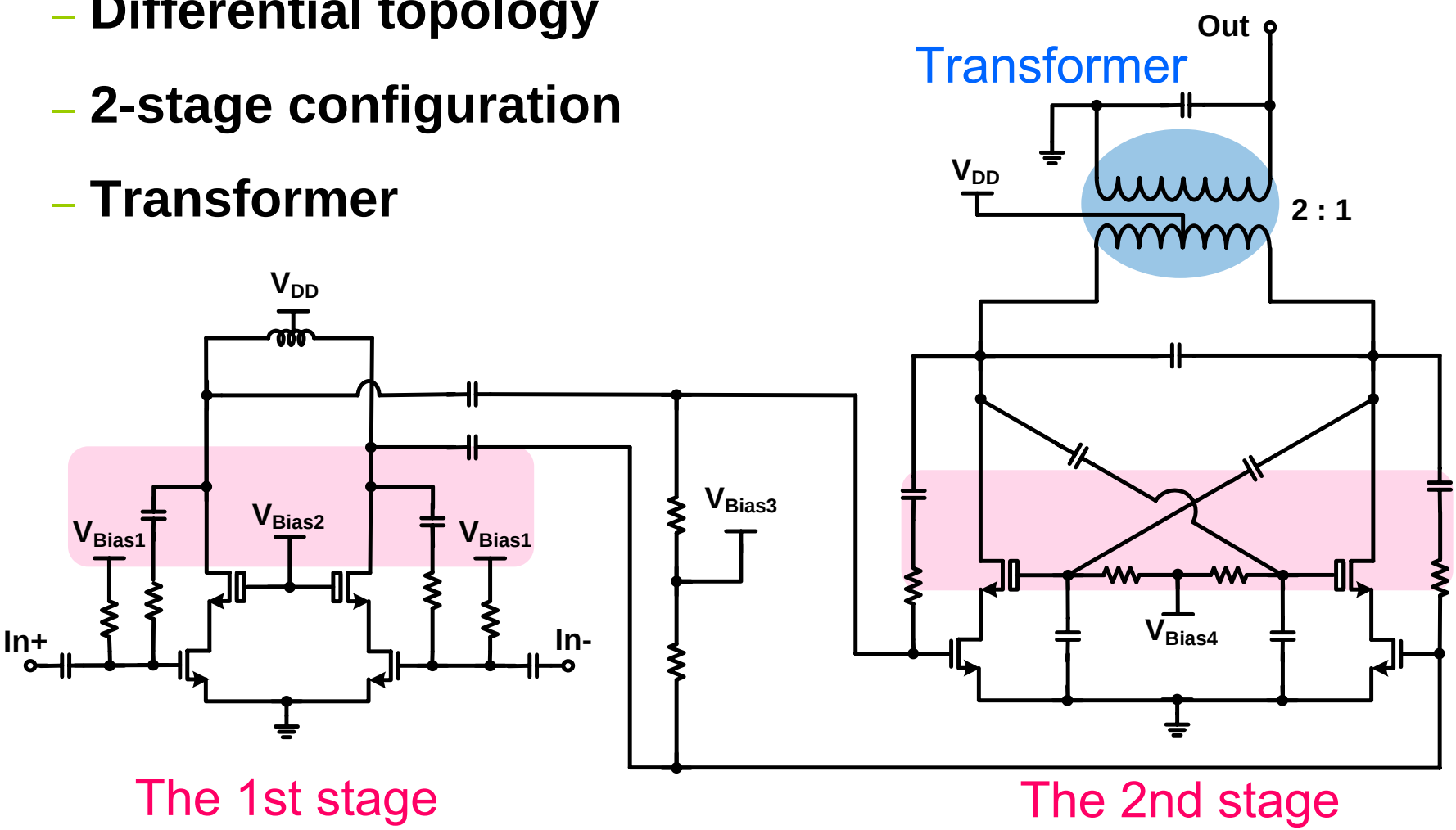
- To achieve a high output power
  - Differential topology
  - 2-stage configuration
  - Transformer



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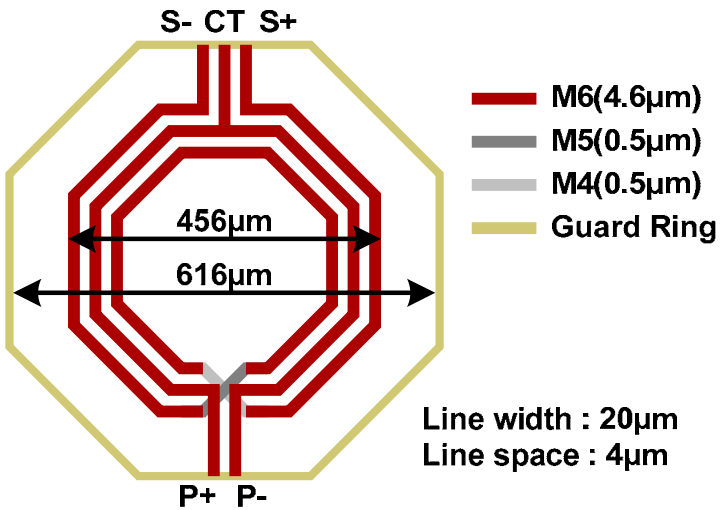
Transformer



- **Relation between P_{sat} & Z_{out}**

$$P_{sat} = \frac{\left(V_{DD}/\sqrt{2}\right)^2}{Z_{out}}$$

- **Theoretical maximum output power P_{sat}**

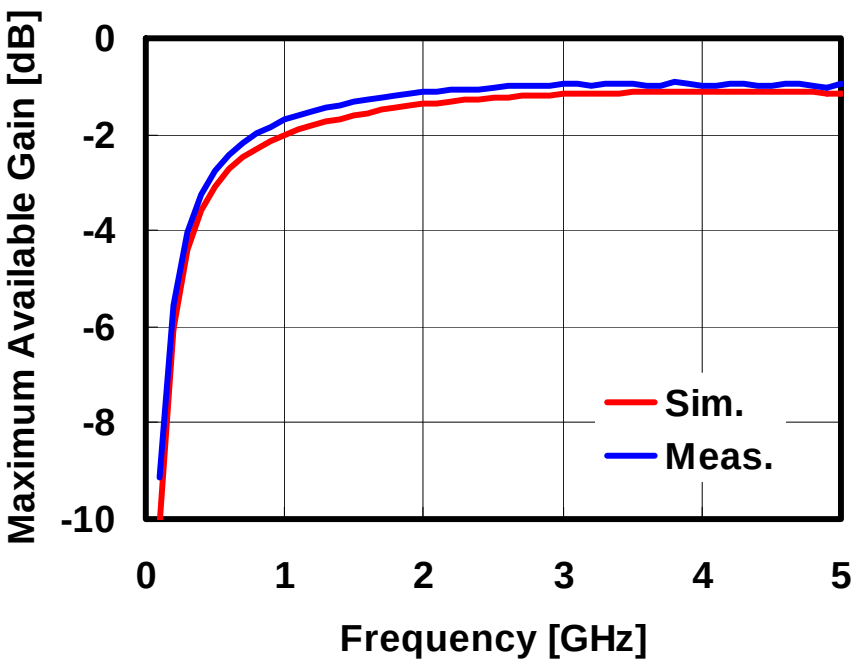
$$P_{sat} = \frac{\left(V_{DD}/\sqrt{2}\right)^2}{\left(\frac{1}{4}Z_{out}\right)} = \frac{\left(2\times 3.3/\sqrt{2}\right)^2}{\left(2\times\frac{1}{4}\times 50\right)}$$

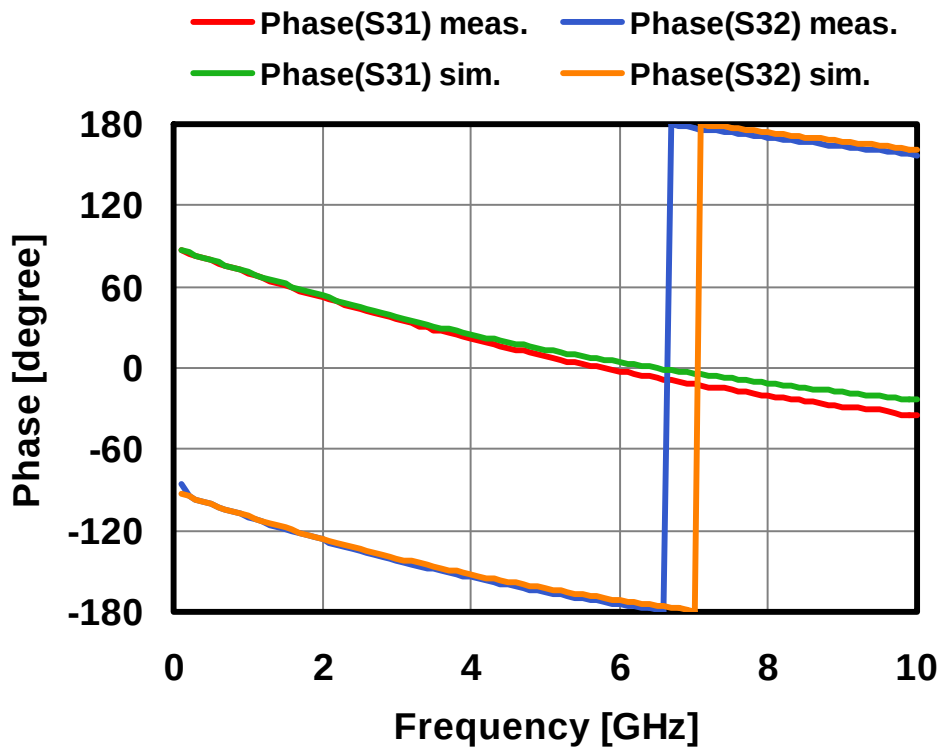
$$= 0.8712[\mathrm{W}] = 29.4[\mathrm{dBm}]$$

- **Turn ratio=2:1**
- **Z_{out} (50Ω)**
  → ¼ Z_{out}(12.5Ω)

Transformer

- Coupling coefficient = 0.7
- Maximum Available Gain(MAG) = -1.05 dB
- Conversion efficiency= $10^{(-1.05\text{dB}/10)} \times 100$ =78.5 %





- Measurement and simulation results agree with each other.

Proposed circuit

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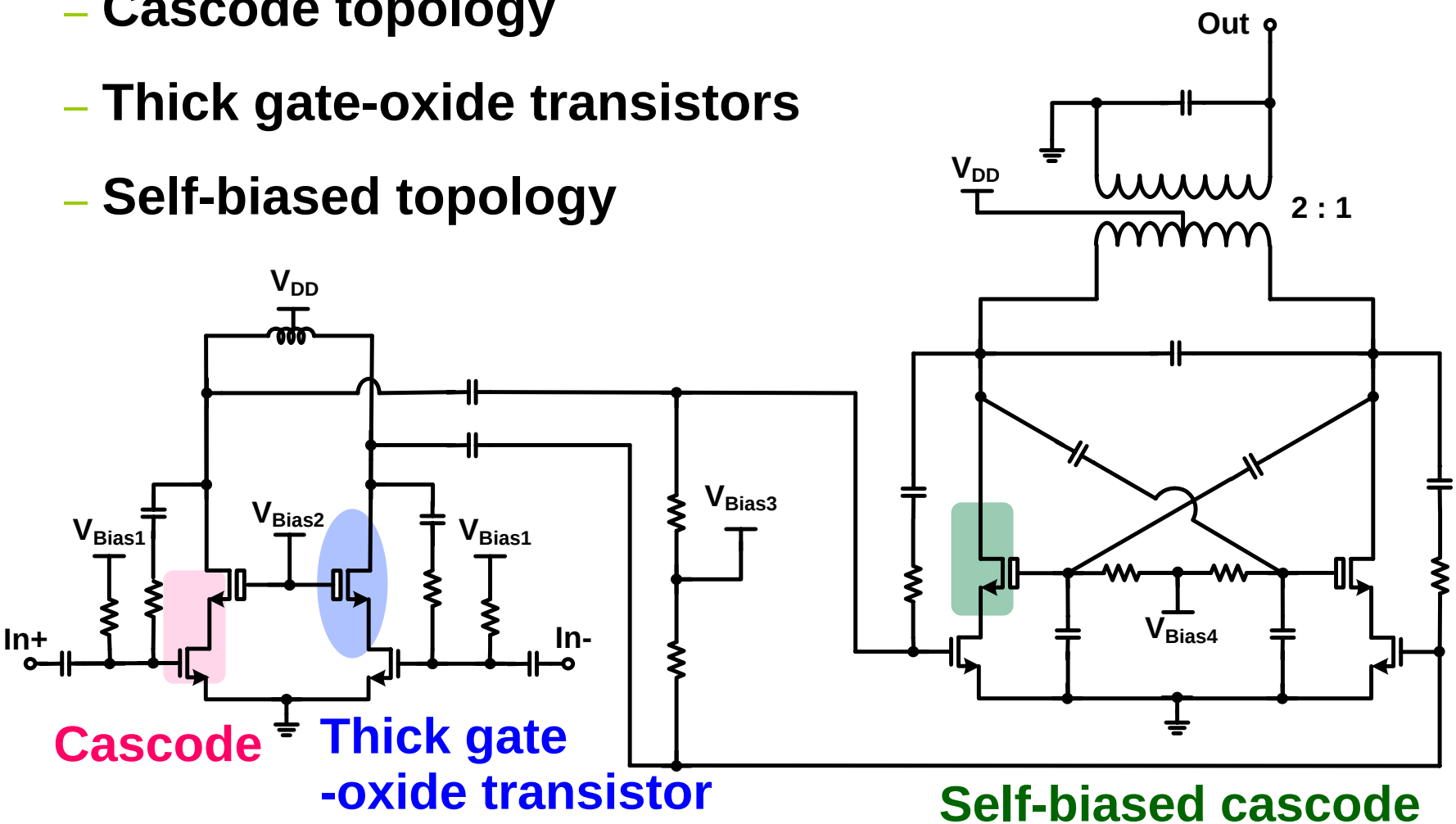
- To sustain voltage stress
  - Cascode topology
  - Thick gate-oxide transistors
  - Self-biased topology



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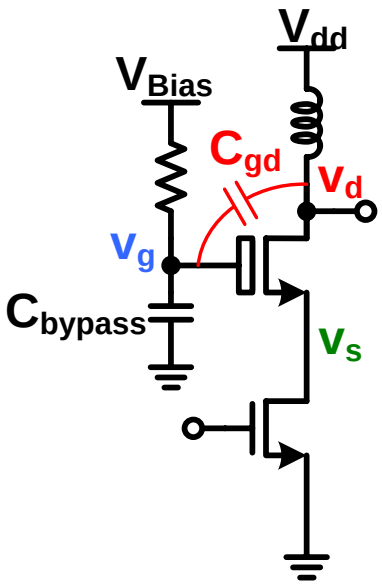
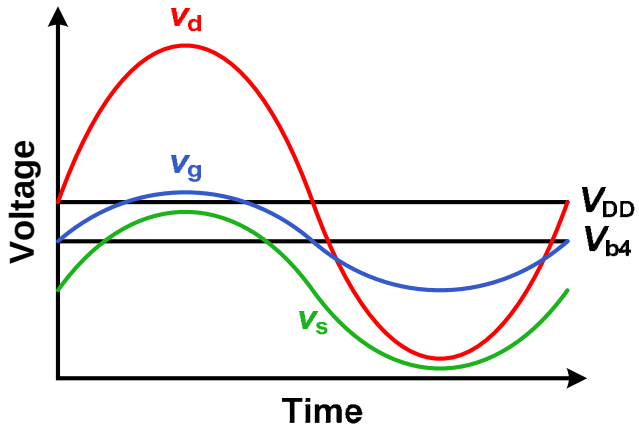
Self-biased cascode

- at the 2nd stage





[Conceptual diagram of voltage waveforms]

If C_{gs} is neglected,

$$v_g = \frac{C_{gd}}{C_{bypass} + C_{gd}} v_d$$

☺ Alleviation of voltage v_{gd}

☺ Prevention of transistor's entering to triode region

☹ Loss of Gain

☹ Area increase by C_{bypass}

[1] T. Sowlati, et al., "A 2.4-GHz 0.18-μm CMOS Self-Biased Cascode Power Amplifier," IEEE Journal of Solid-State Circuits, pp. 1318-1324, 2003

Amplitude adjustment

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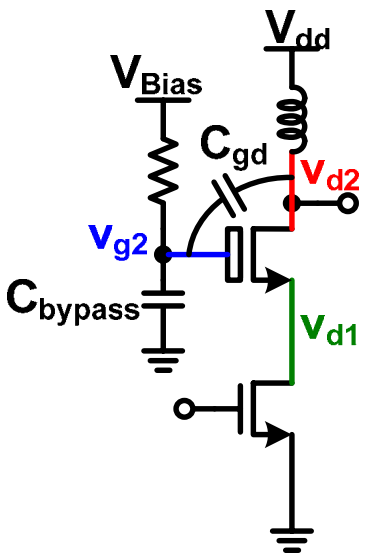
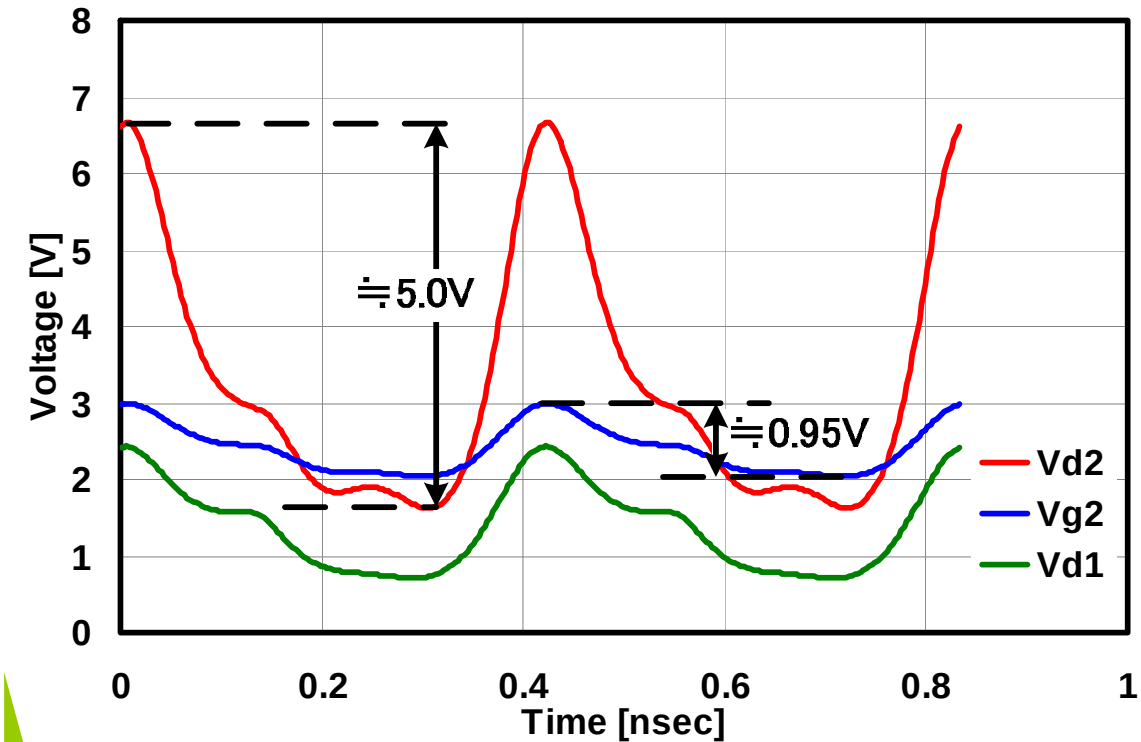


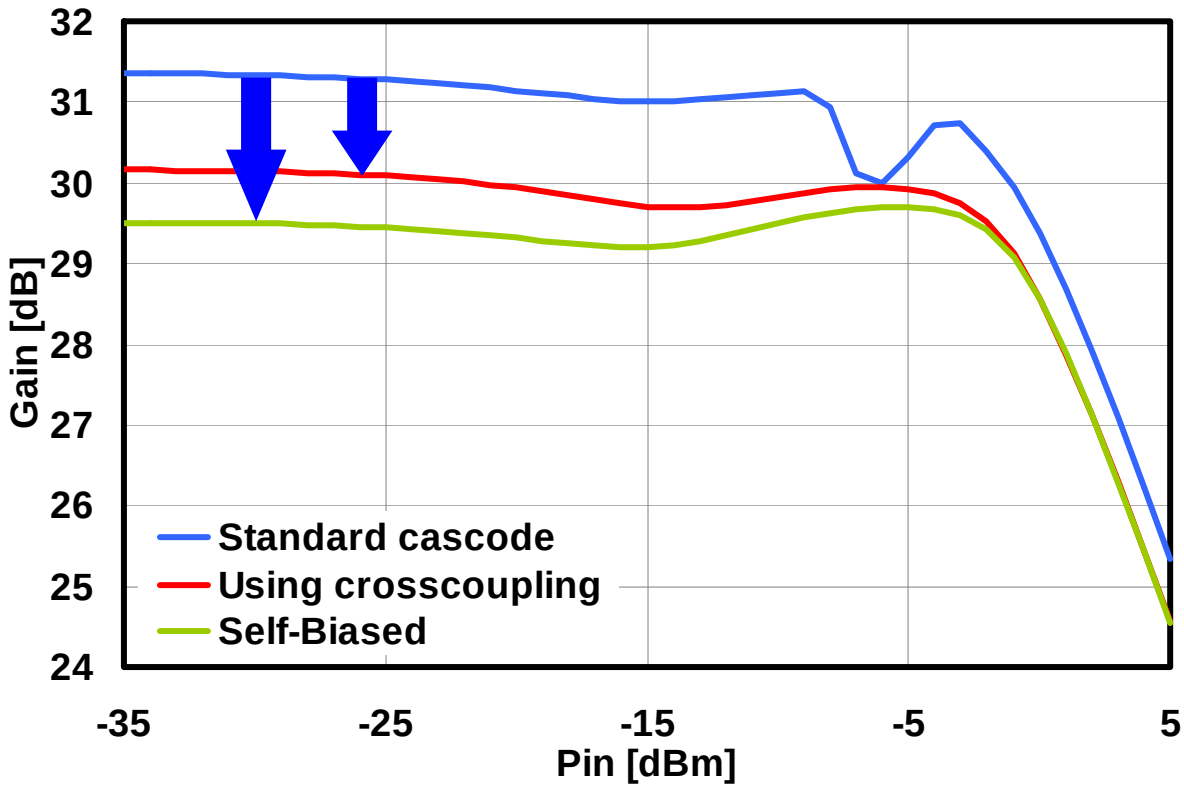
[Self-biased cascode]

- **Voltage waveform**



- V_g amplitude=19% of the V_d amplitude
- C_{bypass}=14.5pF

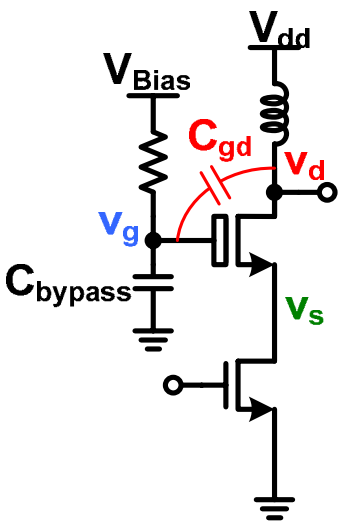
Gain degradation



- **Self-biased cascode method degrades the gain compare with standard cascode method using fixed bias voltage.**

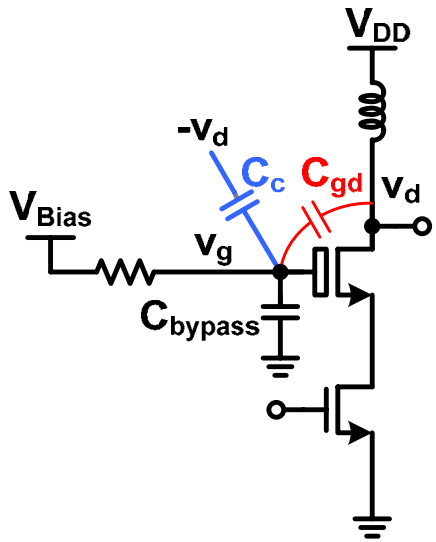
Capacitive cross-coupling

Self-biased cascode



$$v_g = \frac{C_{gd}}{C_{bypass} + C_{gd}} v_d$$

Using capacitive cross-coupling



$$v_g = \frac{C_{gd} - C_c}{C_{bypass} + (C_{gd} - C_c)} v_d$$

- C_c is tuned to v_g amplitude 18% of v_d amplitude
- C_{gd} is reduced, thus C_{bypass} is decreased

Amplitude adjustment 2

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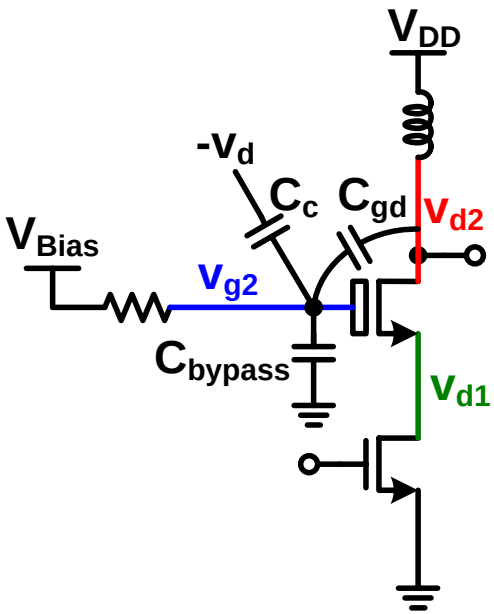
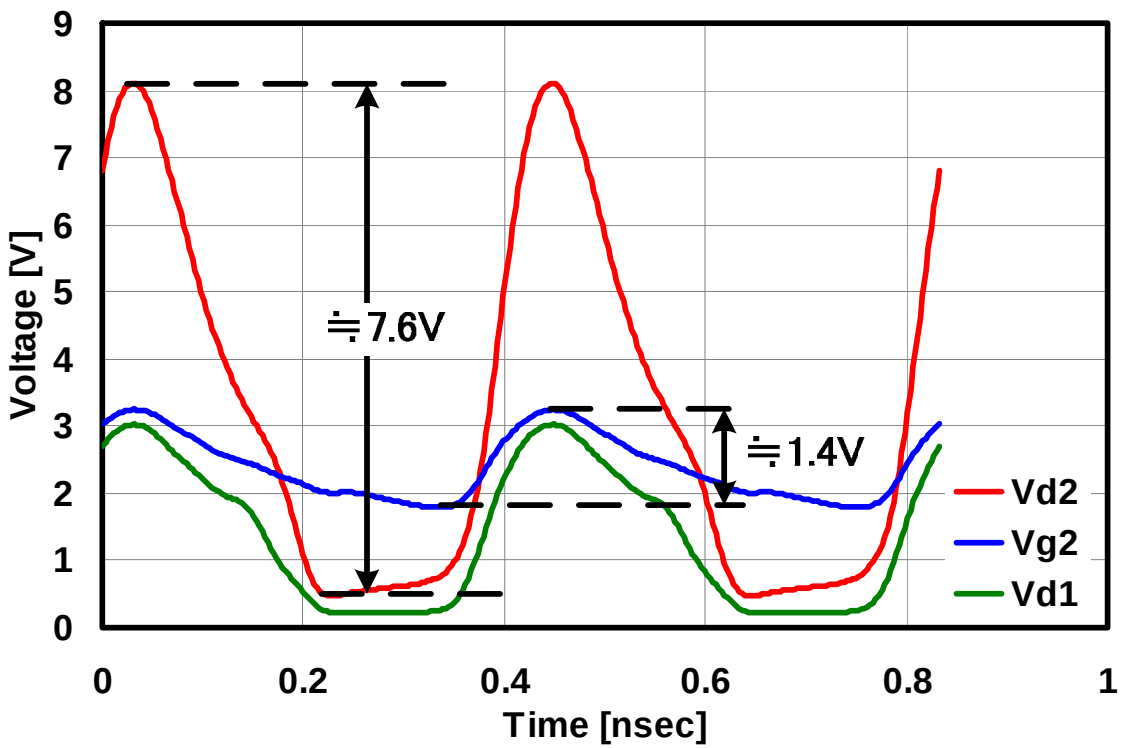


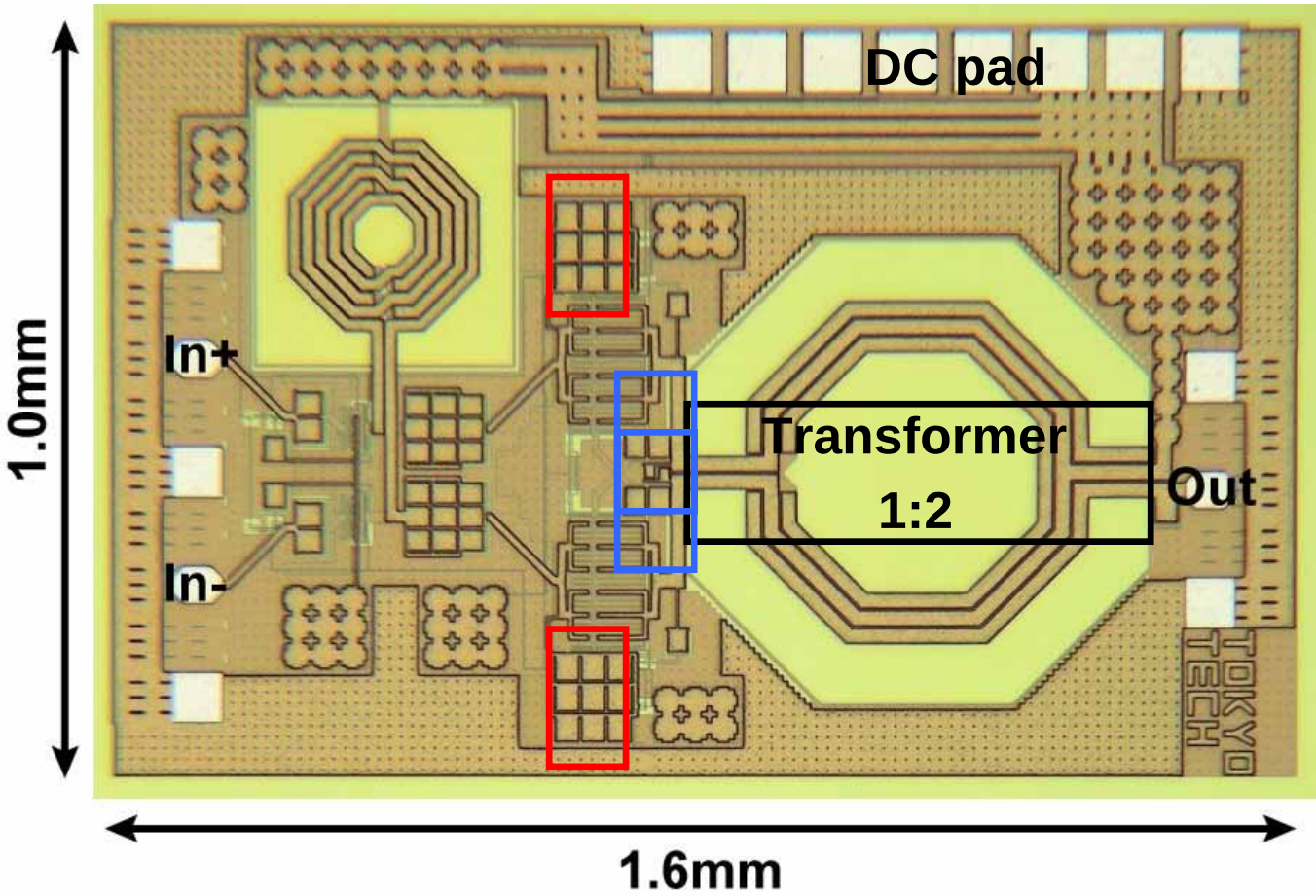
[Self-biased cascode with capacitive cross-coupling]

- **Pin=5dBm**



- V_g amplitude=18% of the V_d amplitude
- C_{bypass}=8.6pF

Chip micrograph

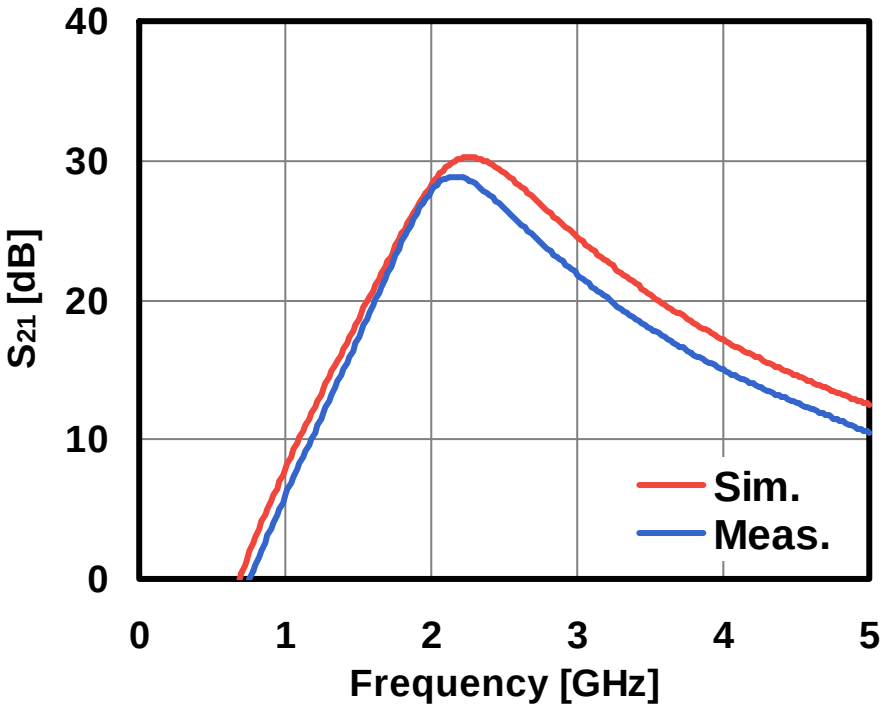


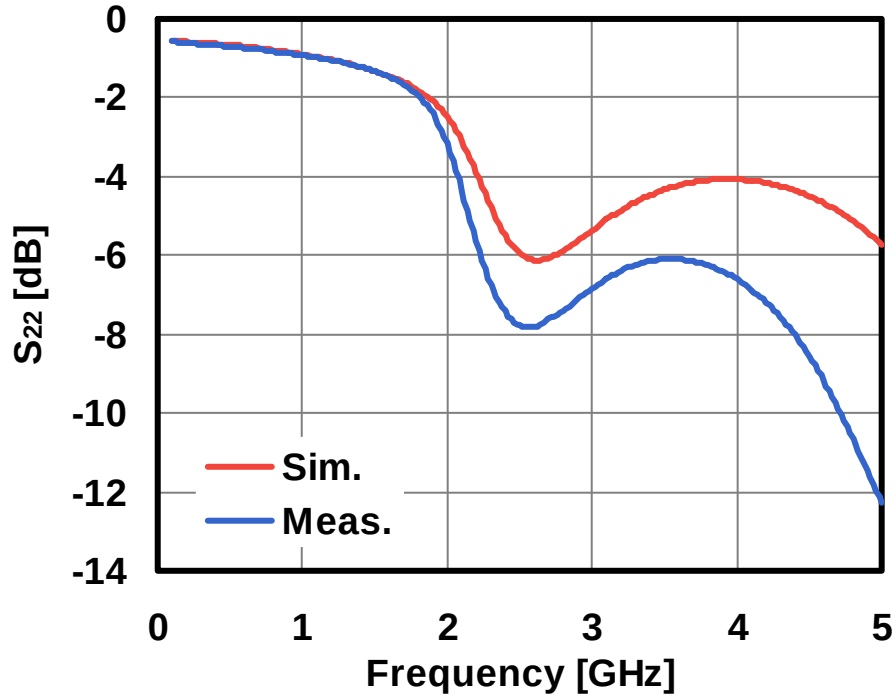
Using
MIM capacitor
(1fF/μm^2)

Bypass capacitor C_{bypass} = 14.5pF→8.6pF

Cross-coupling capacitor C_{cc} = 1.5pF

S-parameter measurement results

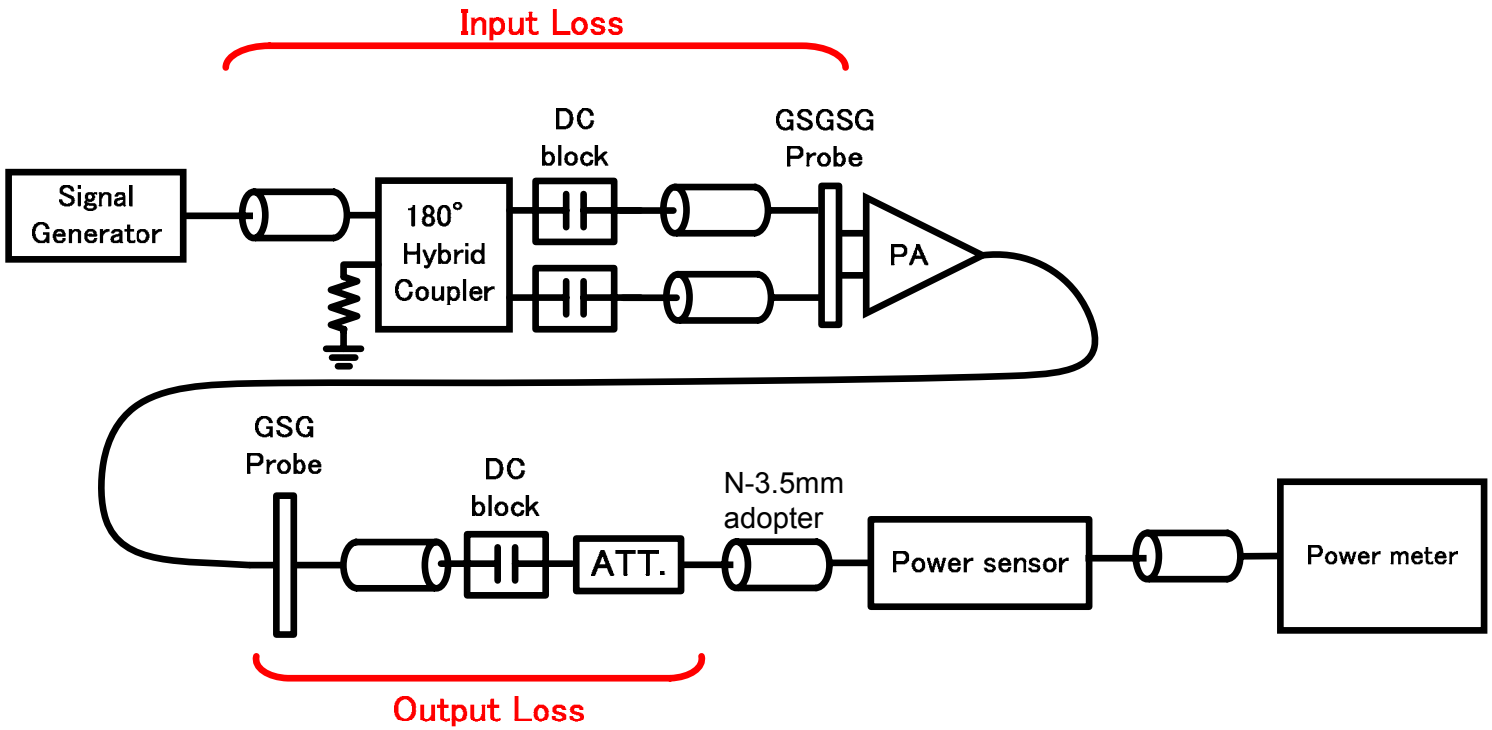




- **Measurement results are roughly in accordance with simulation results**

Measuring system

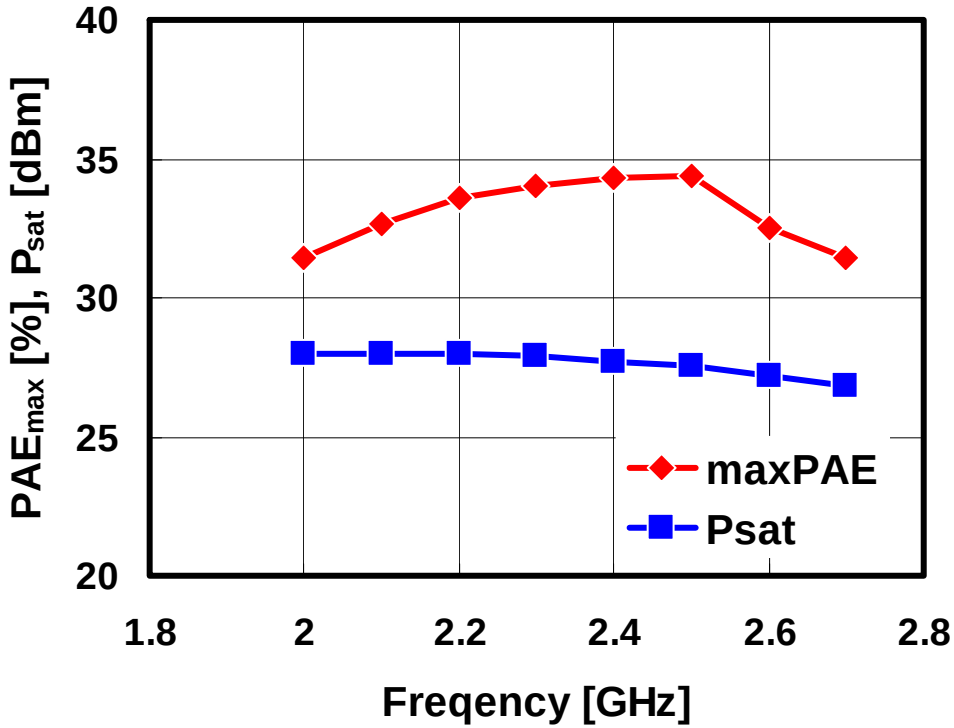
- **Large signal measurement setup**



- **Input and output losses are measured separately, and are calibrated from results.**

Large signal measurement result

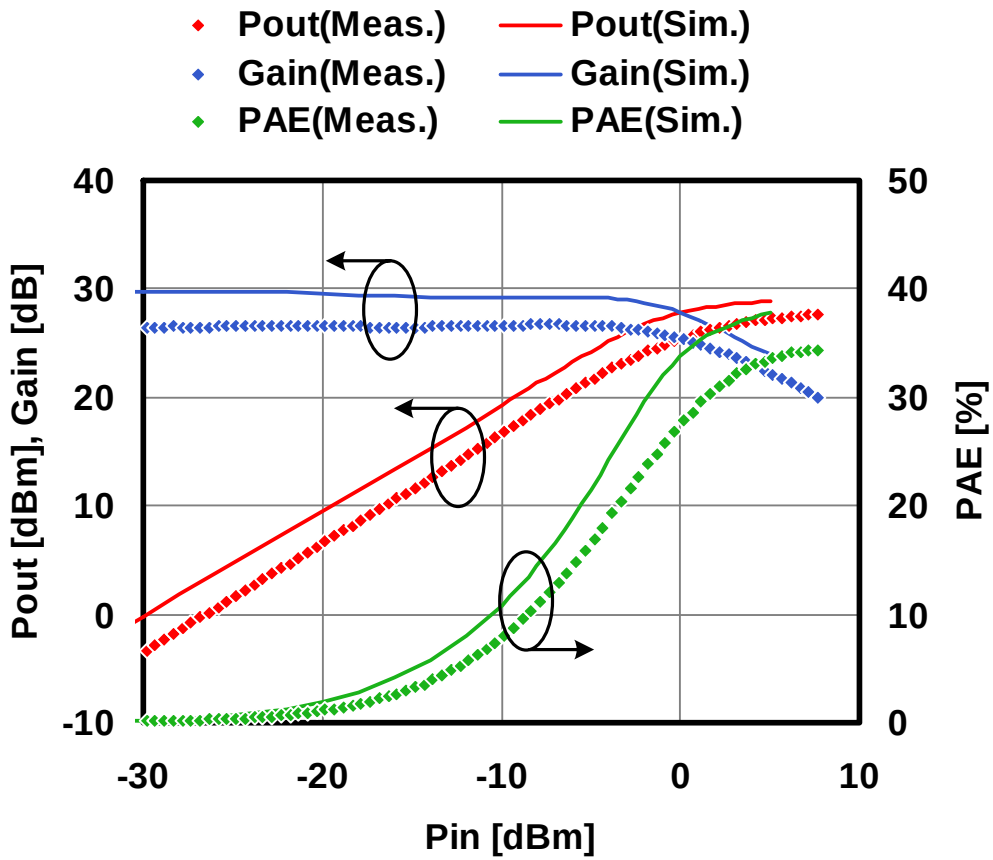
- **Near 2.4 GHz**



- $PAE_{max} > 31$ %
- $P_{sat} > 27$ dBm

Large signal measurement result

2.4 GHz



- P_{1dB} = 25 dBm
- P_{sat} = 27.7 dBm
- Gain = 26.5 dB
- PAE_{1dB} = 26.8 %
- PAE_{max} = 34.3 %

Comparison of CMOS PAs

	[2]	[3]	[4]	[5]	This work
Technology	90nm	130nm	180nm CMOS		
V_{DD}	3.3 V	1.2 V	3.3 V	3.3 V	3.3 V
Frequency	2.4 GHz				
P_{1dB}	27.7 dBm	24 dBm	24.5 dBm	27 dBm	25.2 dBm
P_{sat}	30.1 dBm	27 dBm	-	31 dBm	27.7 dBm
PAE_{peak}	33 %	*32 %	31 %@1dB	27 %	**34.3 %**
Area	4.3 mm^2	1.7 mm^2	1.7 mm^2	2.0 mm^2	**1.6 mm^2**

* Drain efficiency

[2] D. Chowdhury, et al., “A Single-Chip Highly Linear 2.4GHz 30dBm Power Amplifier in 90nm CMOS,” IEEE International Solid-State Circuits Conference, pp. 378-380, 2008

[3] G. Liu, et al., “Fully Integrated CMOS Power Amplifier With Efficiency Enhancement at Power Back-Off,” IEEE Journal Of Solid-State Circuits, vol. 43, No. 3, pp. 600-609, Mar. 2008

[4] J. Kang, et al., “A Single-Chip Linear CMOS Power Amplifier for 2.4GHz WLAN,” IEEE International Solid-State Circuits Conference, pp.761-769, 2006

[5] K. An, et al., “A 2.4 GHz Fully Integrated Linear CMOS Power Amplifier With Discrete Power Control,” IEEE Microwave and Wireless Components Letter, vol. 19, No. 7, pp. 479-481, July. 2009

Conclusion

- Designing 2.4GHz PA with high output power
- Circuit design
  - Using TSMC 0.18μm CMOS process
  - High output power：Differential topology, 2-stage configuration, Transformer
  - Improvement of withstanding voltage：Cascode, Thick gate-oxide transistor, Self-biased cascode
  - Reduce of area for C_{bypass}：Capacitive cross-coupling
- Results
  - P_{1dB} = 25.2dBm, P_{sat} = 27.7dBm, PAE_{peak} = 34.3%
  - Needed C_{bypass} = 14.5pF→8.6pF(41%↓)