

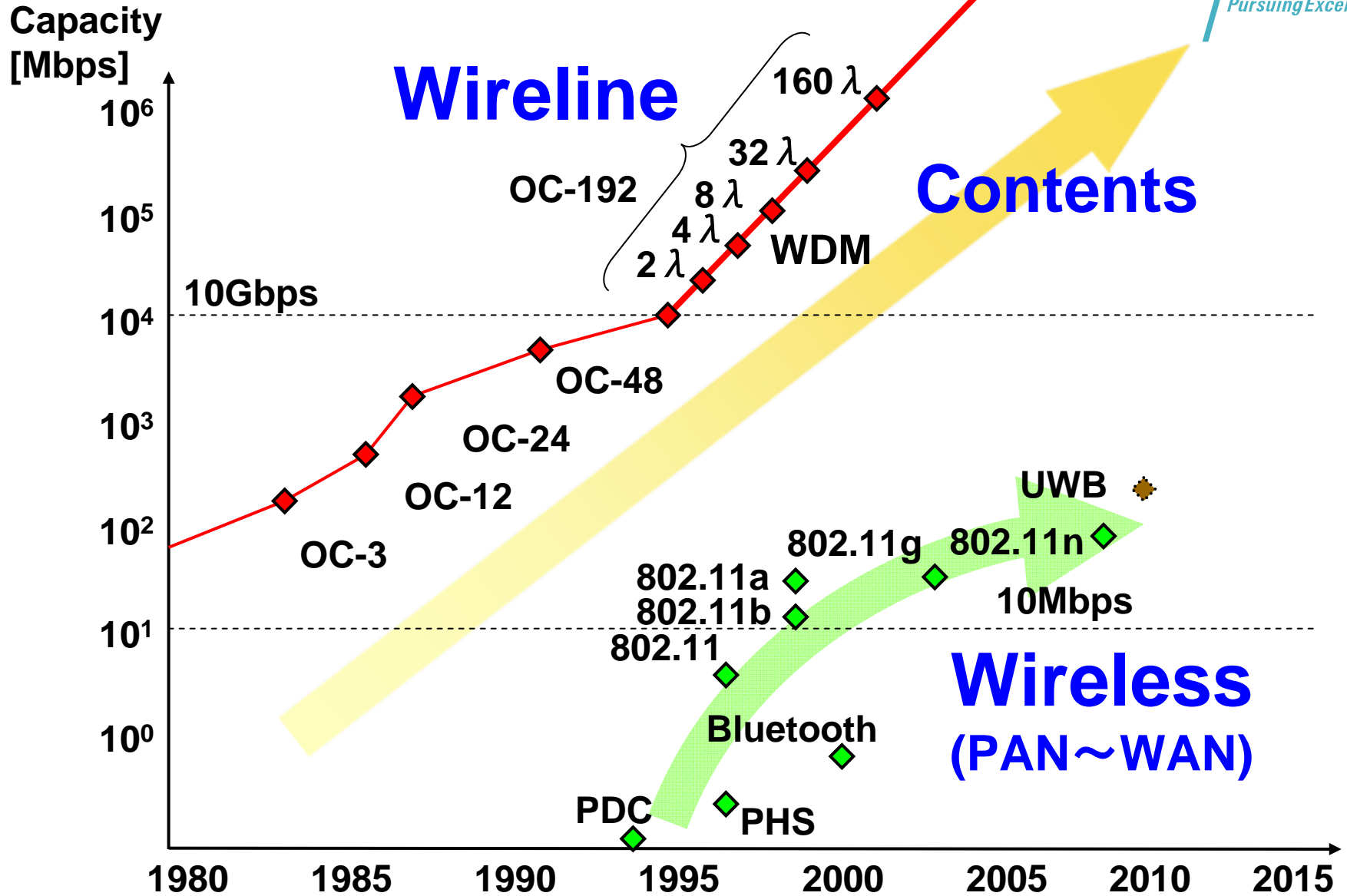
Test Structures for Millimeter-Wave CMOS Circuit Design

Kenichi Okada

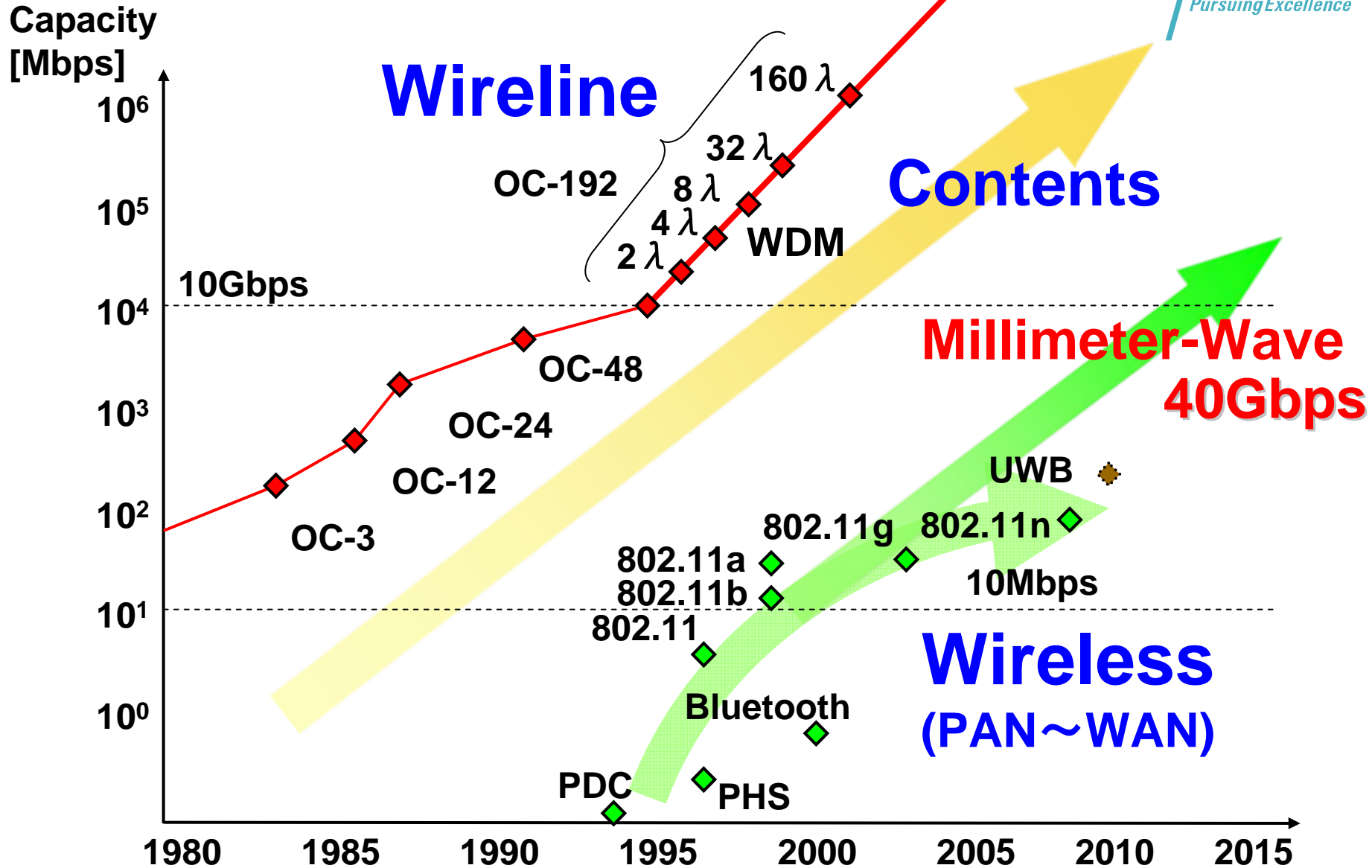
Tokyo Institute of Technology, Japan

- ➔ • **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
- **De-embedding**
- **Conclusion**

Motivation



Motivation



24GHz: Automotive radar

60GHz: IEEE 802.15.3c, WirelessHD, etc.

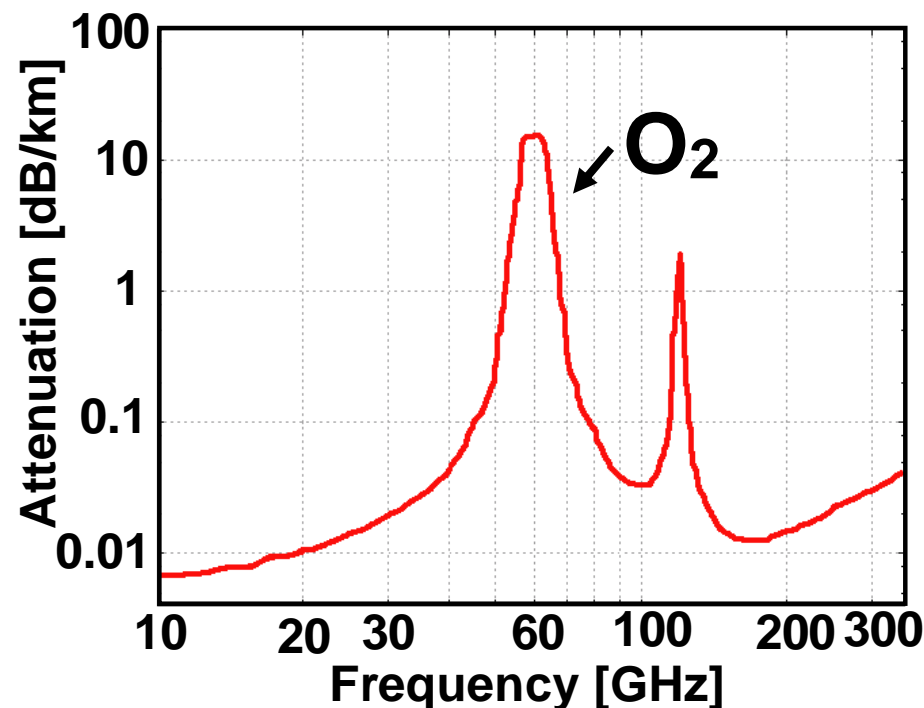
77-79GHz: Automotive radar

94GHz: Imaging

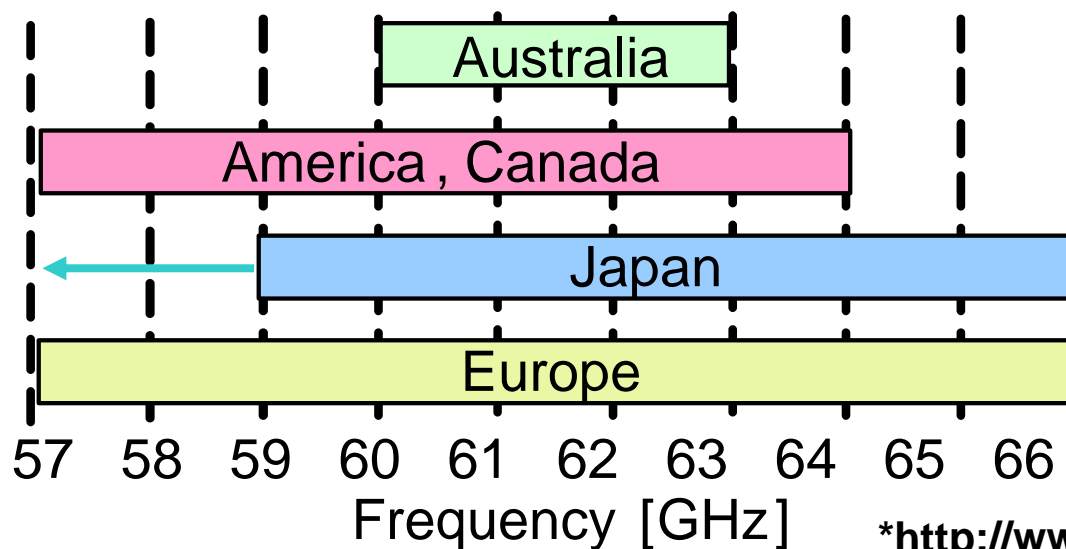
Ultra high speed

Wireless communication

By CMOS



60GHz unlicensed band



*<http://www.tele.soumu.go.jp>

- **9GHz-BW around 60GHz**
 - ➡ **Several-Gbps wireless communication**
- **Use of CMOS process**
 - ➡ **Fab. cost is very important to generalize it.**
 - RF&BB mixed chip can be realized.**

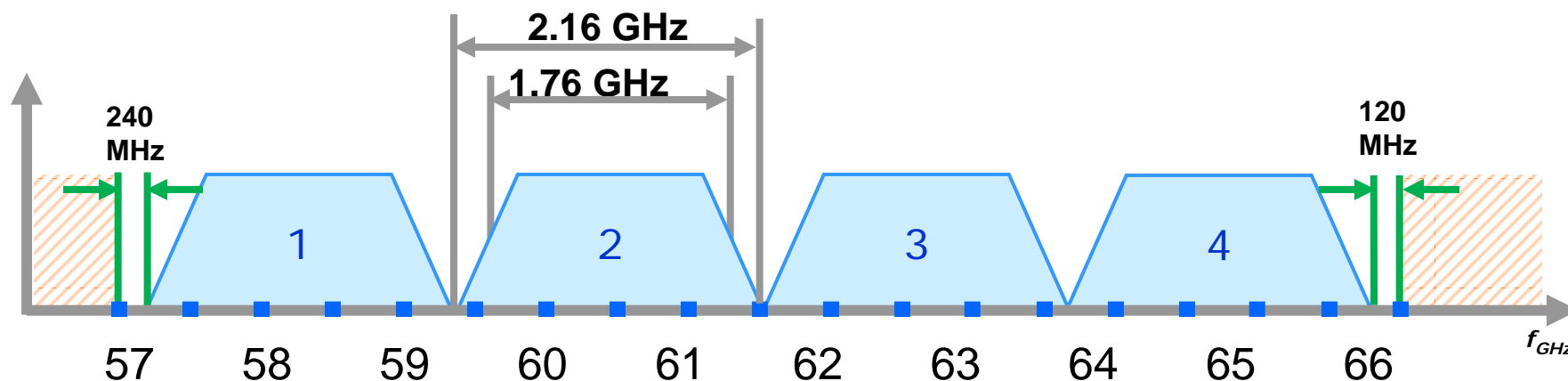
60GHz channel plan

6

IEEE802.15.3c

Ref: IEEE 802.15-09-192-003c with draft doc.

Channel Number	Low Freq. (GHz)	Center Freq. (GHz)	High Freq. (GHz)	Nyquist BW (GHz)	Roll-Off Factor
A1	57.24	58.32	59.40	1.76	0.227
A2	59.40	60.48	61.56	1.76	0.227
A3	61.56	62.64	63.72	1.76	0.227
A4	63.72	64.80	65.88	1.76	0.227



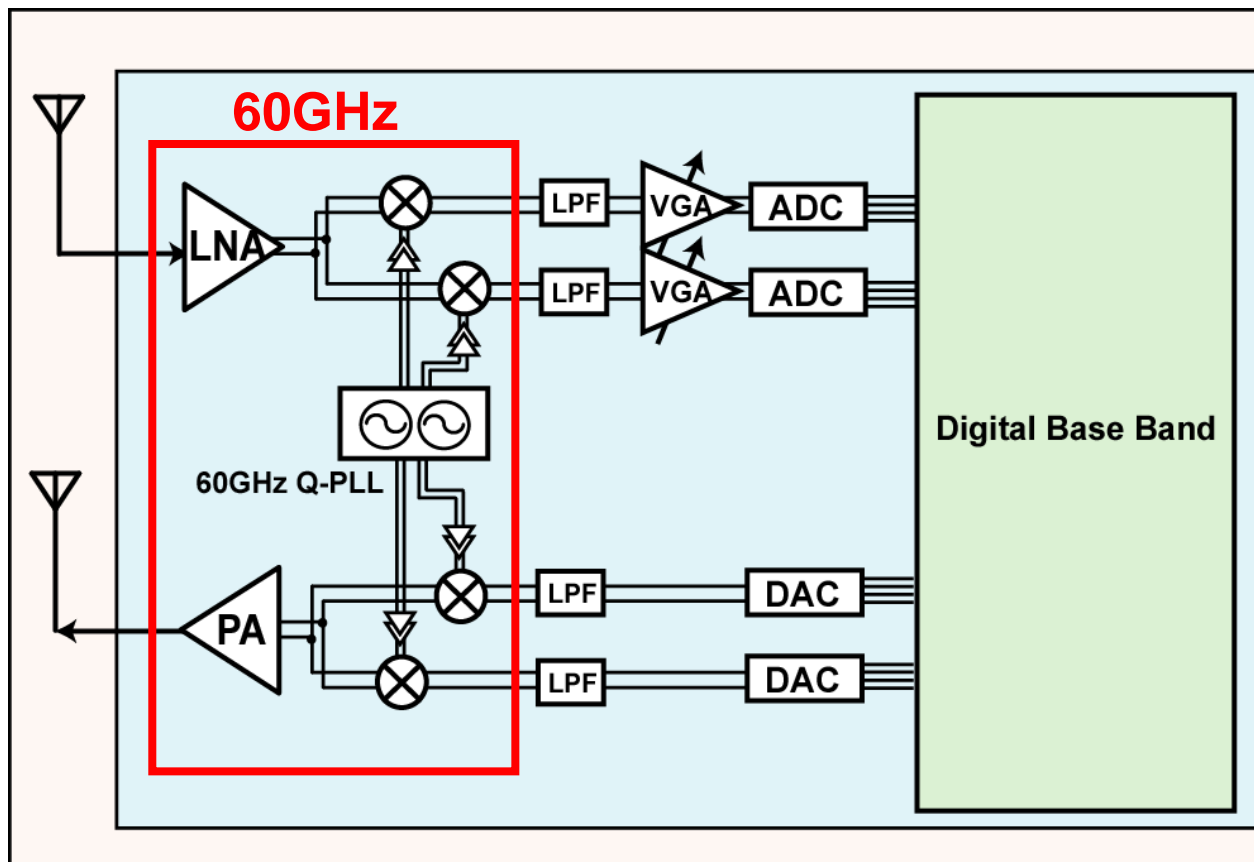
4 channel of 2.16GHz-BW

- One unified MAC
- Three PHYs optimized for respective and specific market segments
 - **Single carrier (SC) PHY**
 - low complexity, low power consumption and low cost
 - handheld mobile applications
 - **High speed interface (HSI) PHY - OFDM**
 - low latency bi-directional data communications
 - PC peripherals
 - **AV PHY - OFDM**
 - optimized for high speed uncompressed video transmission
 - Audio/visual consumer electronics (CE) applications

Ref: IEEE 802.15-09-192-003c

**e.g., 3Gbps(QPSK), 6Gbps(16QAM), 9Gbps(64QAM)
x4ch**

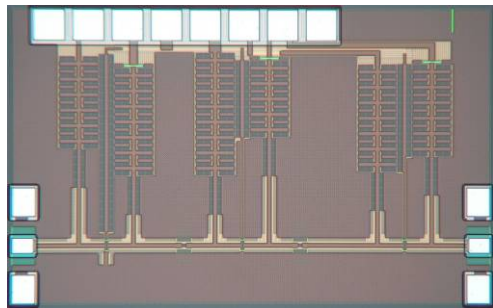
- Motivation
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- Conclusion



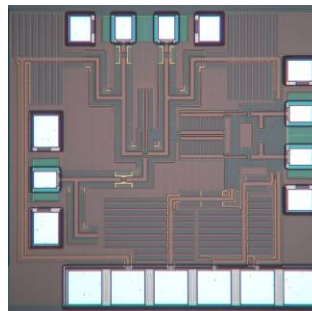
60GHz 2.16GHz-full 4ch direct-conversion by CMOS Tr
QPSK 3Gbps & 16QAM 6Gbps & 64QAM 9Gbps

IEEE 802.15.3c conformance

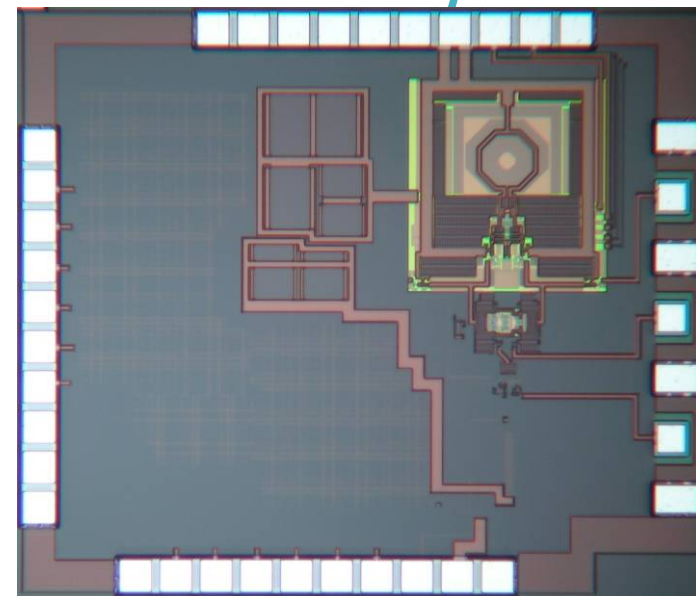
Dynamic power management: <300mW for RF front-end



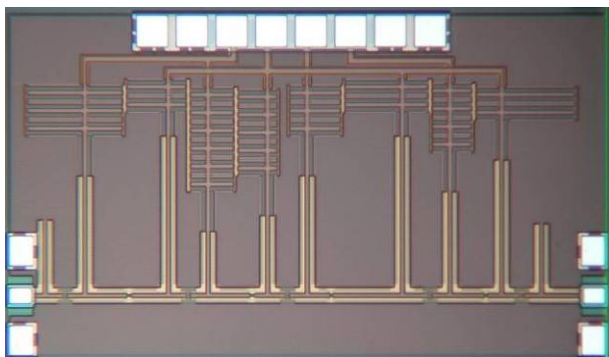
60GHz LNA



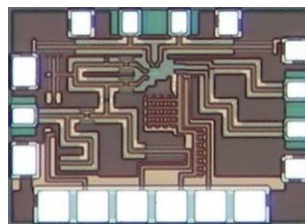
Down-Mixer



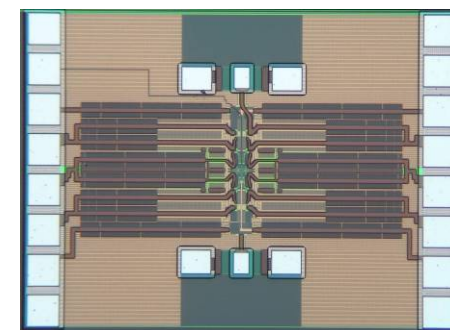
20GHz PLL



60GHz PA



Up-Mixer



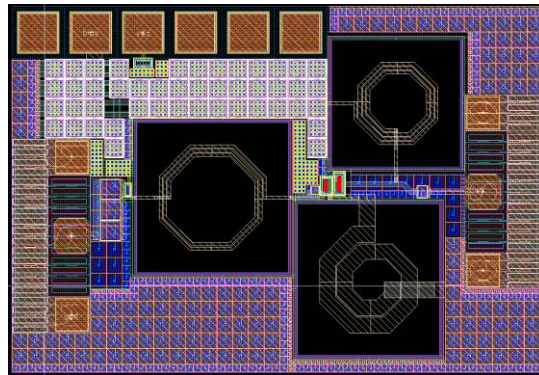
I/Q Tripler

FUJITSU(Eshuttle) CMOS 65nm

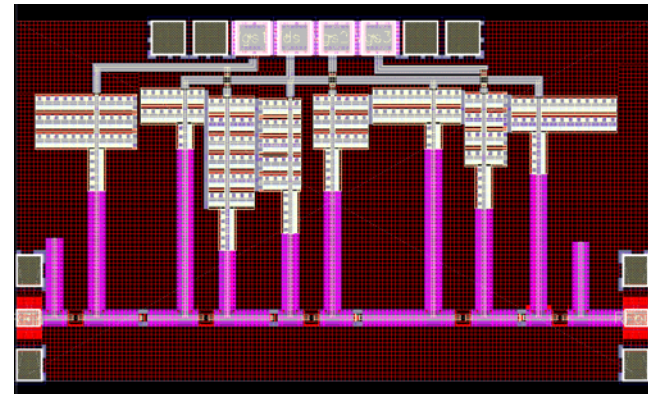
Layout parasitics become critical for mmW circuit design.

1. Interconnects between circuit components become close to the wave length.
2. Dummy metal for CMP
3. Tr gain is very small, and TL is lossy.

Matching blocks



Inductor @5GHz

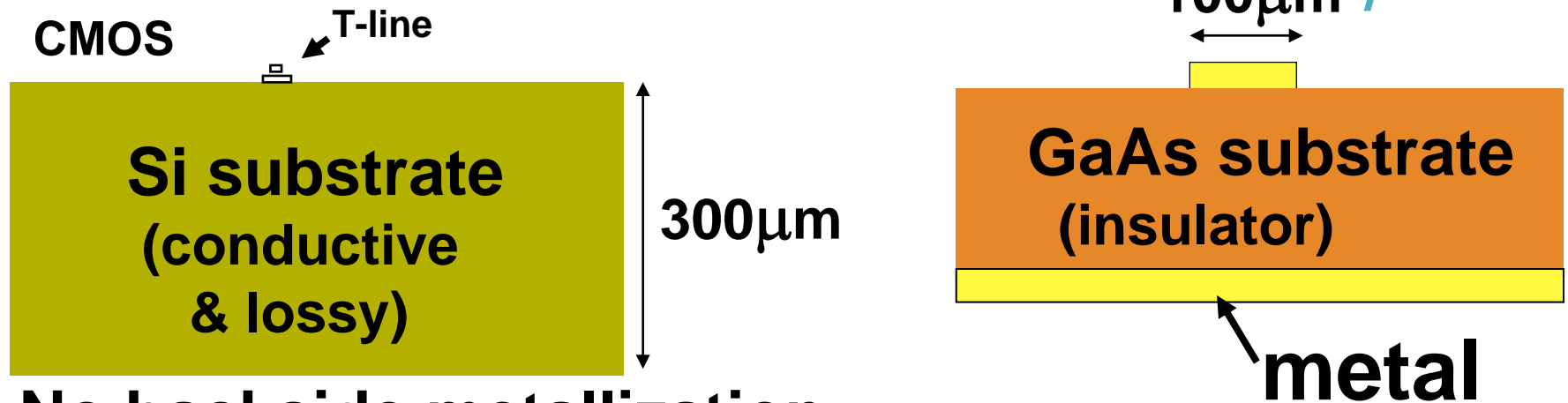


Transmission line @60GHz

At 60GHz, every interconnects should be dealt with as a distributed component.

➡ **The accurate characterization is required.**

Loss of passive devices

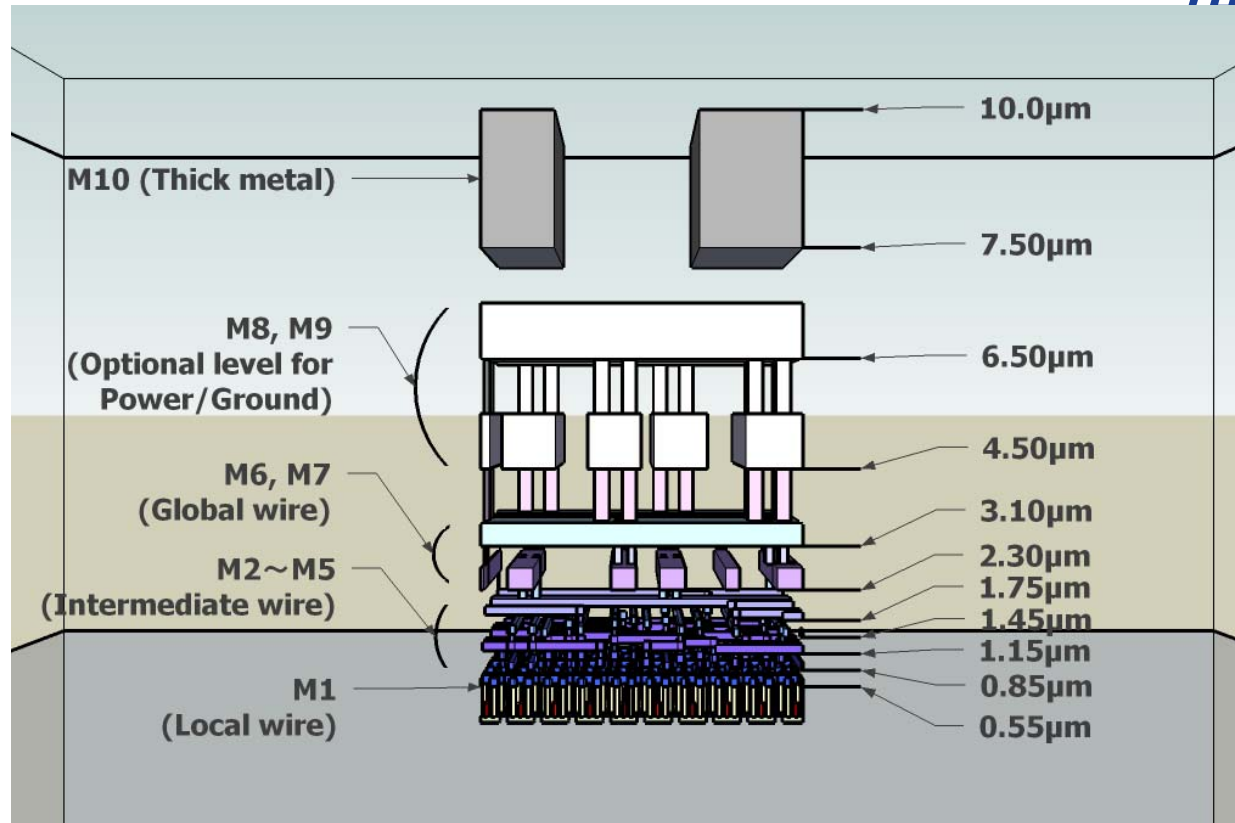


No backside metallization

Conductor loss + Substrate eddy-current loss

50Ω T-line loss: 0.5 – 1.5dB/mm @60GHz

	Si CMOS	GaAs
Wire width	10µm	100µm
Wire thickness	1 – 2µm	10µm
Dielectric thickness	< 5µm	100µm

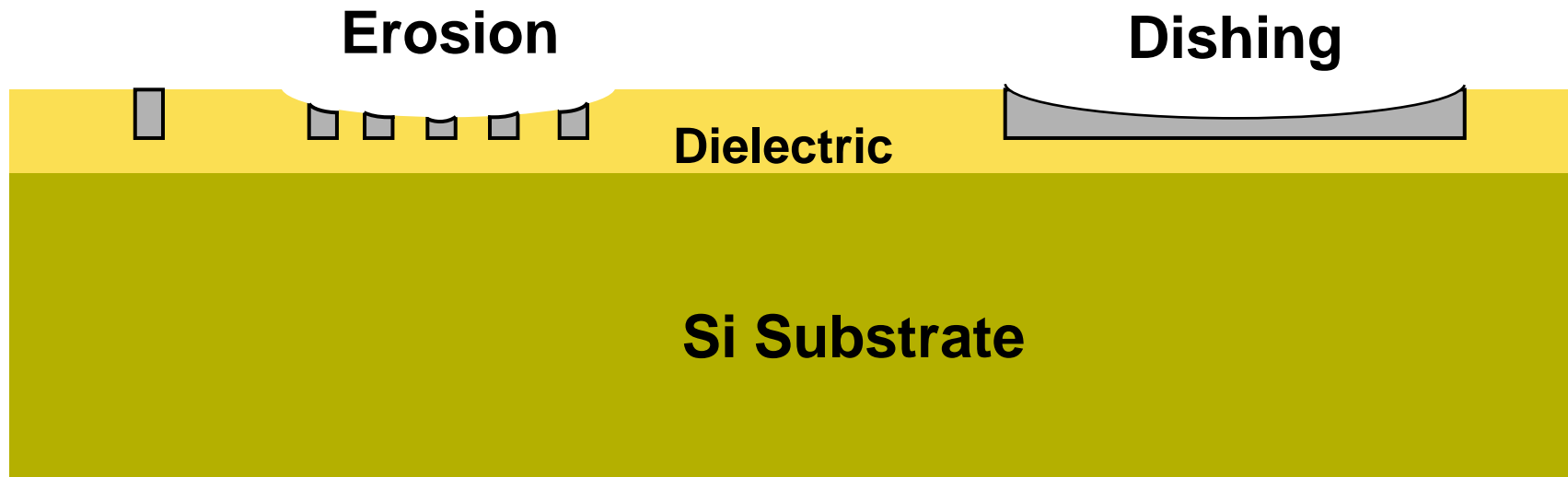


<http://www.tamaru.kuee.kyoto-u.ac.jp/~tsuchiya/LSI-3D-CG.html>

- Every tiers have a different cross-sectional structure with different dielectric constant.
- EM simulation becomes considerably difficult.
- Cu wire needs high-resistance barrier metal.

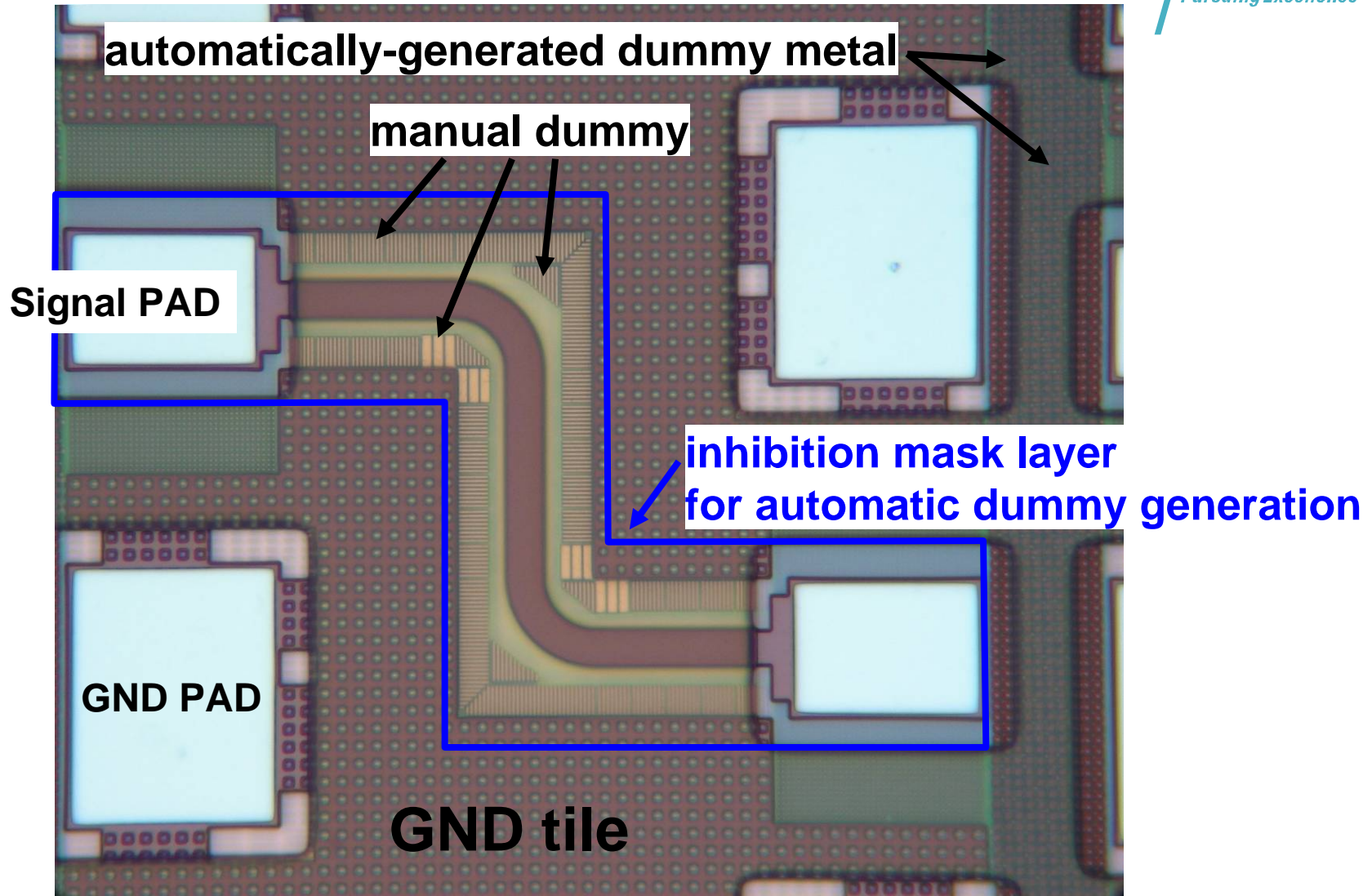
Density rule for CMP

CMP (Chemical Mechanical Polishing/Planarization)
every metal layers are polished.



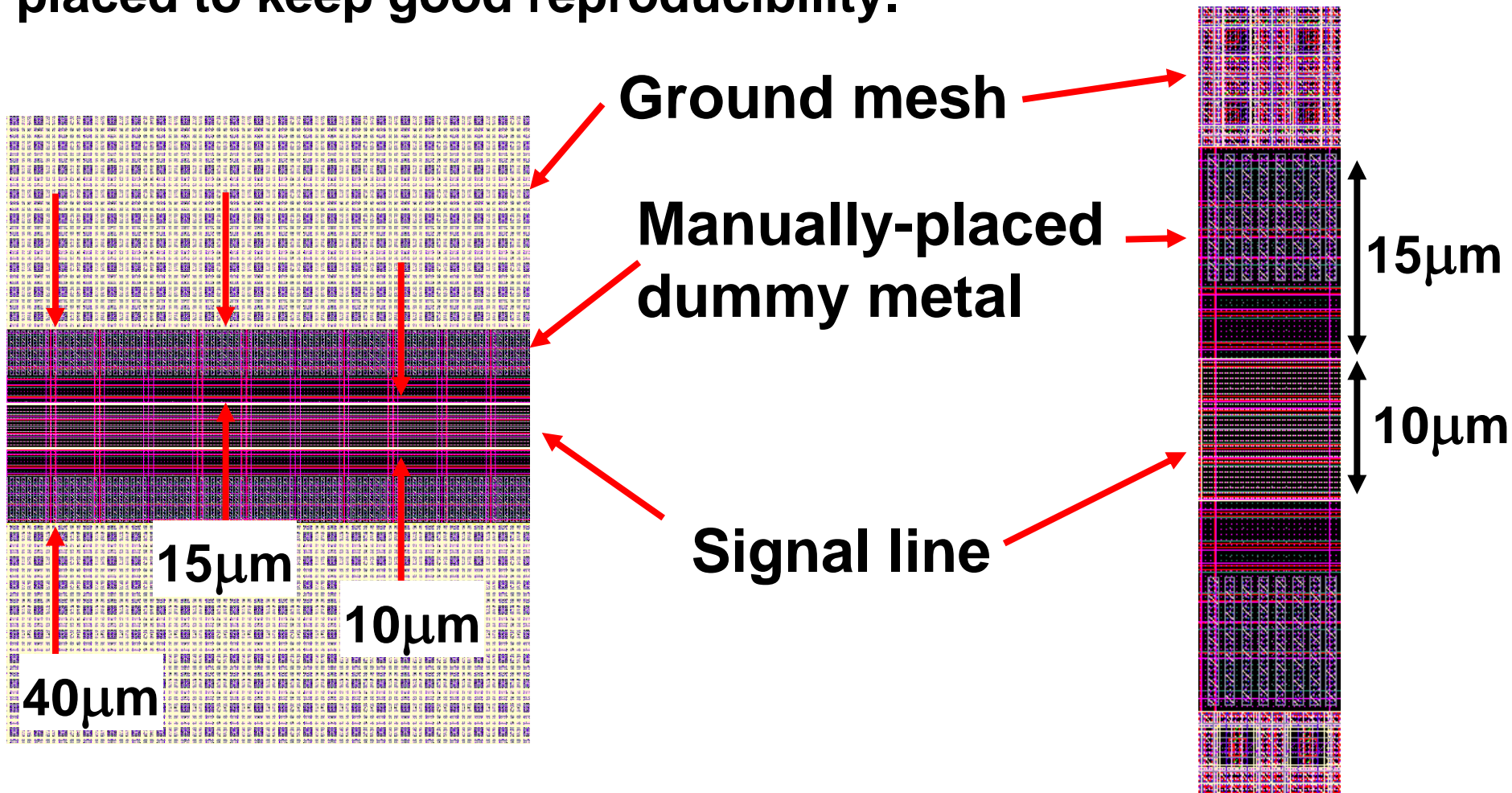
- **Uneven metal density causes nonuniform metal thickness.**
- **Dummy metals are required to keep a constant metal thickness.**

Dummy metal

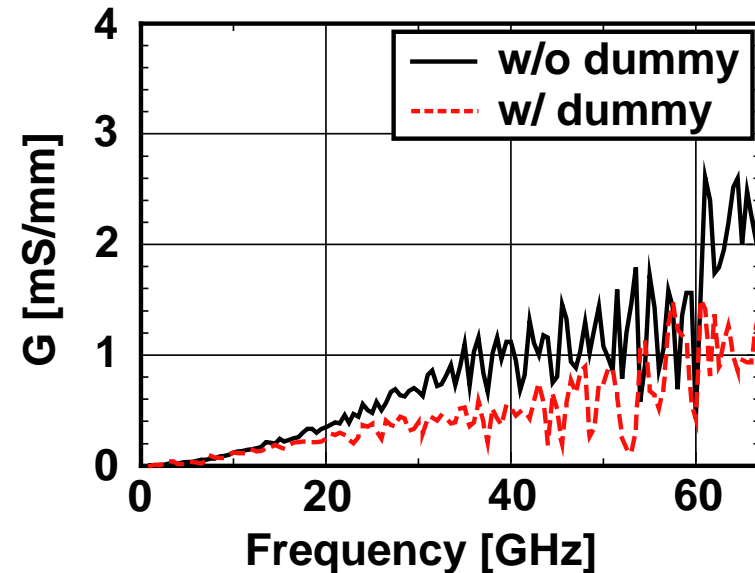
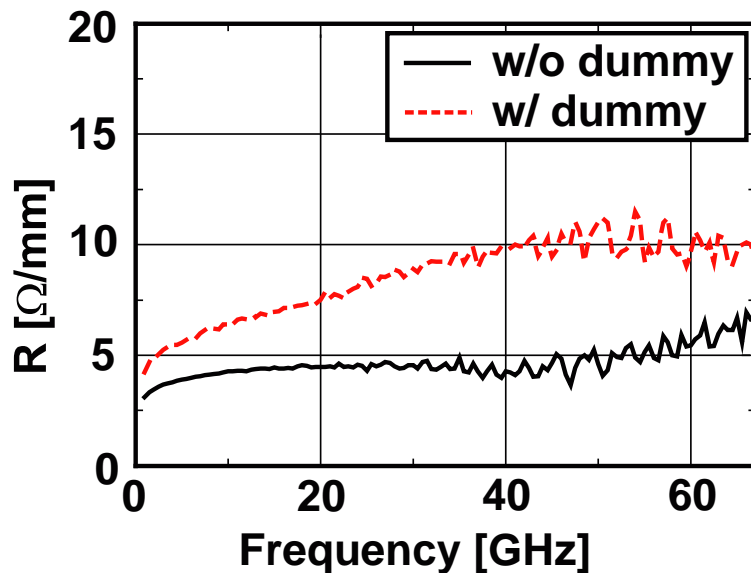
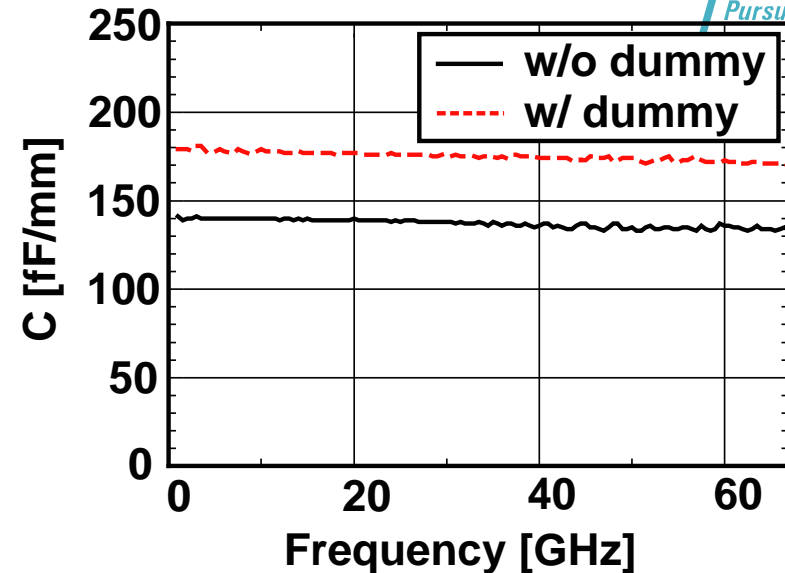
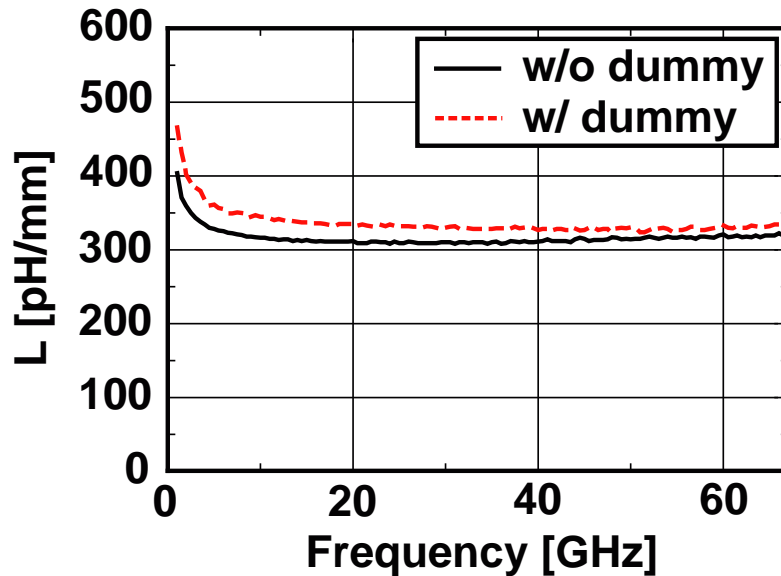


Dummy metal in TL

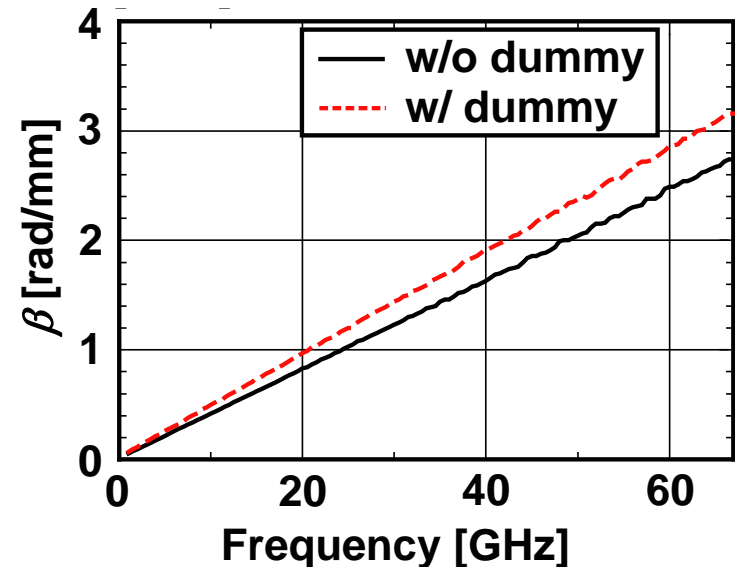
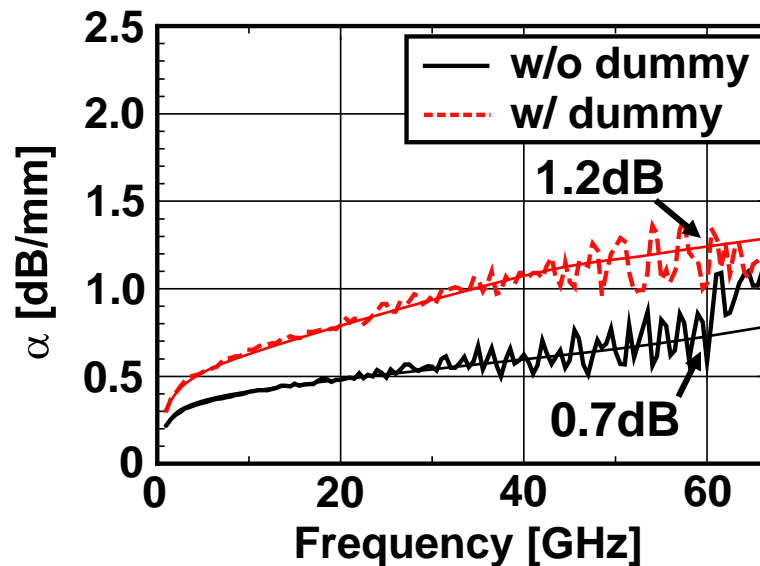
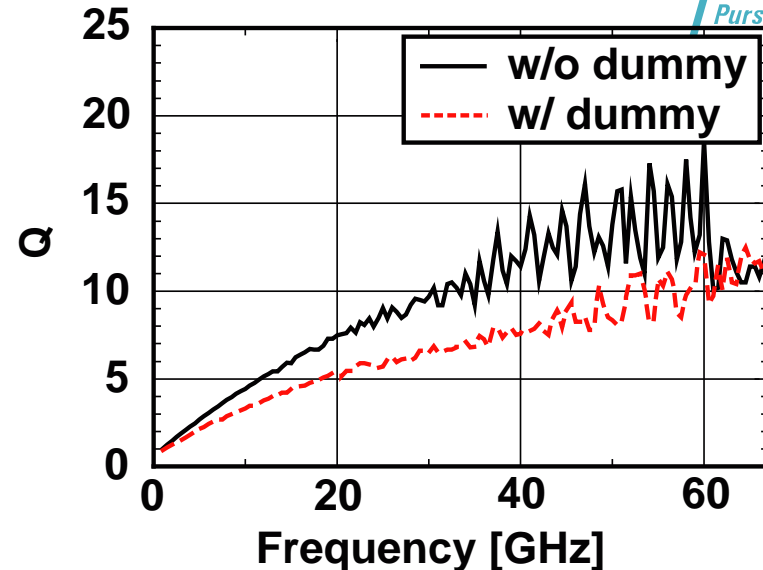
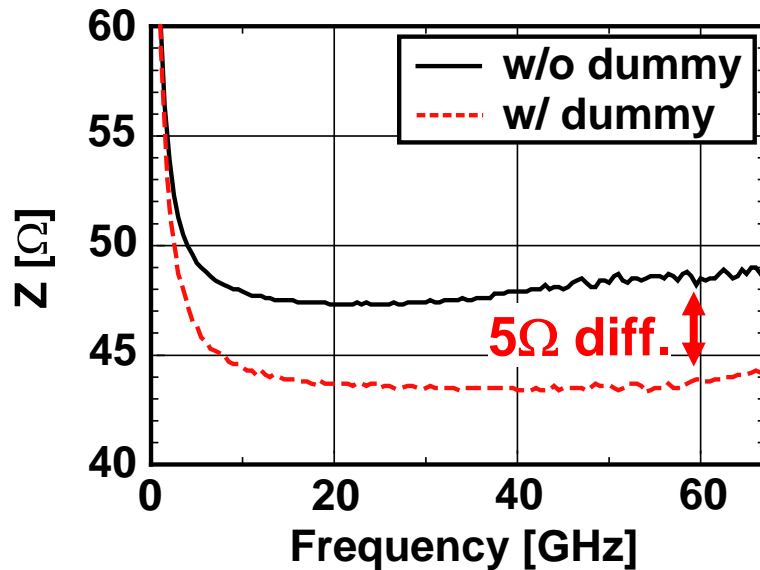
To avoid random production of dummy metal, it is manually placed to keep good reproducibility.



Dummy influence on T-line



Dummy influence on T-line



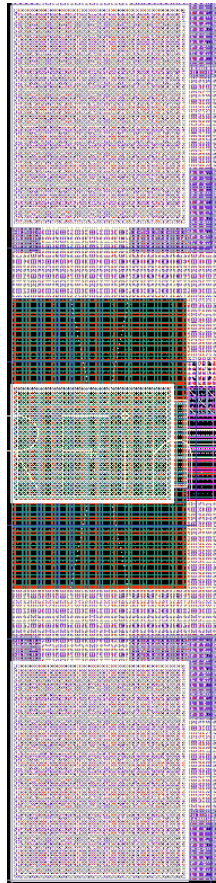
Dummy metals are required for CMP.

- **Loss** (mainly caused by eddy current)
 - Too-close dummy causes loss in T-lines.
- **Parasitic capacitance**
- **Layout complexity**
 - The common MS model cannot be used.
 - EM simulation is also difficult.

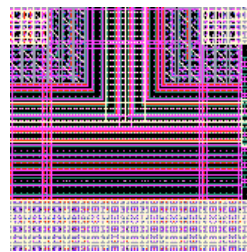
Tile-based layout

Each component is previously measured and modeled.
The same layout is utilized to maintain modeling accuracy.

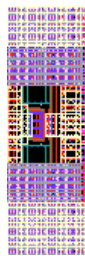
Bond-based design: Y. Manzawa, *et al.*, APMC 2008
5 μ m pitch



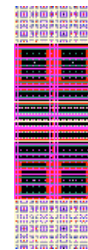
RF PAD



T-Junction



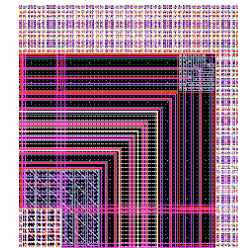
Tr



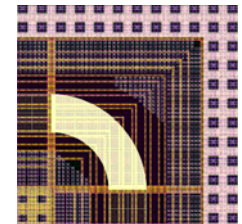
TL



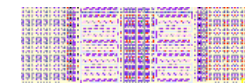
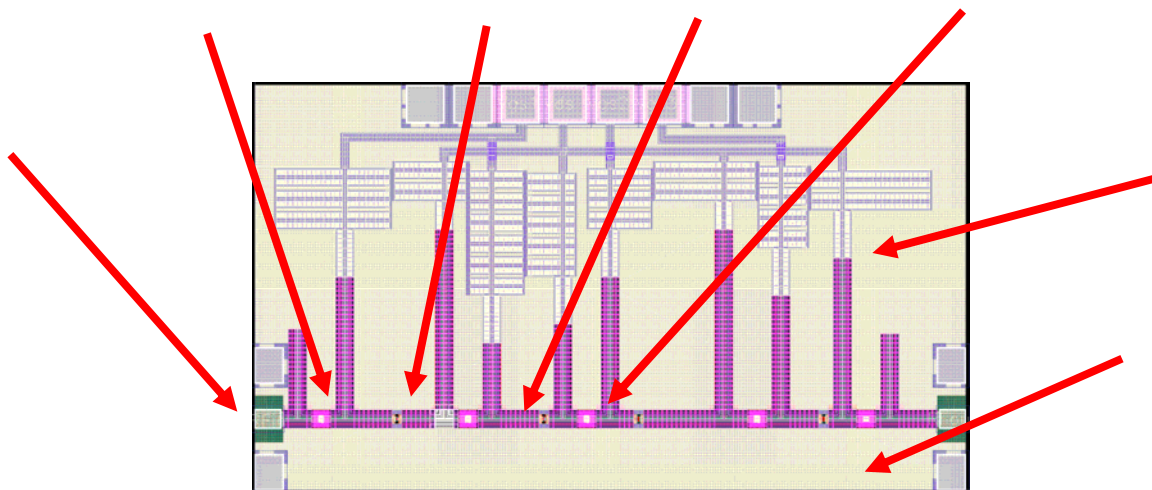
C



bend



curve



MIM TL



GND-Tile

See inside of top_pdk and top_meas.

top_pdk top_meas



To see simulation results, copy top_pdk.dds and top_meas.dds.

PDK

Nominal	Fast	Slow
1.0F/um ² MIM Cap	c. mim15rf	
1.0F/um ² MIM Cap	c. mimrf	
1.2v HS NFETs	nche,ncherf	
1.2v Std. NFETs	nch,nchrf	
1.2v HS PFETs	pche,pcherf	
1.2v Std. PFETs	pch,pchrf	
3.3v HS NFETs	fh3nes,fh3nerf (N/A)	
3.3v HS PFETs	fh3pes,fh3perf (N/A)	
Single-ended Inductors	ind_3p3,ind_0p9 stack (N/A)	
Diff Inductors	inddiff_3p3,inddiff_0p9_stack (N/A)	
1.2v Mosvar	vn_rf	
3.3v Mosvar	vnmh3rf	
VFNP	vpnp3_10 (N/A)	
Unsalicided resistors	rnsr,rnsr_pwr,rnsr_nw (520-555 Ohm/Sq)	
N-Salicided resistors	rnsr,rnsr_pwr,rnsr_nw (15 Ohm/Sq)	
P-Salicided resistors	rsp,rsp_pwr,rsp_nw (20 Ohm/Sq)	

PVT

Transistor (PDK)

nchrf,ncherf,pchrf,pcherf
w>=0.73um, L>=60 nm, nf>=4

Resistor (PDK)

Unsalicided resistors (rnsr,rnsr_pwr,rnsr_nw)
w>=0.5um, L>=2.0um
(520-550 Ohm/Sq) depending aspect ratio

N-Salicided resistors (rnsr,rnsr_pwr,rnsr_nw)
w>=0.5um, L>=3.0um
(15 Ohm/Sq)

P-Salicided resistors (rsp,rsp_pwr,rsp_nw)
w>=0.5um, L>=3.0um
(20 Ohm/Sq)

Varactor (PDK)

vn_rf
0.65um <= (wg,lg) <= 103um (Design Rule)
wg>=2um, lg>=0.1um, nf>=15 (Layout PDK)

vn_rf is recommended for VCO.

vnmh3rf, vpnh3rf
wg>=2um, lg>=0.35um, nf>=15 (Layout PDK)

MIM Capacitor (PDK)

c. mimrf
1.6um <= (W,L) <= 103um (Design Rule)
W<=6um, L>=17um (Layout PDK)

c. mim15rf cannot be used.

c. mim is only for DC.
no resistance, no shunt capacitance

Varactor

MOS cap

3.3V MOS decoupling (PDK nonDFM)
cponw33
Sum <= 1 <= 10um?, 10um <= w <= 20um? (PDK)
-3.6 < vd < 3.6
0 < vg < 3.6

cponw33 4.2F/um²
c. mimrf 1.0F/um²

cponw33 can be used up to 20GHz because of large parasitic resistance.

NMOS

PMOS

model C

Capacitor (model)

MIM TL (model)

Transmission Line (model)

RF PAD (model)

60um x 40um RF PAD

DC probe (meas.)

only reliable up to 20GHz

MIM TL

TL with L/T

DC probe

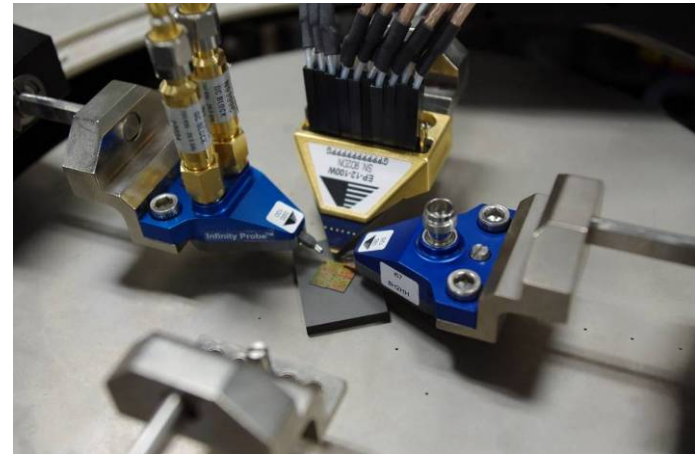
RF PAD

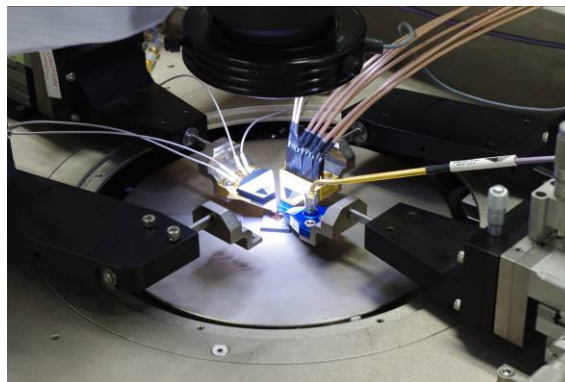
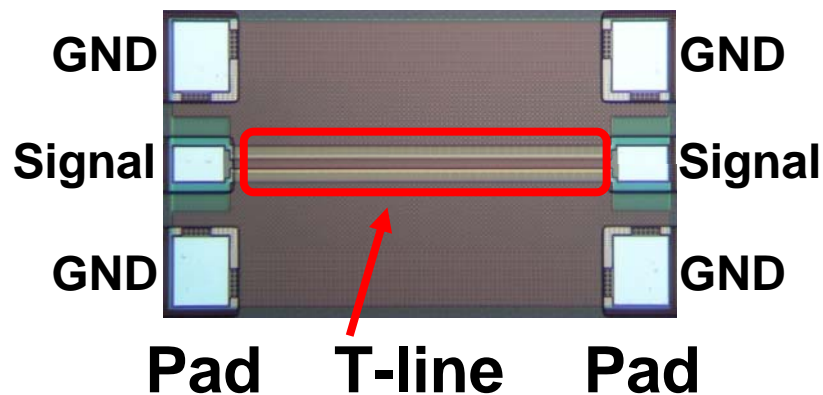
Each component is implemented as an in-house PDK for Agilent ADS.

- **Tile-based layout**
 - Layout and circuit model are strictly corresponded, which contributes to avoid uncertainty caused by **dummy metals** and **interconnections** between circuit components.
- **Measurement**
 - mmW measurement is still challenging
 - Accuracy of **de-embedding** becomes a considerably sensitive at mmW frequencies.
- **Characterization**
 - No fab-provided PDK for mmW circuit design
 - Measurement is not so accurate
 - TEG is very important.

- Motivation
- Issues for mmW CMOS Circuits
- ➔ • Device Characterization
 - Transmission line
 - Branch & bend line
 - Transistor
 - Decoupling capacitor
 - 1-stage amplifier
 - DC probe
- De-embedding
- Conclusion

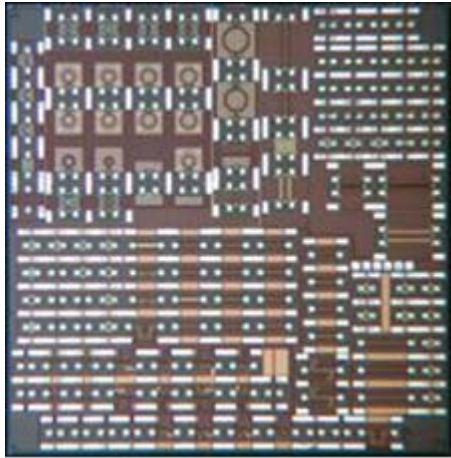
- Network analyzer
 - S-parameter measurement
- RF probe





- Transistors
- Transmission line
- Branch & bend line
- Spiral inductor
- Balun
- Series capacitor
- Decoupling capacitor

- DC pad
- RF pad
- Bonding wire



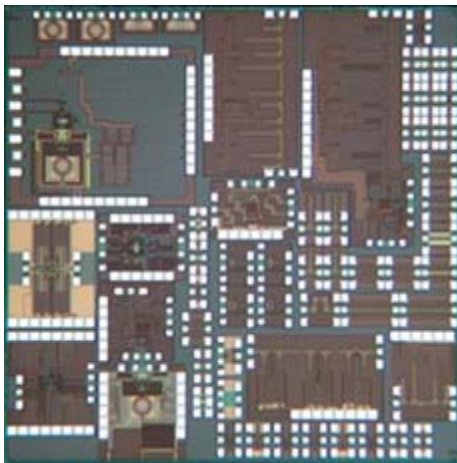
Initial T.O.

Initial T.O. for Modeling

- Transistors (CS, CG with various layouts)
- Transmission line (various length & Z_0)
- Branch & bend line
- Spiral inductor
- Balun
- Series capacitor
- Decoupling capacitor
- De-embedding patterns
- 1-stage amplifier for the model evaluation
- DC probe

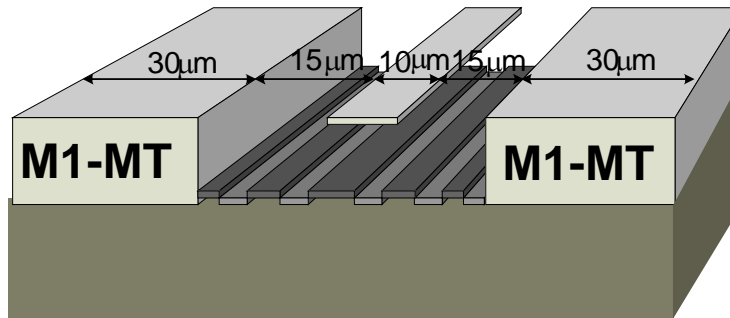
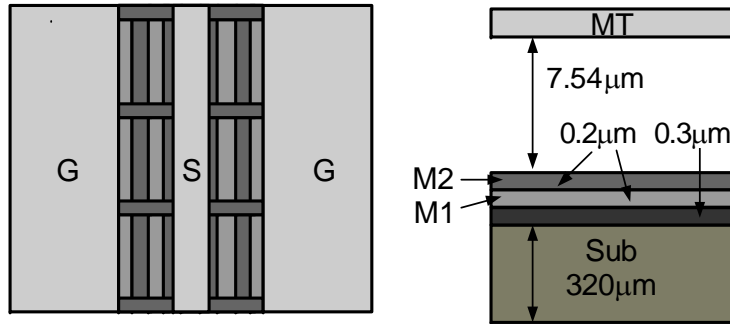
Second T.O.

- Circuit building blocks
- Whole system

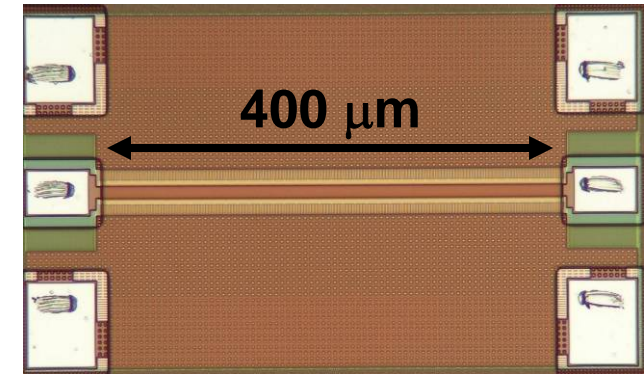


Second T.O.

- Motivation
- Issues for mmW CMOS Circuits
- Device Characterization
 - ➔ – Transmission line
 - Branch & bend line
 - Transistor
 - Decoupling capacitor
 - 1-stage amplifier
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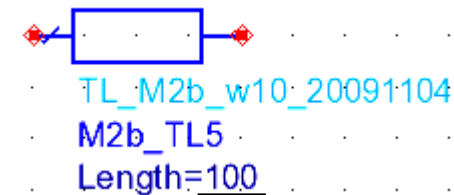
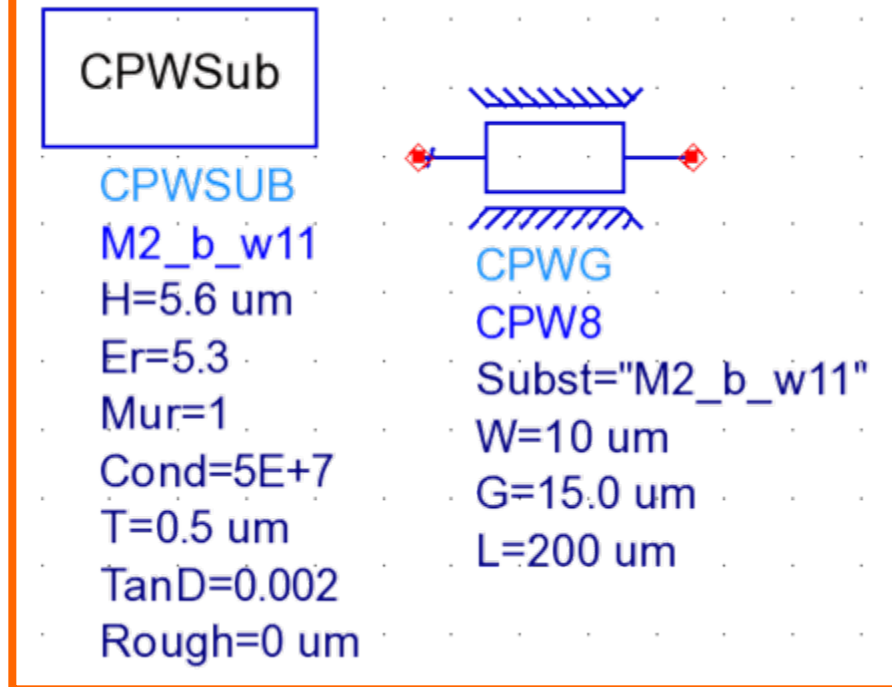
Structure



Microphoto

- Guided Micro-Strip (GMS)
- M1-MT ground wall (for density)
- Totally shielding the substrate from the signal line by using M1-M2 grounded-strips

CPW model (ADS)



configurable

- To meet measured α , β , Q and Z_0 , substrate model is individually extracted for each structure.
- RLGC is not good, and S-parameters should also be checked.

Z , α , β , and Q can be calculated from S-parameters.

$$e^{-\gamma l} = \left\{ \frac{1 - S_{11}^2 + S_{21}^2}{2S_{21}} \pm K \right\}^{-1} \quad K = \left\{ \frac{(S_{11}^2 + S_{21}^2 + 1)^2 - (2S_{11})^2}{(2S_{21})^2} \right\}^{\frac{1}{2}}$$

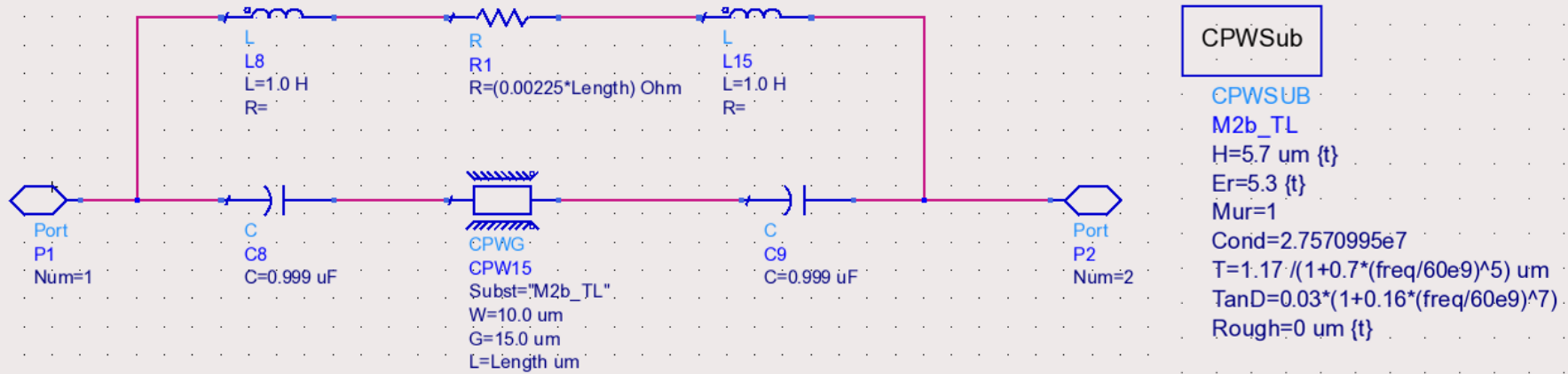
therefore

$$Z_0^2 = Z_{\text{ref}}^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2} \quad Q = \frac{\beta}{2\alpha}$$

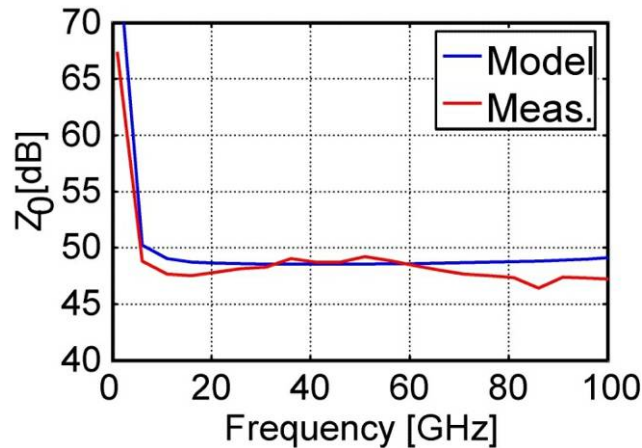
$$\gamma = \alpha + j\beta$$

W. R. Eisenstadt and Y. Eo, IEEE T-MTT 1992.

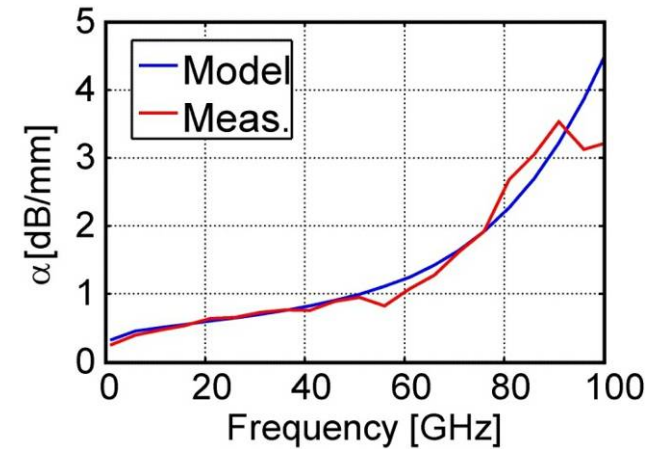
T-Line model (detail)



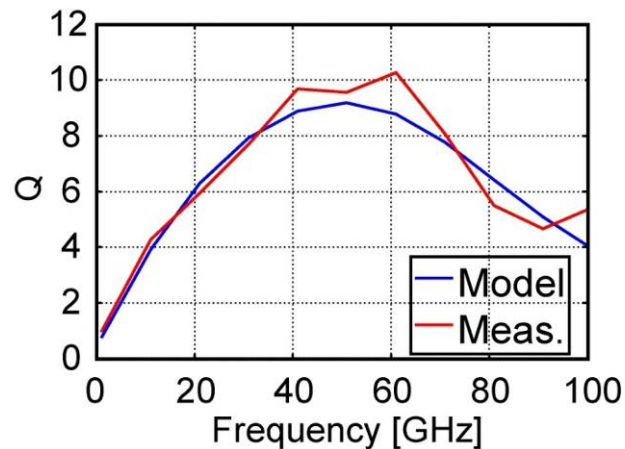
- DC characteristic is separately characterized.
- $\tan\delta$ and dielectric thickness are frequency-dependent.



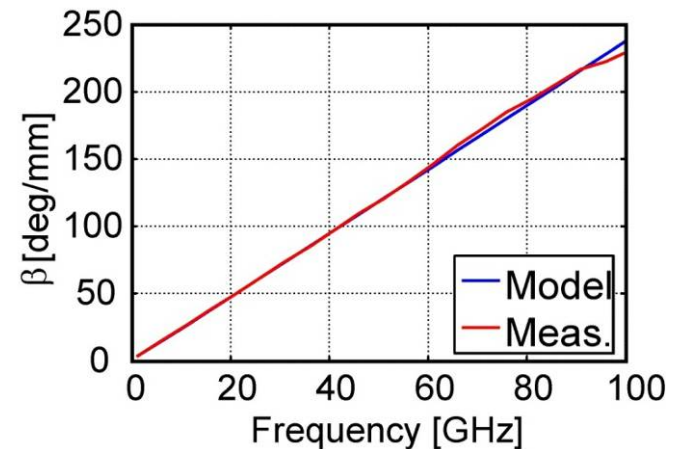
Characteristic impedance



Attenuation constant

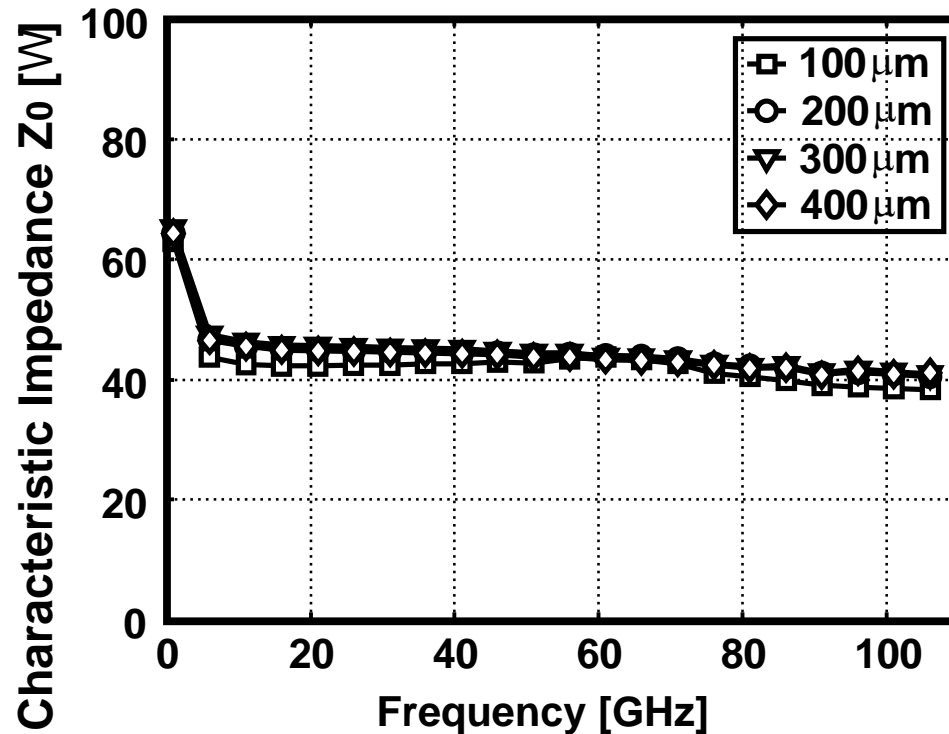


Quality factor



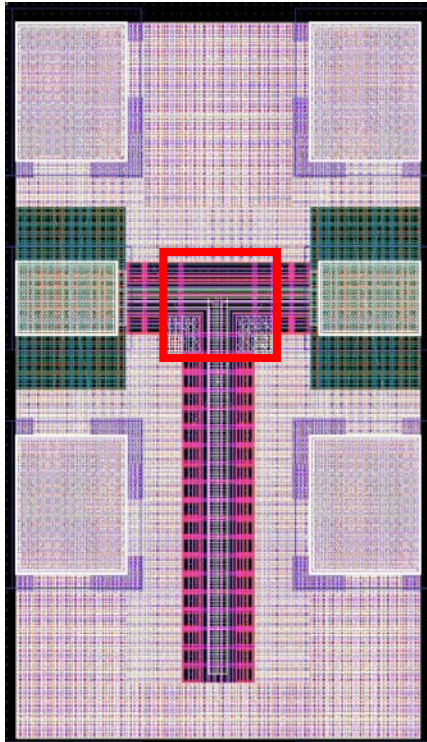
Phase constant

1. PAD model is built by measurement results of 200 μm and 400 μm T-lines.
2. Measurement results of 100 μm , 200 μm , 300 μm , and 400 μm T-lines are de-embedded by using the PAD model.

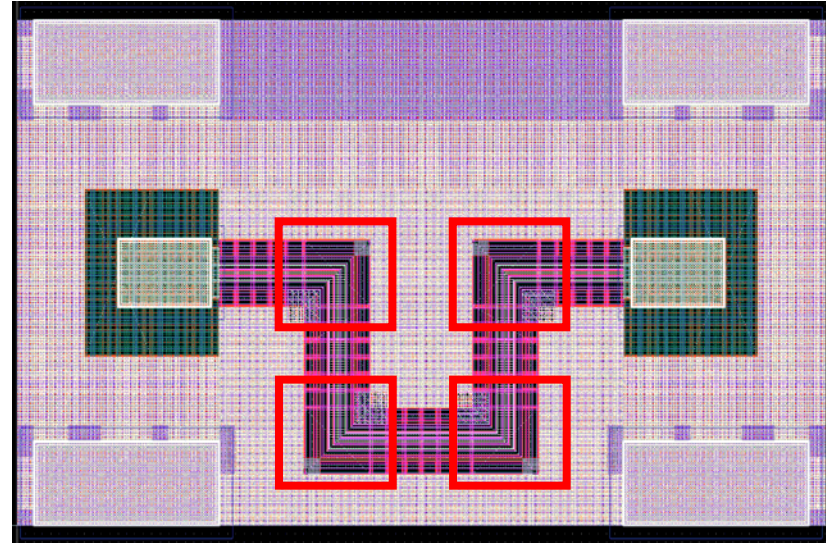


*different TL from the previous one

- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
 - Transmission line
 - ➔ – Branch & bend line
 - Transistor
 - Decoupling capacitor
 - 1-stage amplifier
 - DC probe
- **De-embedding**
- **Conclusion**

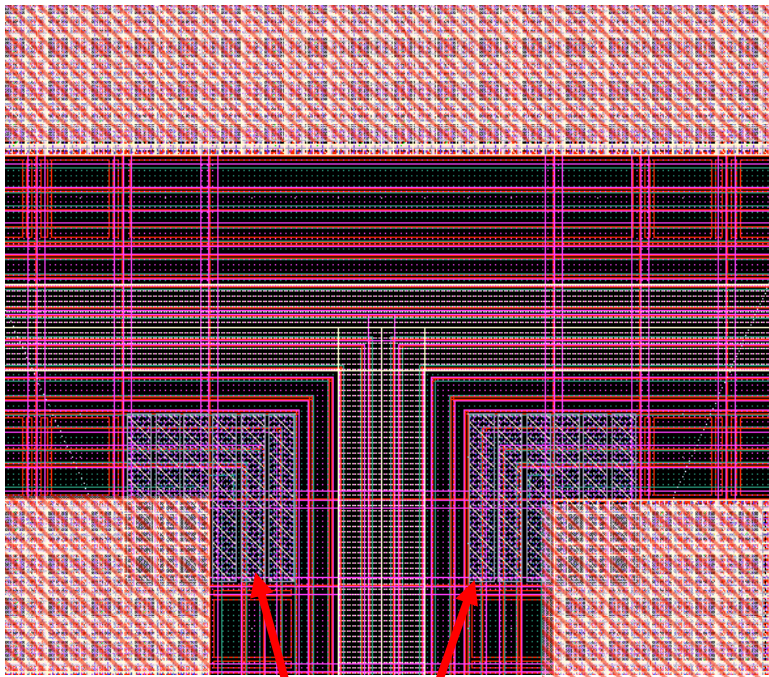


with 200 μm shunt TL



with 4 bending parts

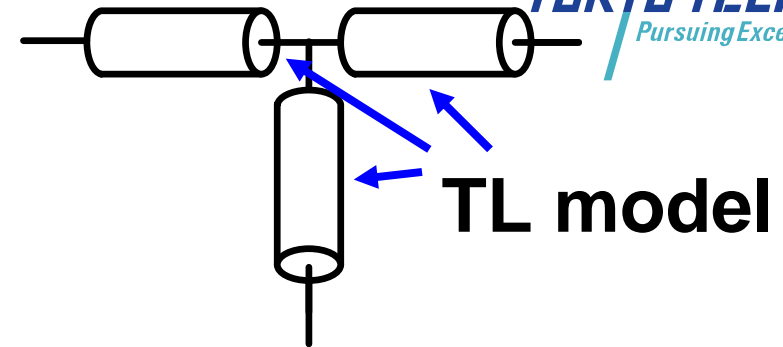
Each red-box part is characterized as a combination of optimized transmission lines.



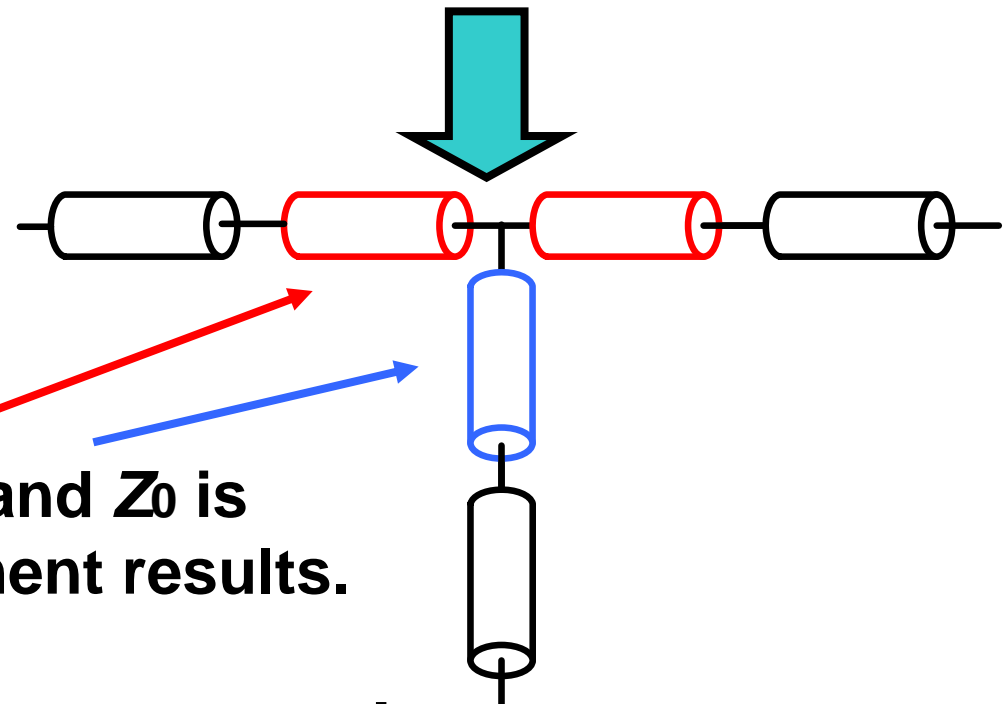
dummy metal

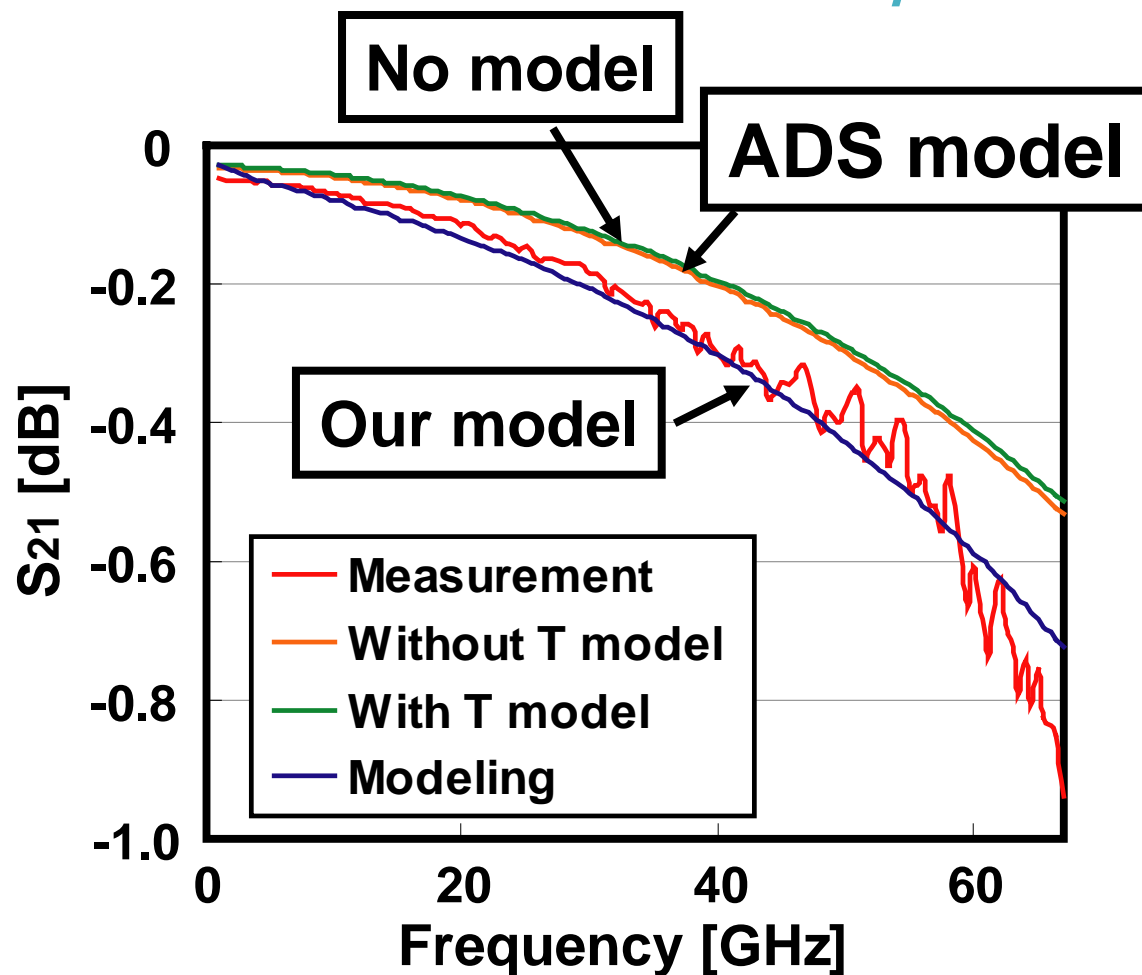
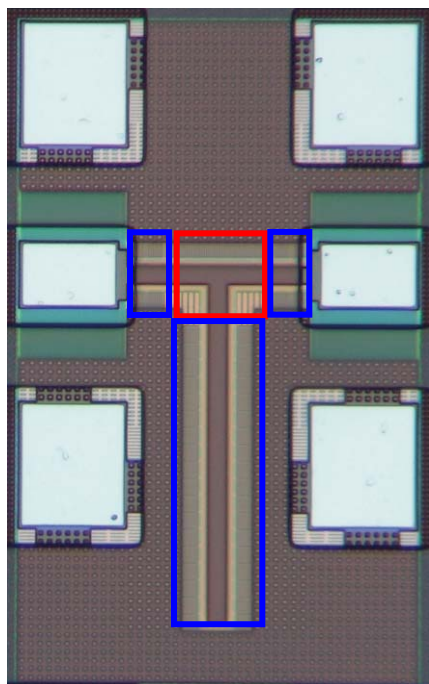
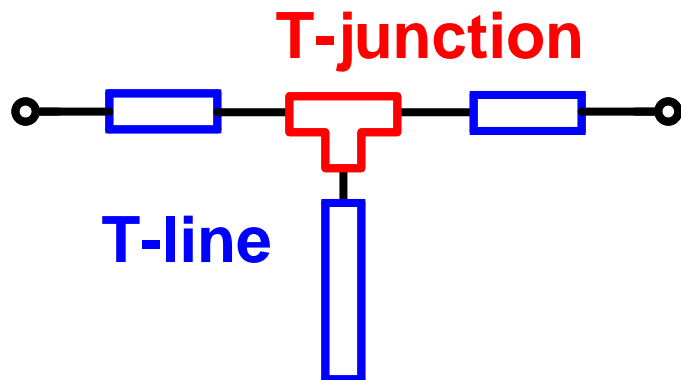
Lower Z_0 TLs are utilized, and Z_0 is adjusted for the measurement results.

Dummy metal causes unexpected response.

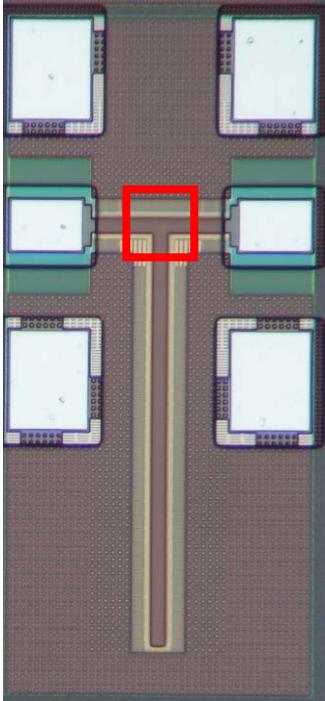


Straightforward modeling

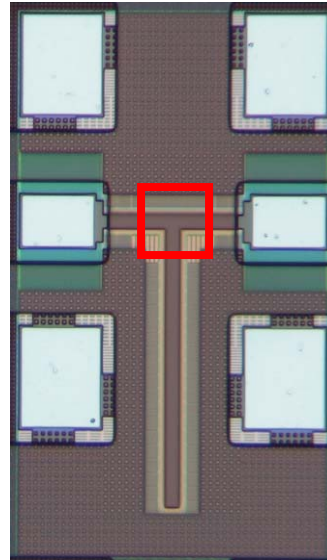




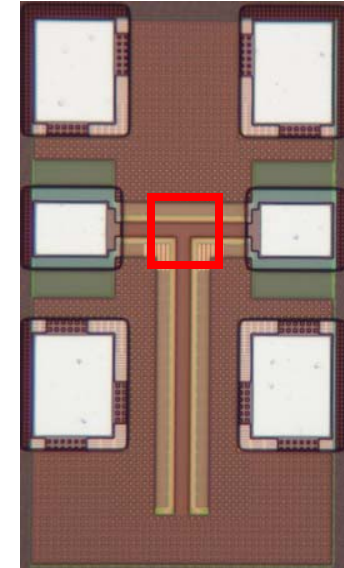
A simple analytical model cannot be used.



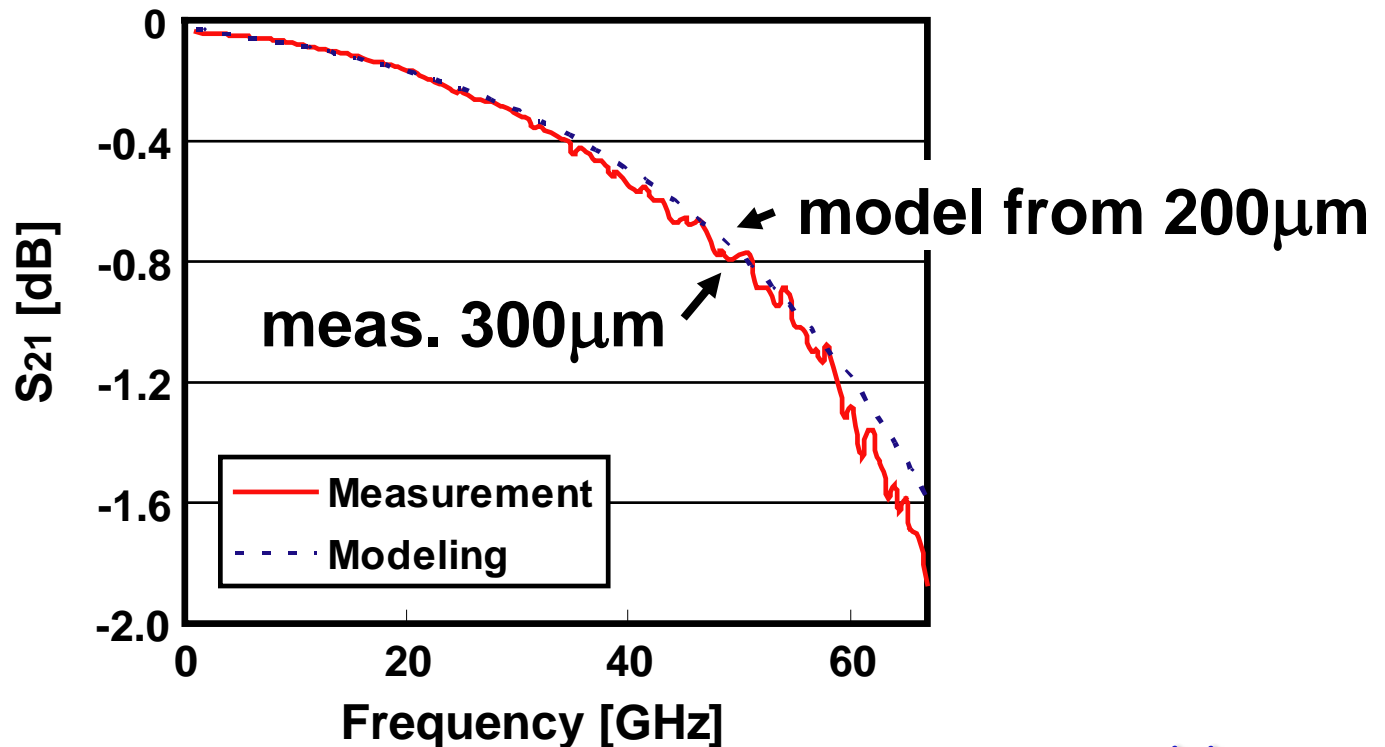
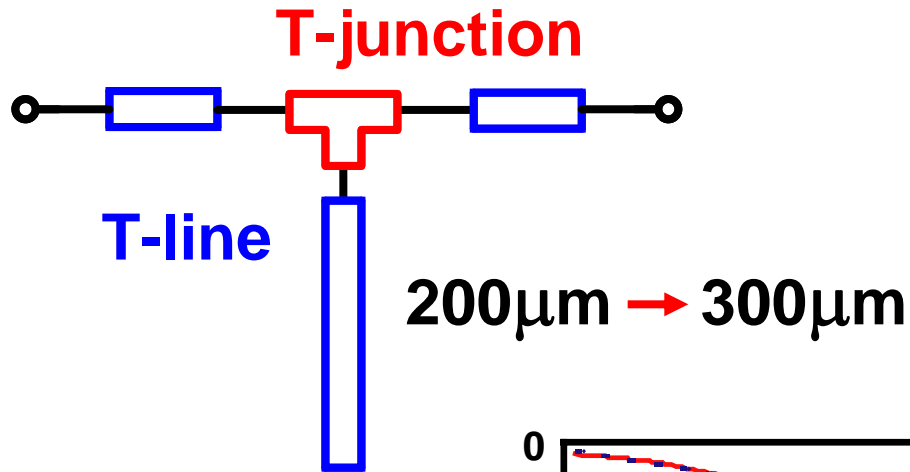
**300 μ m open-stub
used for verification**



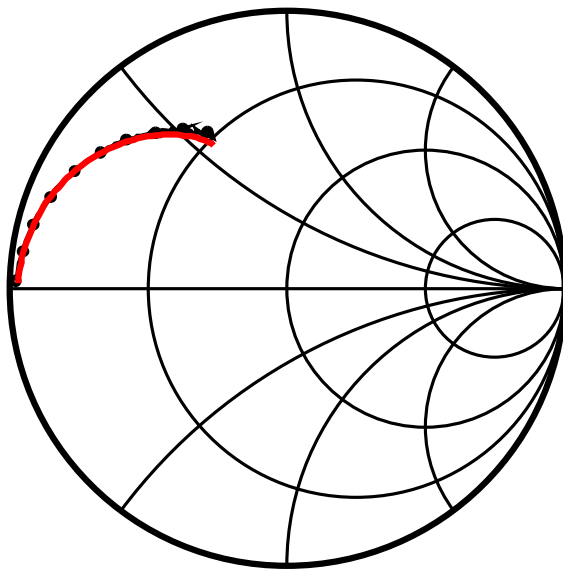
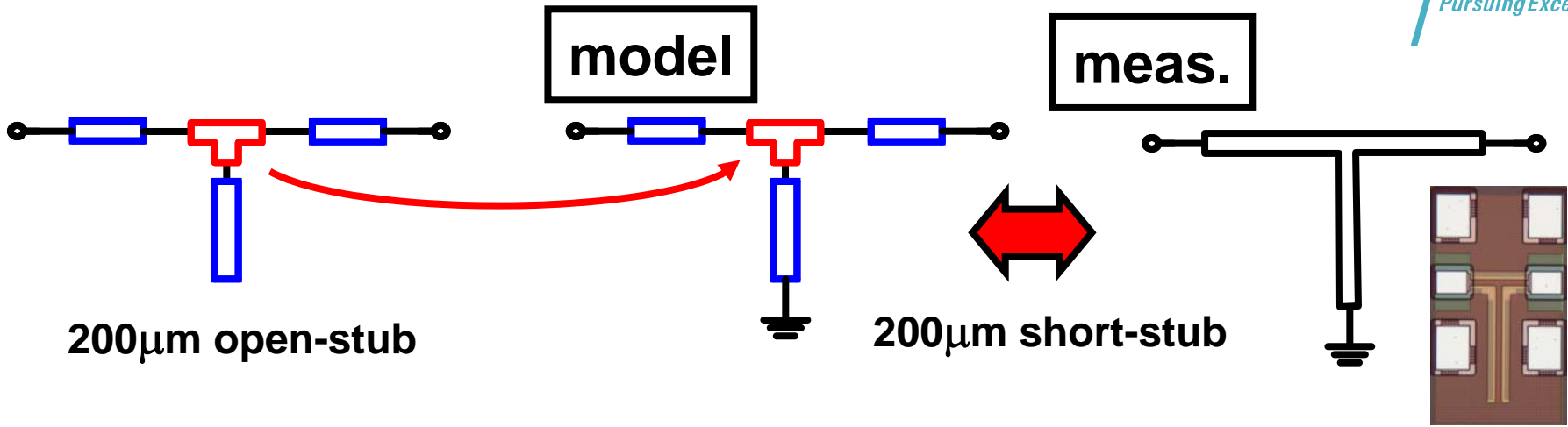
**200 μ m open-stub
used for modeling**



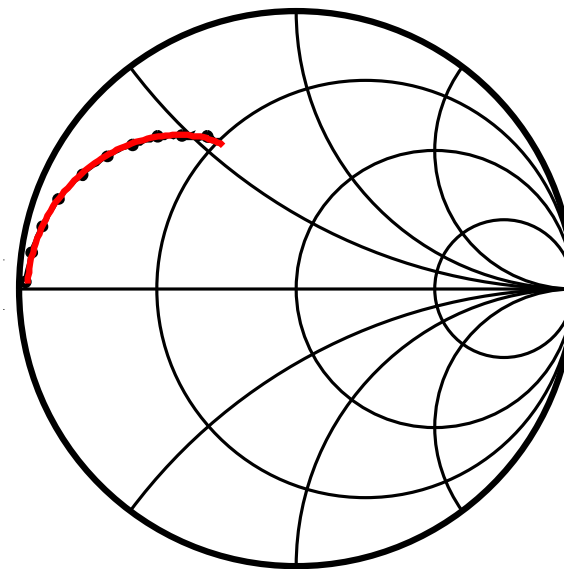
**200 μ m short-stub
used for verification**



Verification with short stub

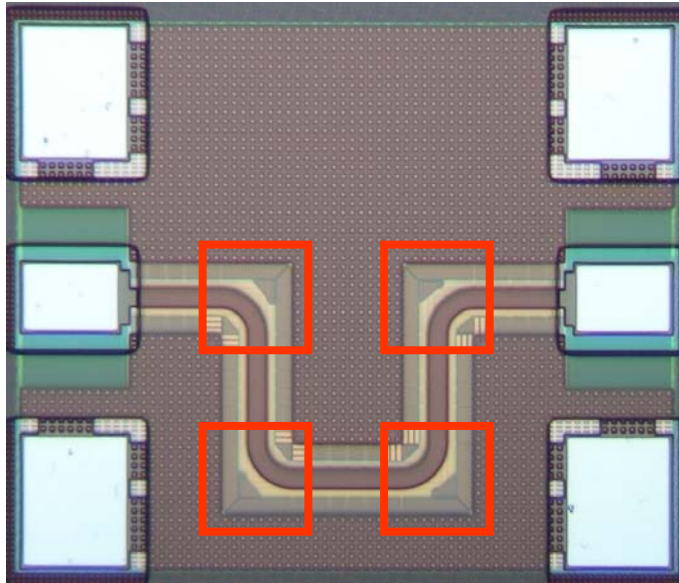


S_{11} (1-67GHz)

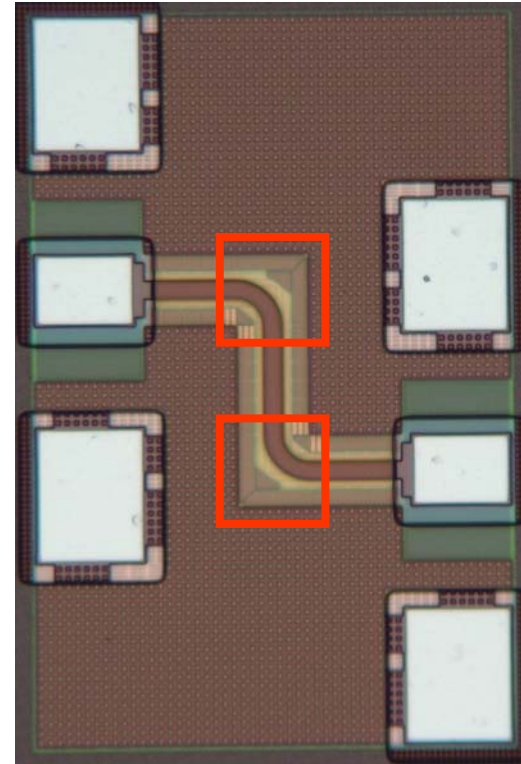


S_{22} (1-67GHz)



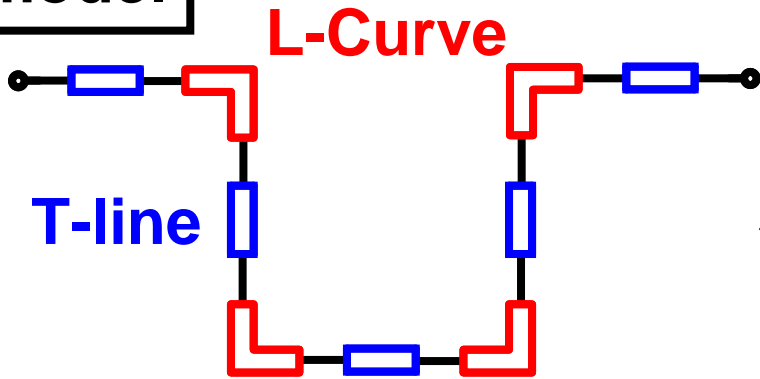


4-L-curve

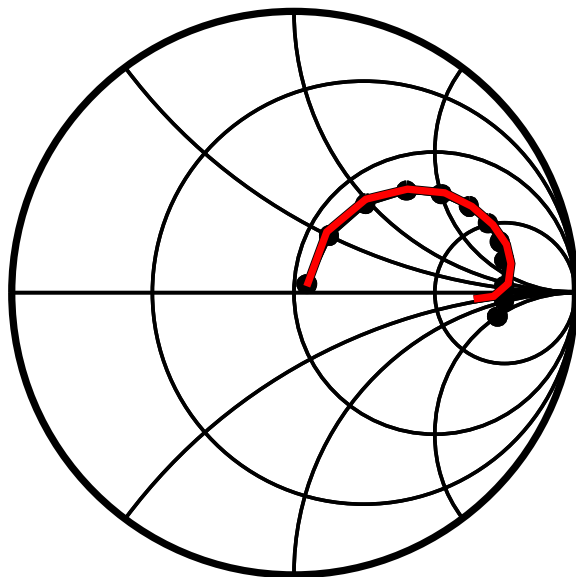
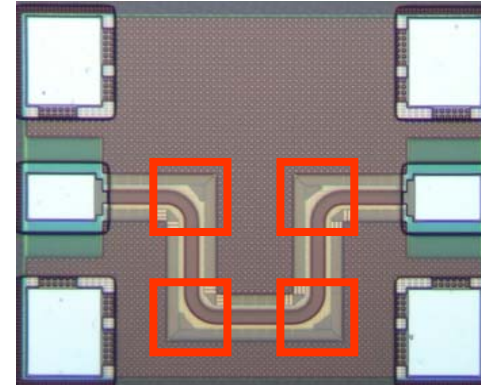


2-L-curve

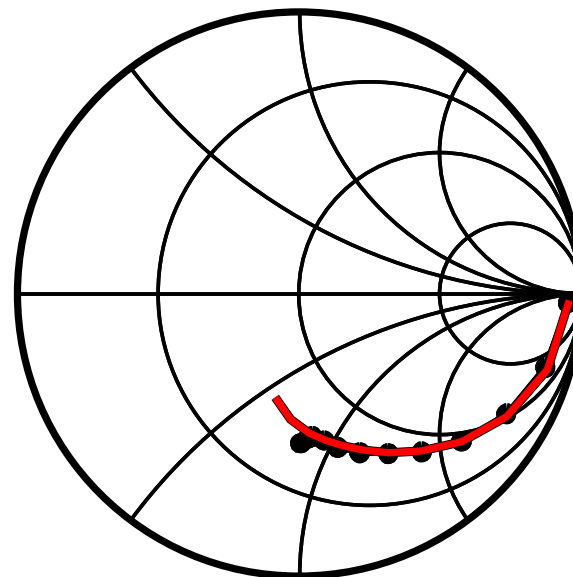
model



meas.



S_{11} (1-67GHz)

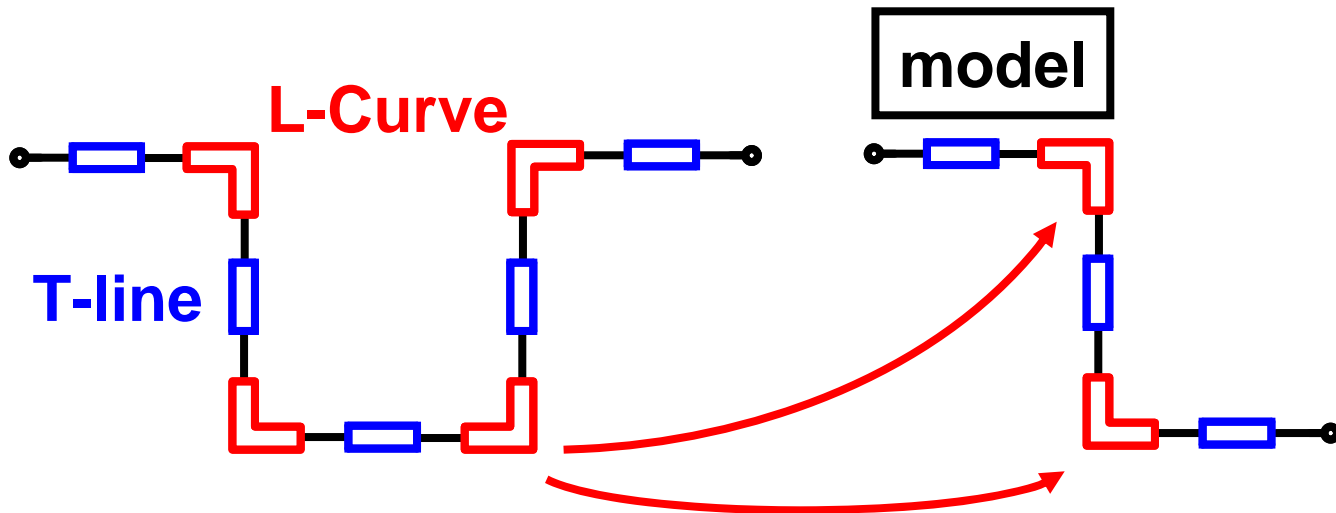


S_{21} (1-67GHz)

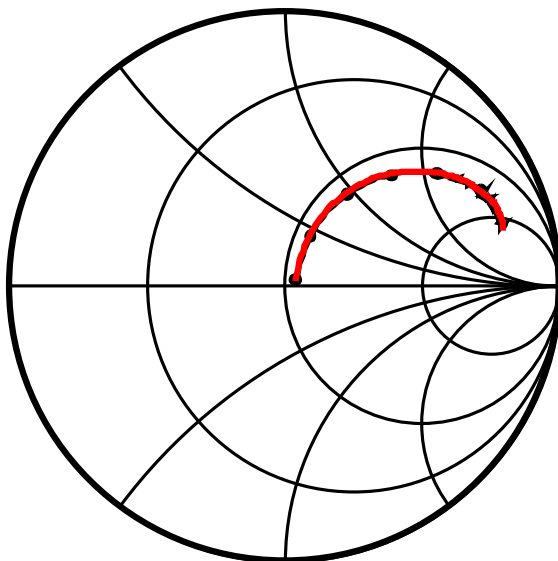
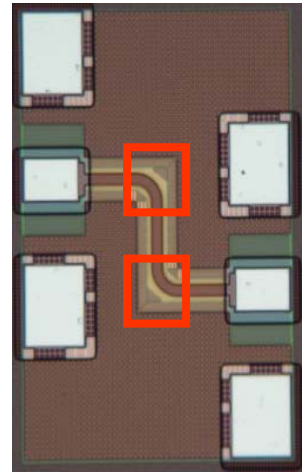
● Meas.
— Model

normalized by 20Ω

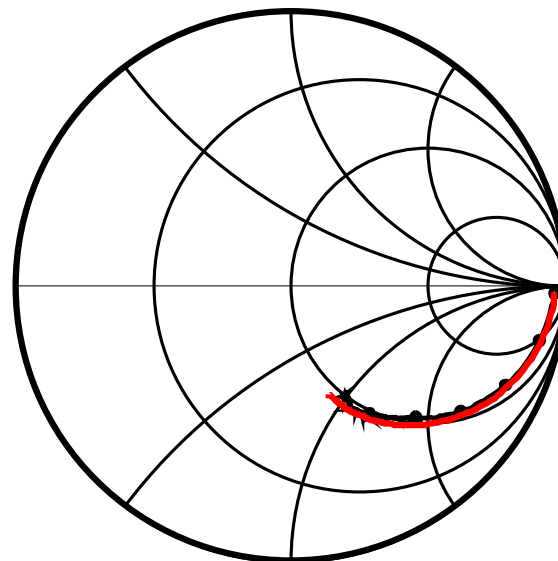
Verification with 2-bend



meas.



S_{11} (1-67GHz)



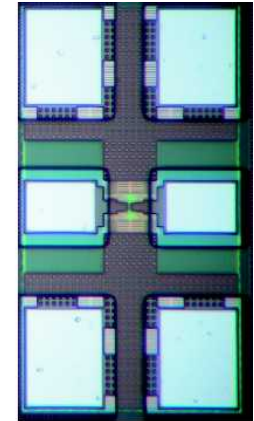
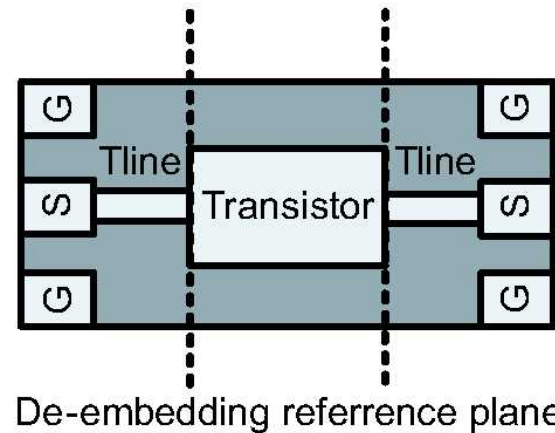
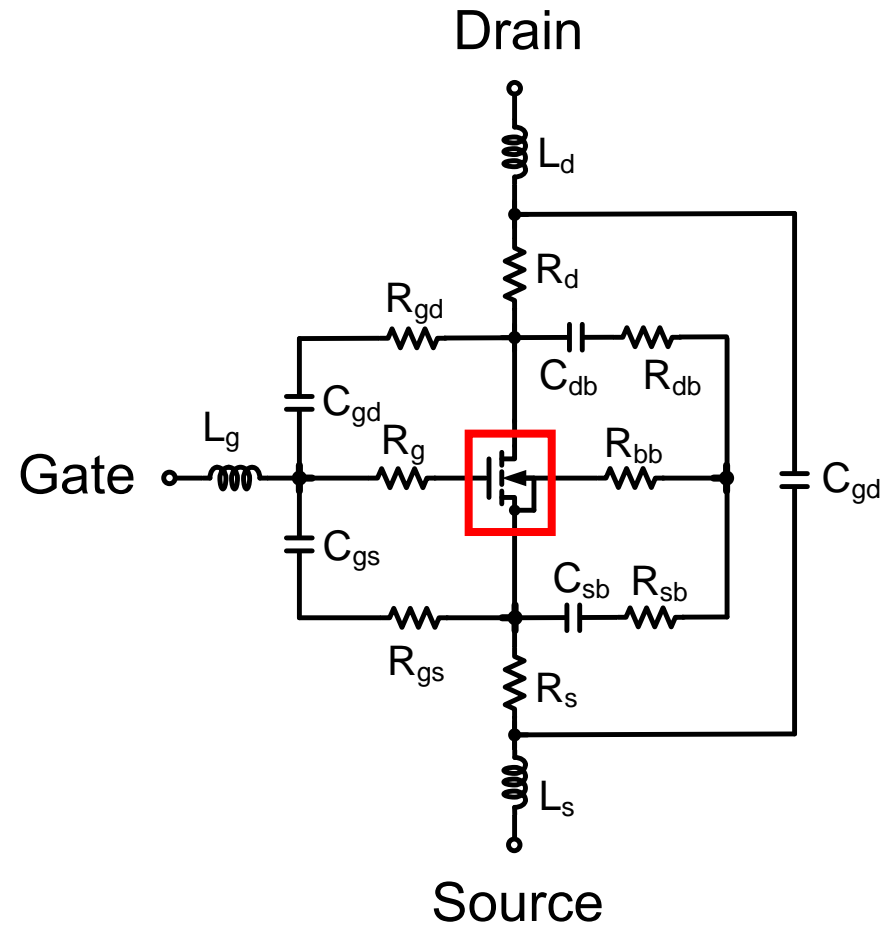
S_{21} (1-67GHz)

● Meas.
— Model

normalized by 20Ω

- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
 - Transmission line
 - Branch & bend line
 - ➔ – Transistor
 - Decoupling capacitor
 - 1-stage amplifier
 - DC probe
- **De-embedding**
- **Conclusion**

- Tr. is modeled from two-port measured results



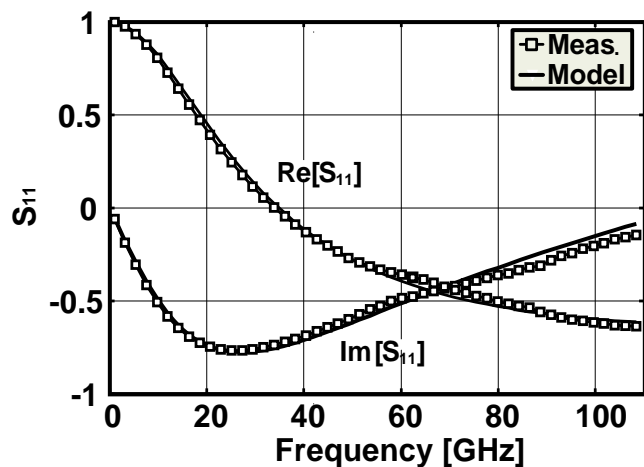
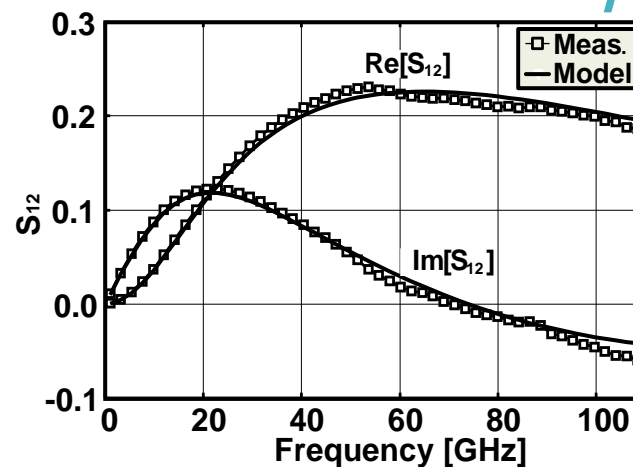
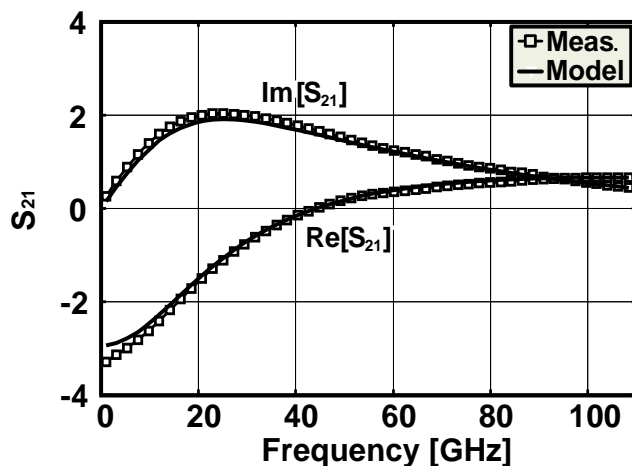
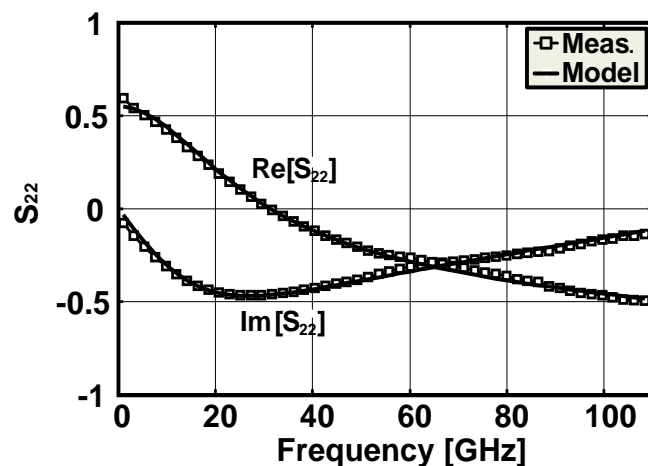
Test structure

Microphoto

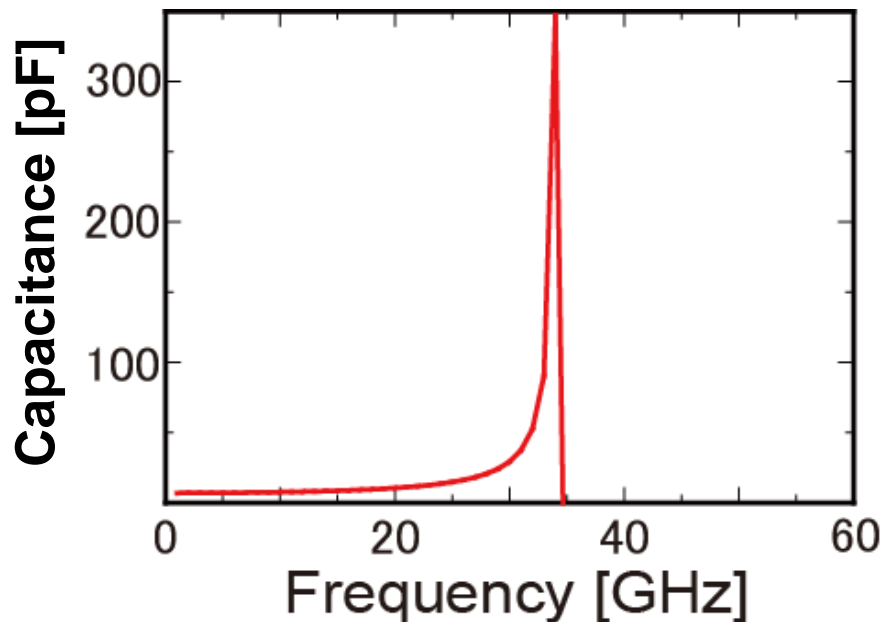
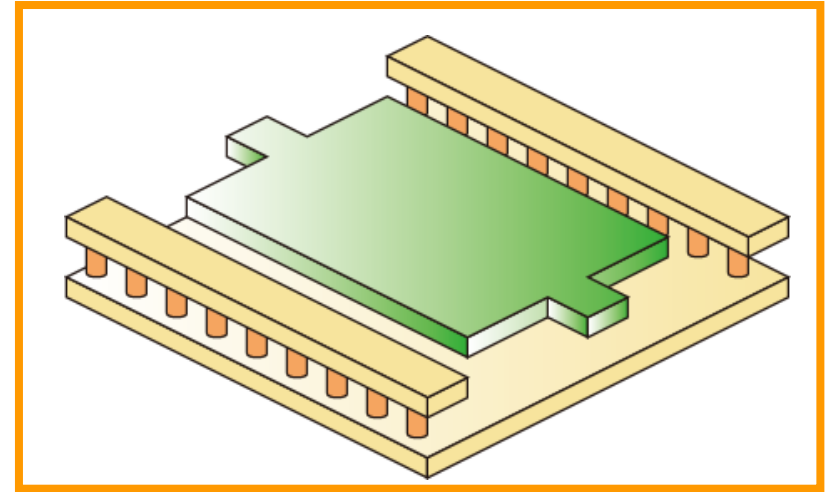
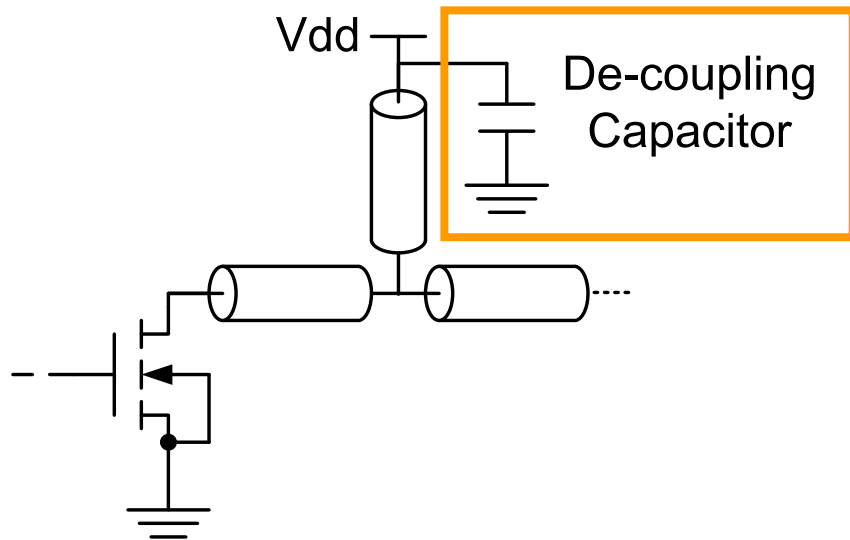
- Based on BSIM4 model
- Small signal
- With external ind., cap., res.

Transistor model

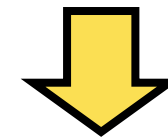
Extracted results of Tr model

 S_{11}  S_{12}  S_{21}  S_{22}

- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
 - Transmission line
 - Branch & bend line
 - Transistor
 - ➔ – Decoupling capacitor
 - 1-stage amplifier
 - DC probe
- **De-embedding**
- **Conclusion**



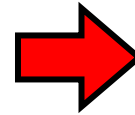
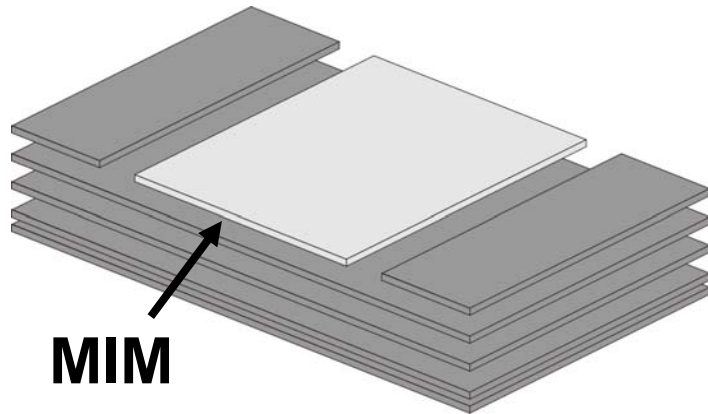
Area efficiency is large, but the self-resonance freq. is low.



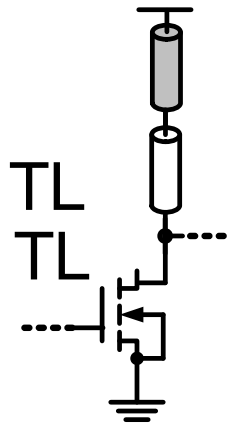
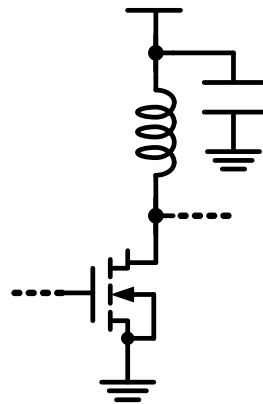
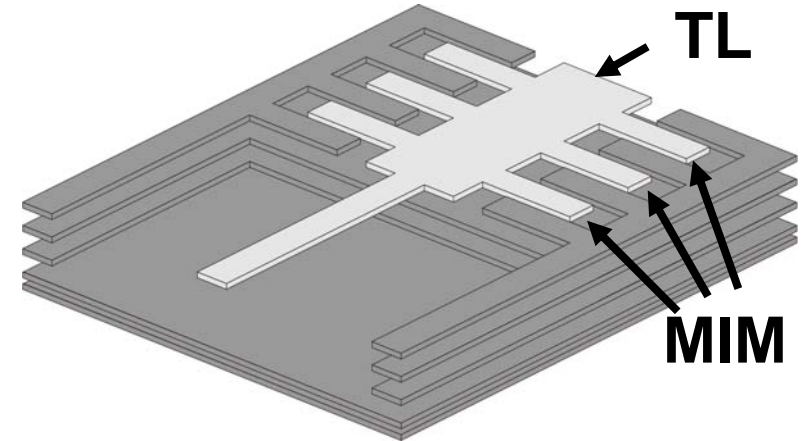
The regular layout of MIM cap. cannot be used at 60GHz.

TL-shape MIM capacitor

parallel plate MIM cap.



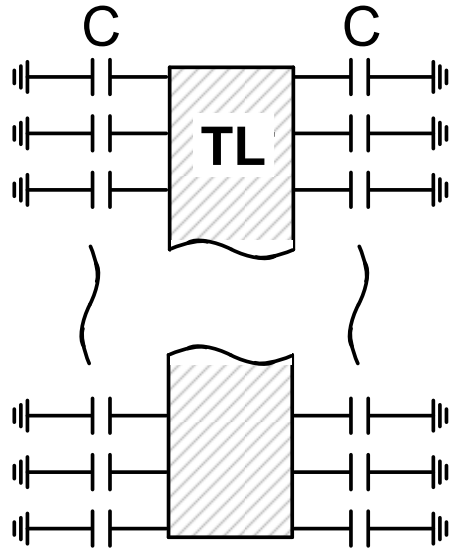
TL arranged MIM cap.[1]



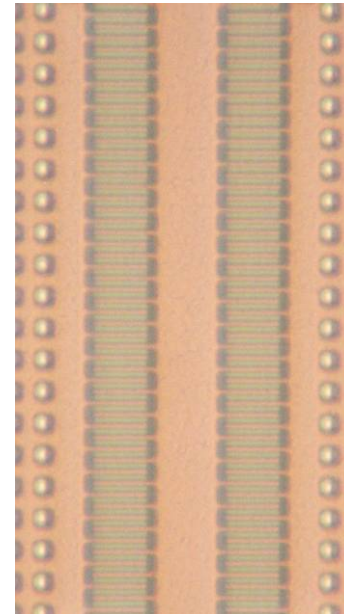
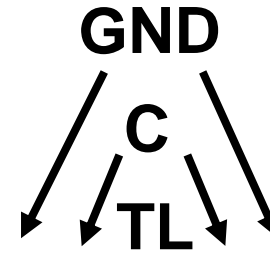
[1] T.Suzuki, *et al.*, ISSCC 2008.

[2] Y.Natsukari, *et al.*, VLSI Circuits 2009.

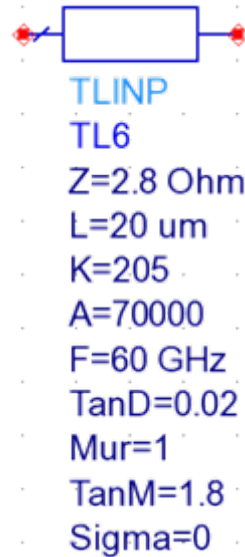
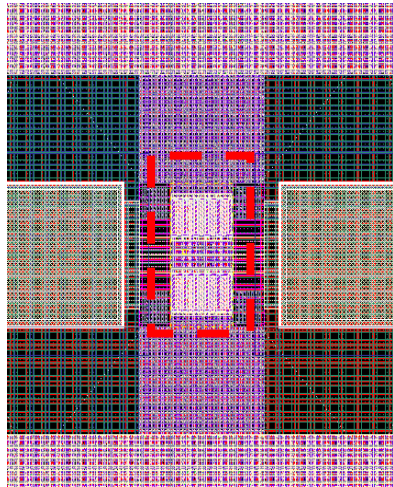
Extendable for length



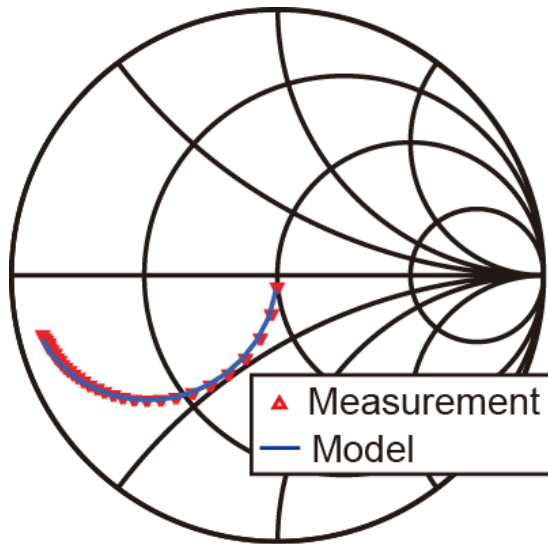
MIM TLine structure



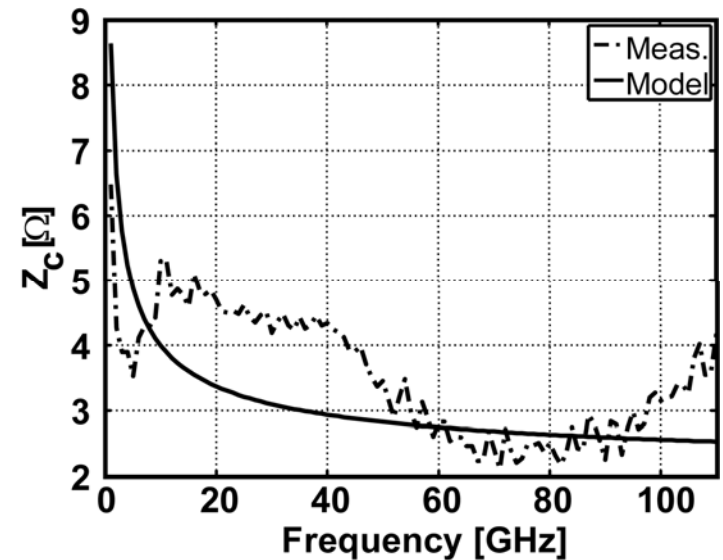
Microphoto



Characterized as a transmission line



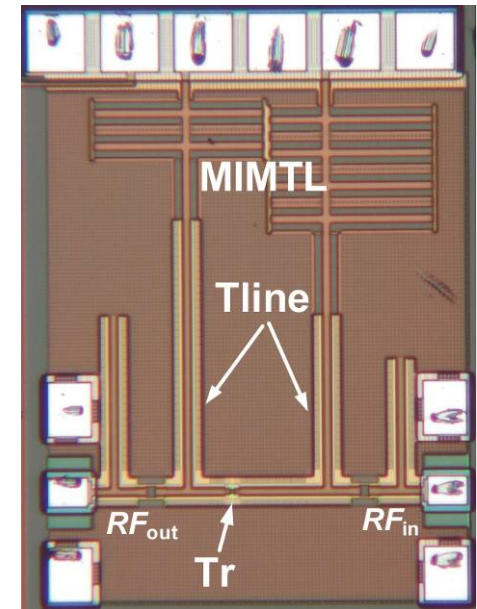
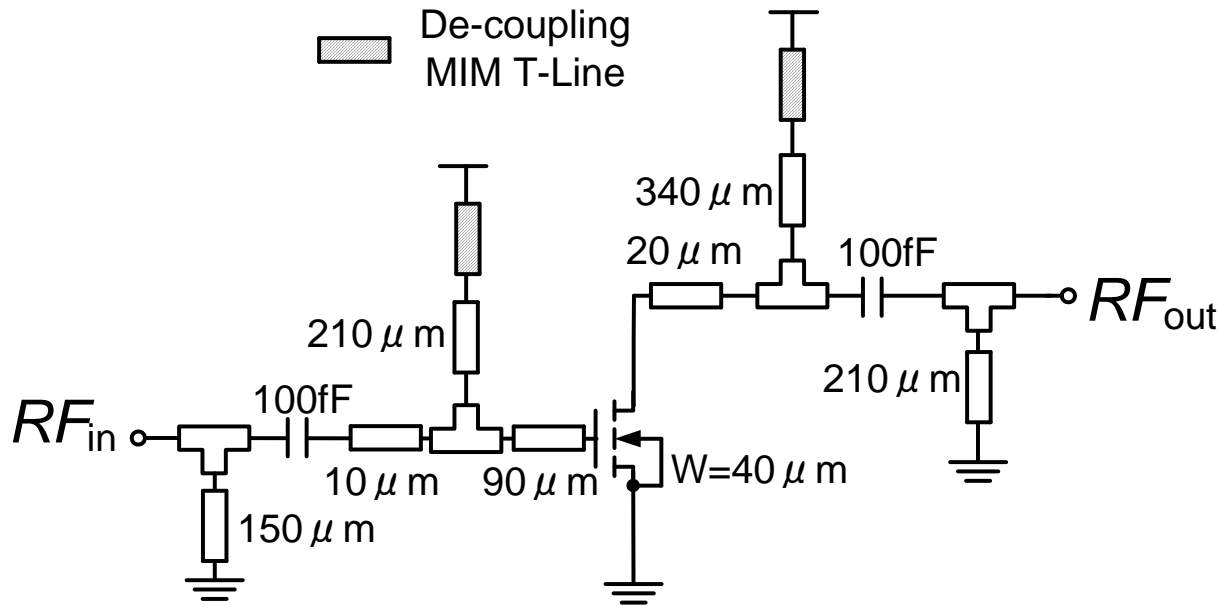
S_{11} (1-67GHz)



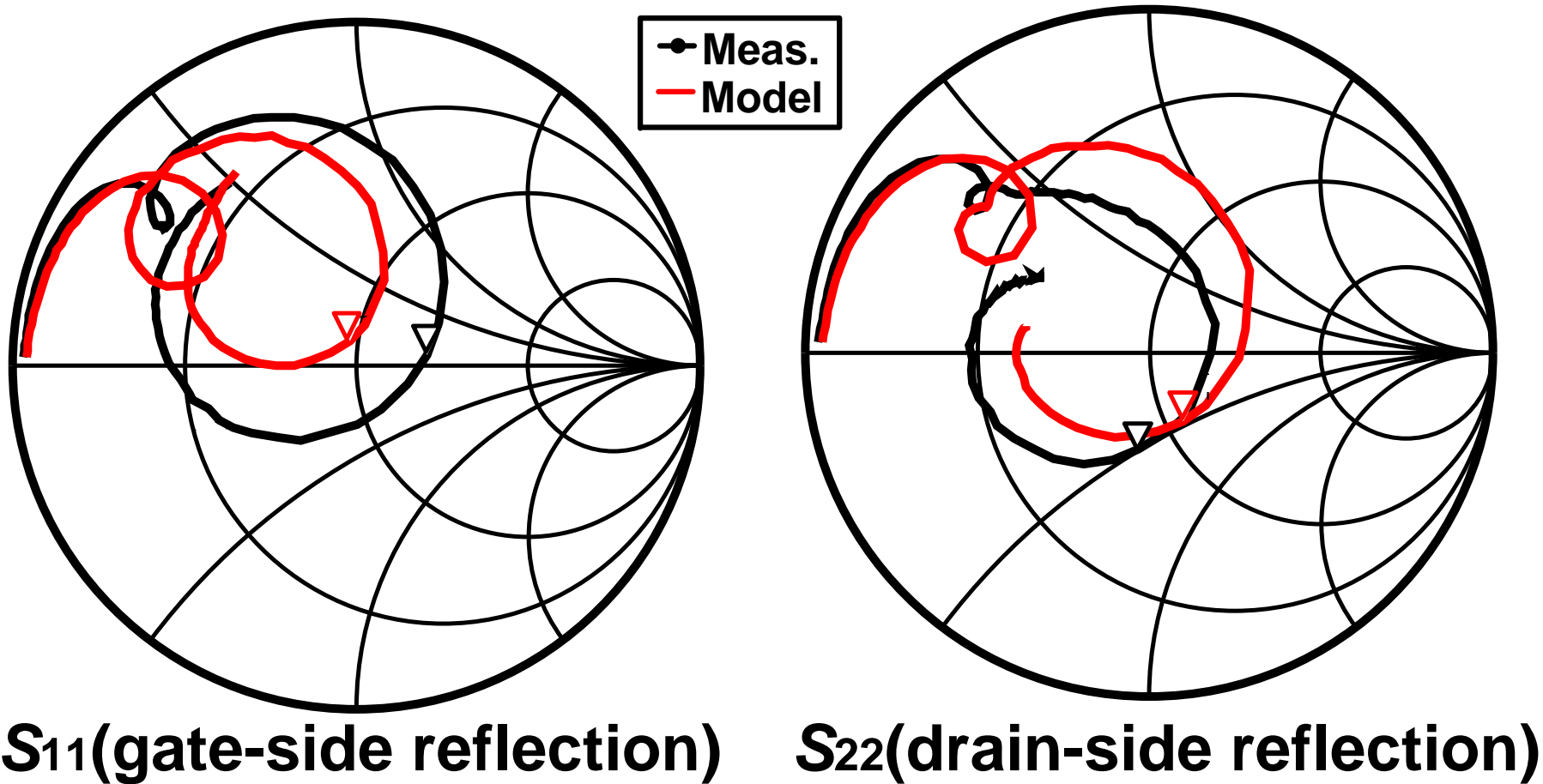
Z_0

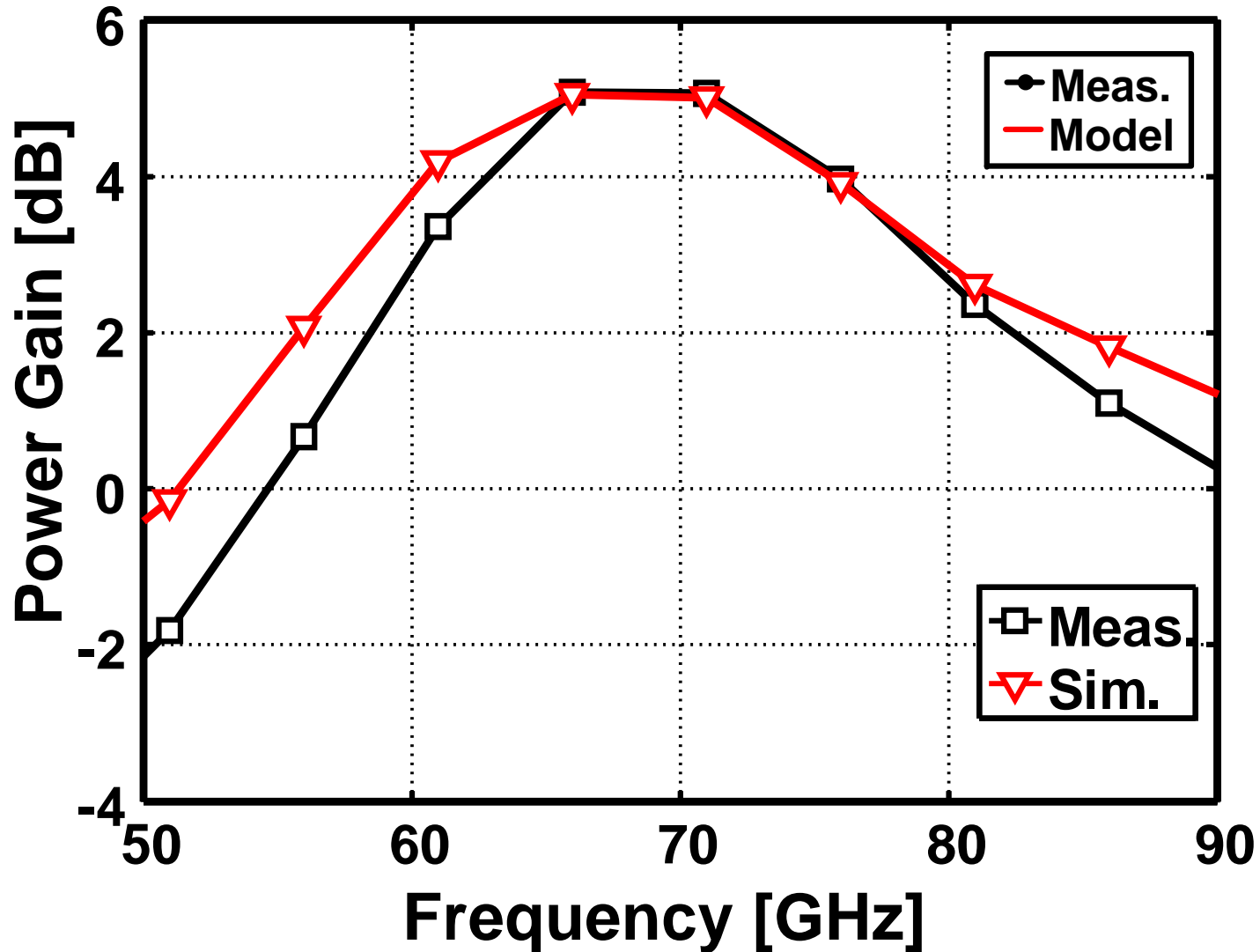
- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
 - Transmission line
 - Branch & bend line
 - Transistor
 - Decoupling capacitor
 - ➔ – 1-stage amplifier
 - DC probe
- **De-embedding**
- **Conclusion**

A 1-stage amplifier is also used for a verification.



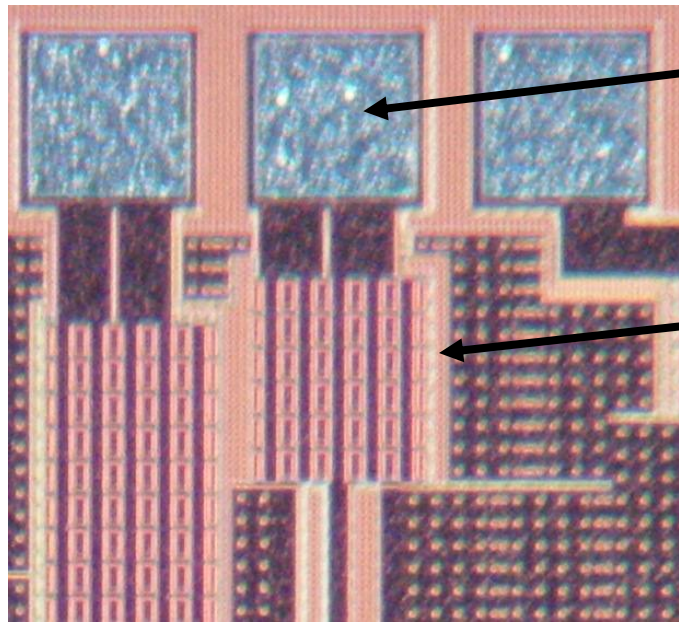
Schematic





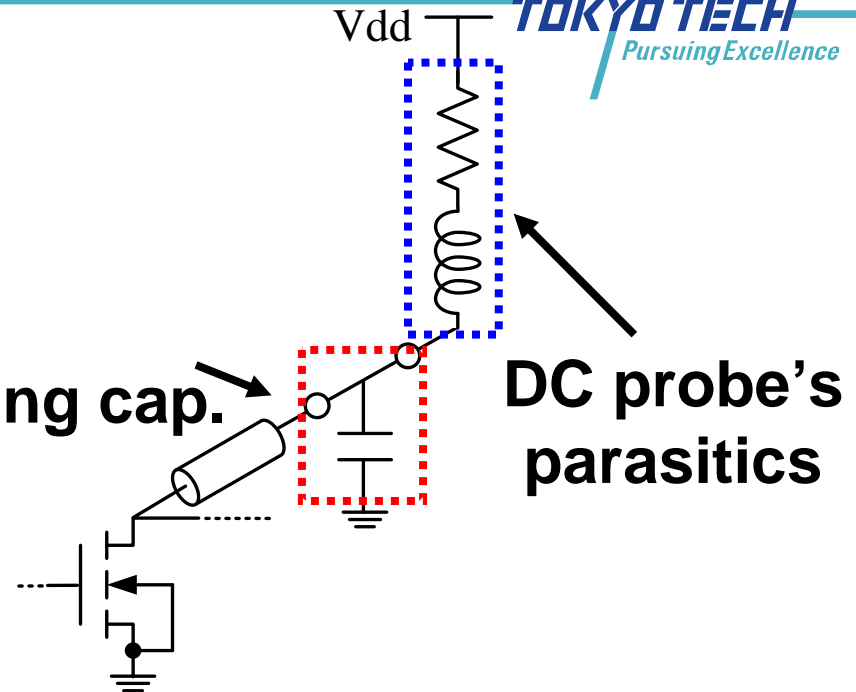
- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
 - Transmission line
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 - ➔ – DC probe
- **De-embedding**
- **Conclusion**

DC probe impedance



DC pad

On-chip de-coupling cap.



DC probe's parasitics

100MHz

1GHz

10GHz

100GHz

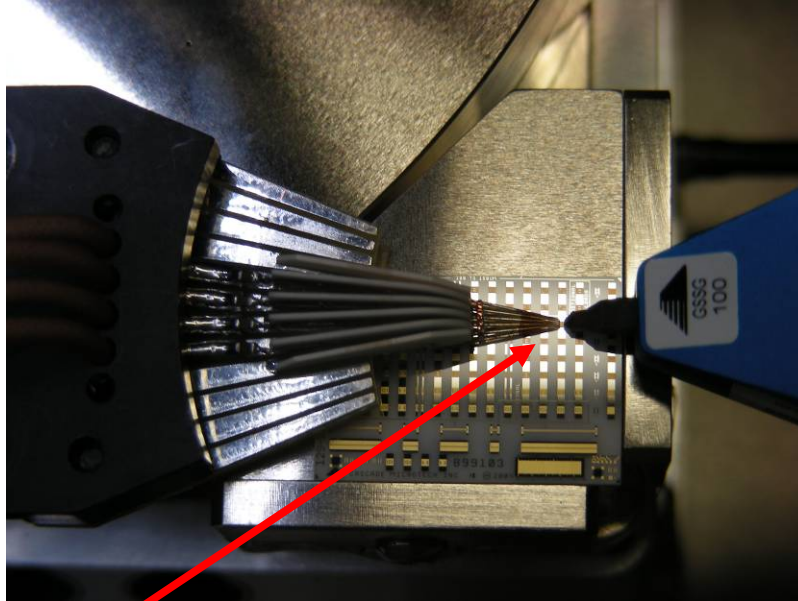


External de-coupling capacitor works well. e.g., DC probe

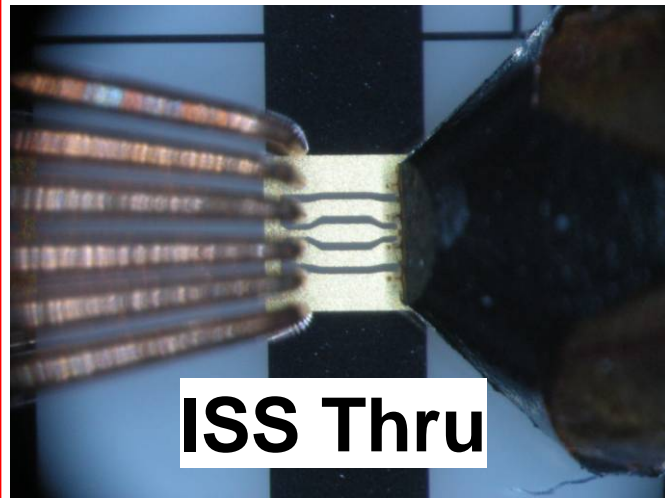
Supply impedance is not stable. Oscillation

On-chip de-coupling capacitor works well.

DC
Probe
(DUT)



RF
Probe



ISS Thru

- DC pad/probe is characterized, and it is taken into account in circuit simulation.
- RF pad is also characterized.

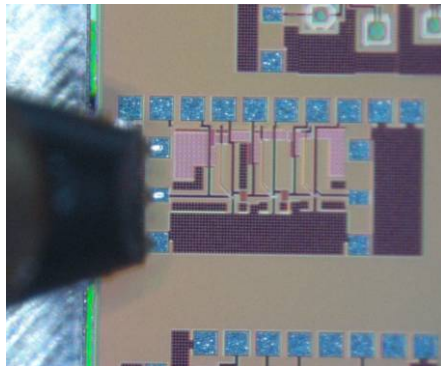
- De-embedding
- Transistor layout optimization
- Spiral inductor
- Balun
- RF Pad
- DC probe / bonding wire / bump / filler / PCB

A modeling approach to design a 60GHz CMOS amplifiers

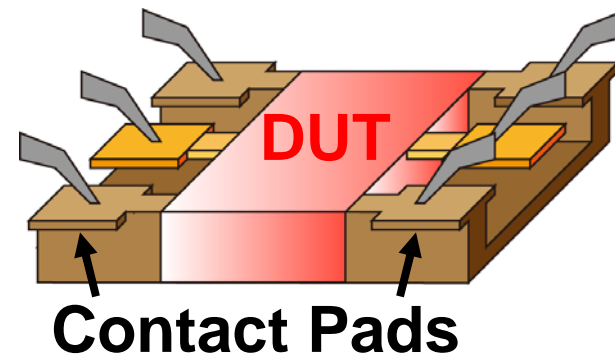
- 1. Design issue of TL on CMOS chips is different from that of compound semiconductors.**
e.g., dummy metal, lossy substrate, large conductive loss, etc
- 2. Branch modeling**
- 3. Distributed modeling of de-couple MIM cap.**
- 4. Evaluation using a 1-stage amplifier**

- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
- ➔ • **De-embedding**
 - **Open-Short, Thru-Only method**
 - **L-2L method**
- **Conclusion**

- On-wafer probing measurement
 - Contact pads are needed.
 - Measurement data includes pad parasitic components.
 - At high frequency, parasitic components are not negligible.
- De-Embedding
 - Remove parasitic components from measurement data

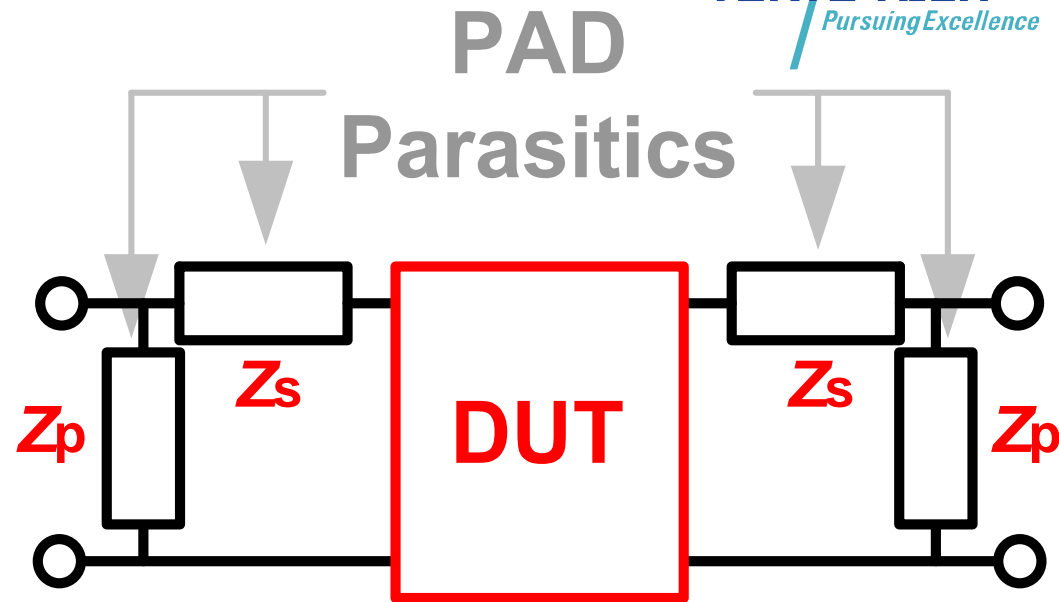
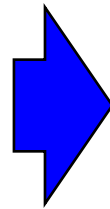
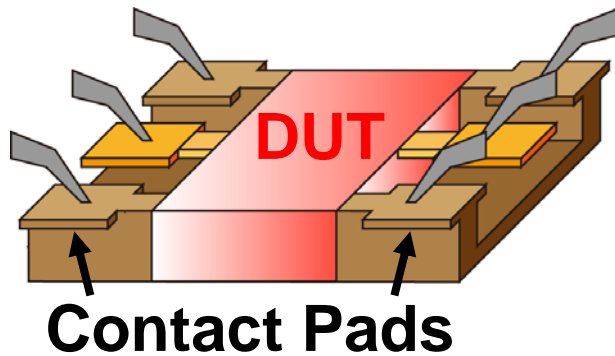


Measurement

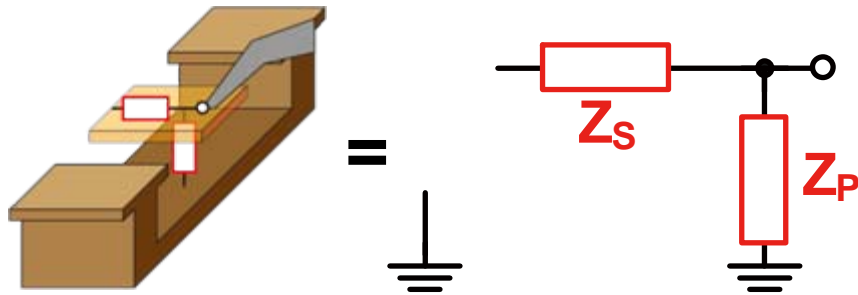
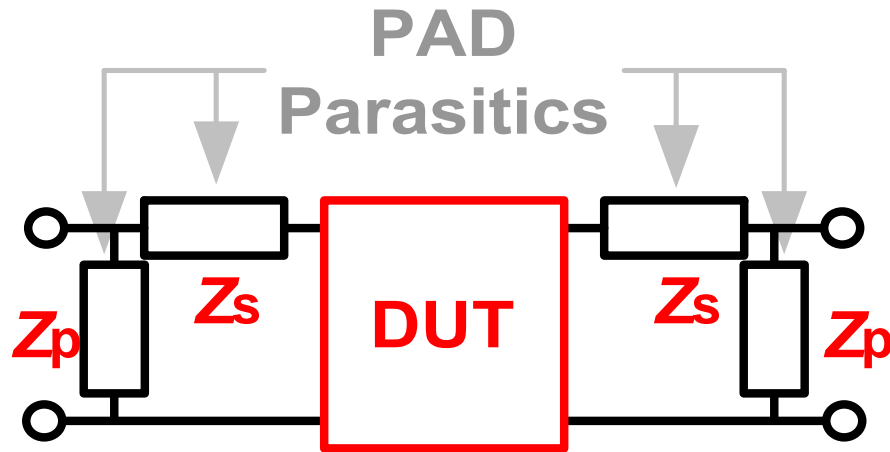


Parasitic elements of contact pads

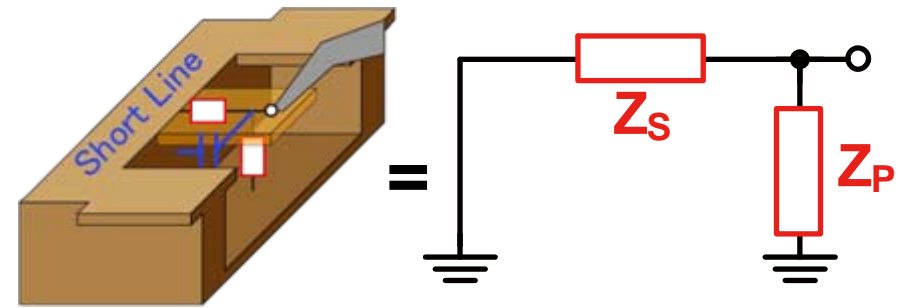
- **Lumped-constant approach**
 - **Open-Short**
 - **Open-Short-Thru**
 - **Thru-only**
- **Distributed-constant approach**
 - **L-2L**
 - **Mangan's method**
 - **Takayama's method**



- **Simple Series-and-Shunt model**
 - Z_p : Shunt parasitic components of contact pad
 - Z_s : Series parasitic components of contact pad
- **T-parameter model**
 - Characterized by 4 or 3 complex parameters



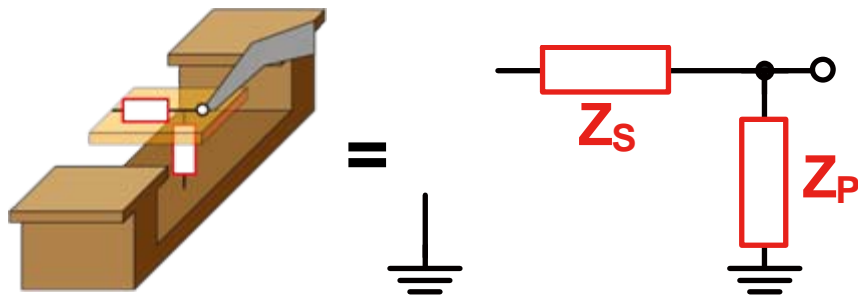
OPEN



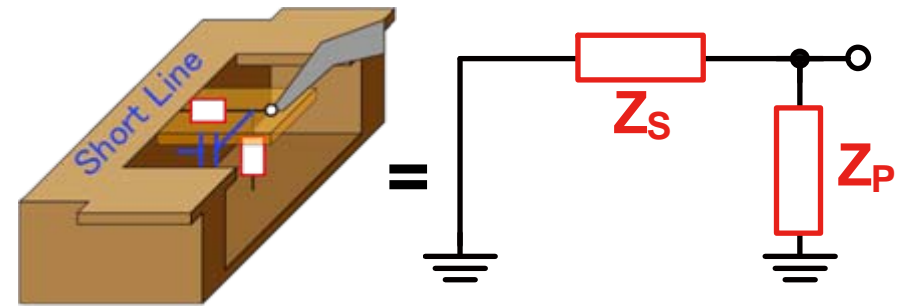
SHORT

Problem at high frequency

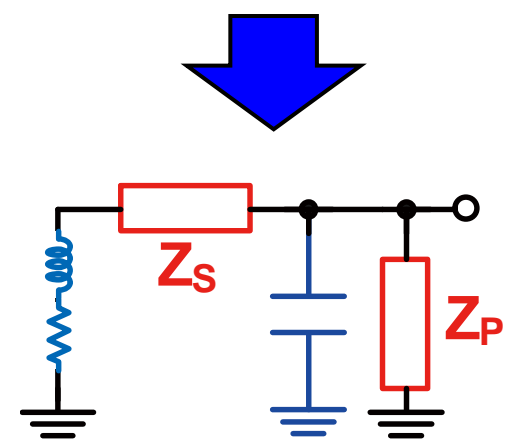
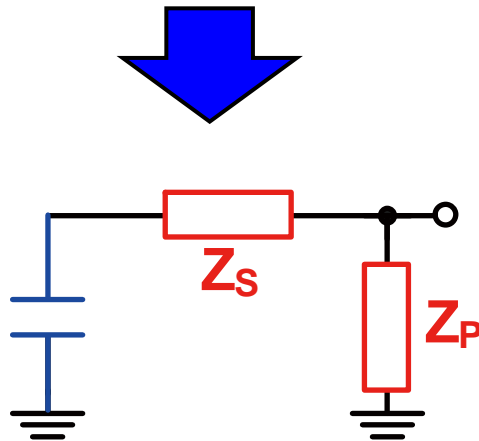
– Ideal short cannot be obtained.



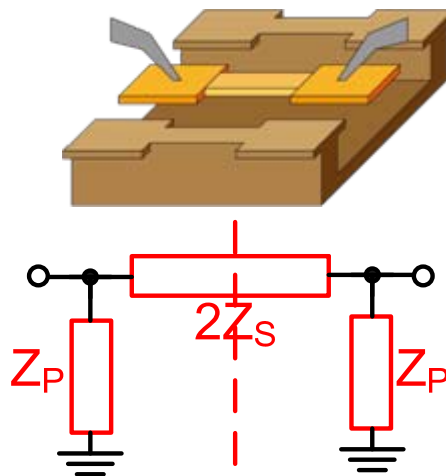
OPEN



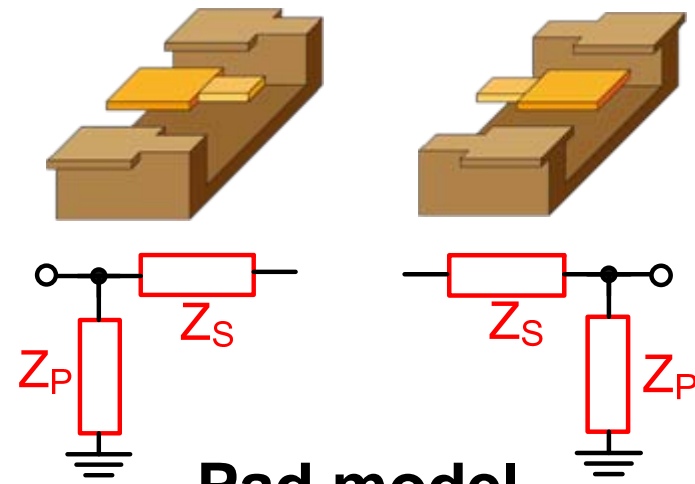
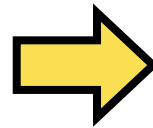
SHORT



- **Short-Line-Structure**
 - The measurement result is characterized as a “ π ”-PAD model.
 - Separate in two symmetric parts
- **Issue of this method at high frequency**
 - The line length must be short.
 - The distance between probes is too short.



Thru (short line) structure

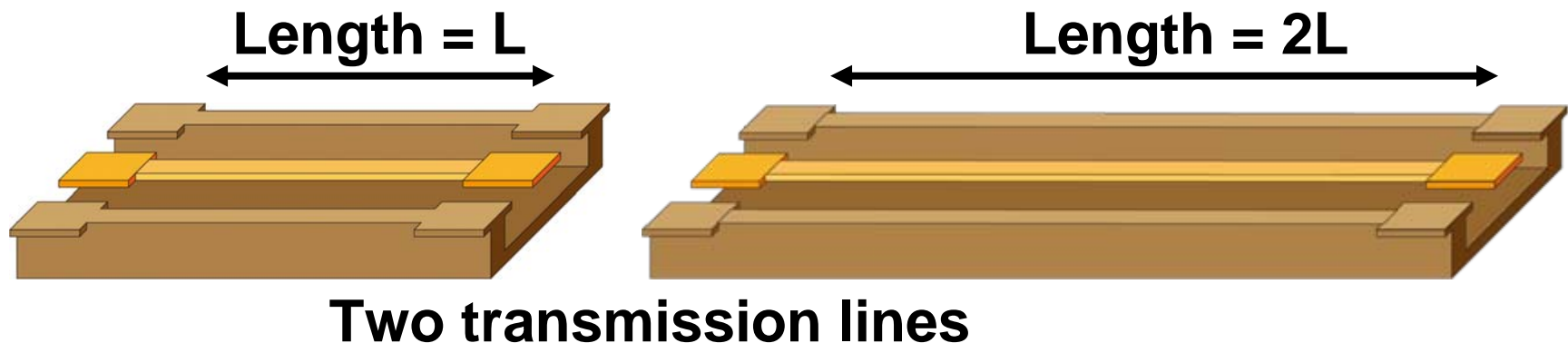


Pad model

*H. Ito, *et al.*, IMS 2008

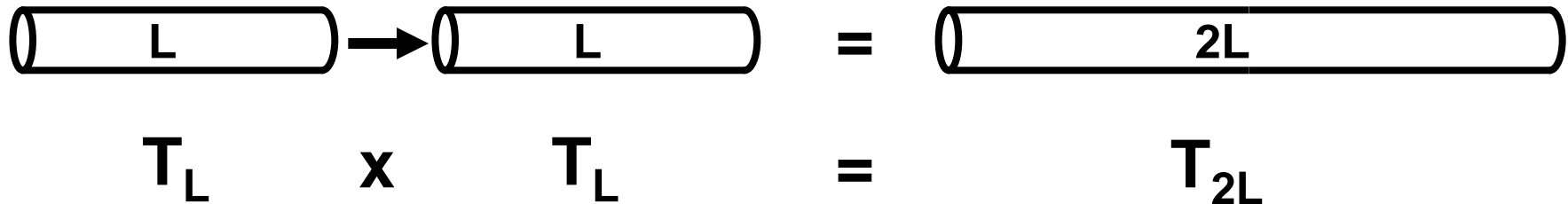
- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
- **De-embedding**
 - **Open-Short, Thru-Only method**
 - ➔ – **L-2L method**
- **Conclusion**

- A kind of multi-line de-embedding methods
 - The line lengths are L and $2L$.
 - Not need “Short” or “Thru (Short-Line)”
- De-embed transmission lines from the measurement data
 - Build a pad model
 - The pad model is used to de-embed the pad components from other TEG.

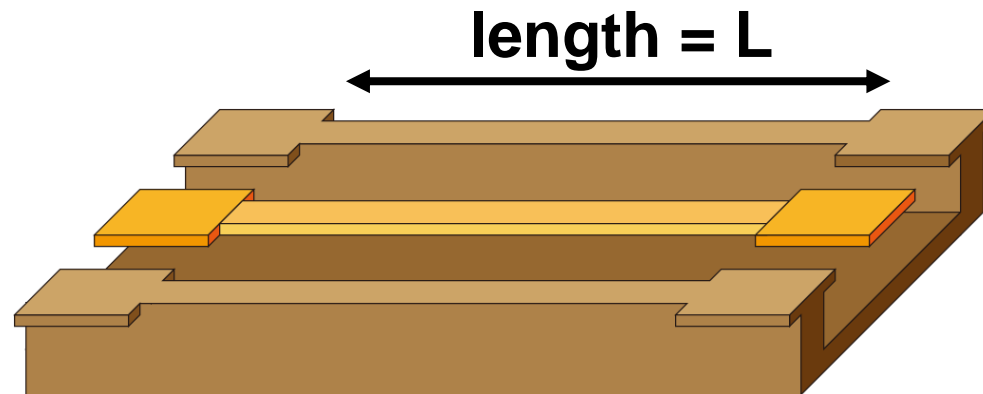


*J. Song, *et al.*, EPEP 2001

S \leftrightarrow **T** T-Parameters (Scattering transfer parameters)



- T-parameters can be calculated from S-parameters.
- Series connection of T-parameters can be calculated as a product of T-parameters.
- T-parameters are not reciprocal.



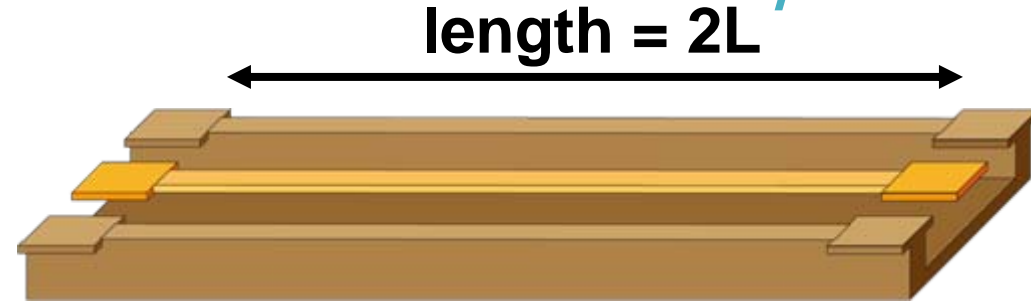
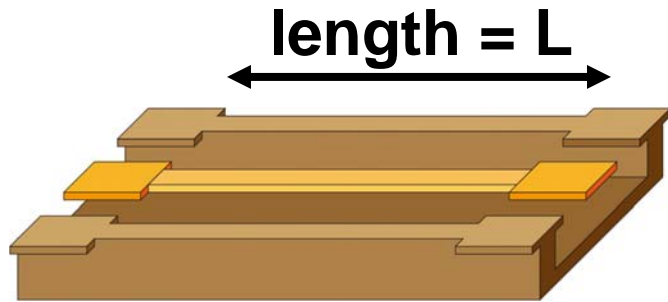
arbitrary

$$T_{L+PAD} = T_{LPAD} \times T_L \times T_{RPAD}$$

If we have T_{LPAD}^{-1} and T_{RPAD}^{-1} ,

$$\begin{aligned} T_{LPAD}^{-1} T_{L+PAD} T_{RPAD}^{-1} \\ &= T_{LPAD}^{-1} (T_{LPAD} T_L T_{RPAD}) T_{RPAD}^{-1} \\ &= T_L \end{aligned}$$

L-2L de-embedding method



$$T_{L+PAD} = T_{LPAD} T_L T_{RPAD}$$

$$T_{2L+PAD} = T_{LPAD} T_{2L} T_{RPAD}$$

$$(T_{2L} = T_L^2)$$

$$T_{L+PAD} T_{2L+PAD}^{-1} T_{L+PAD}$$

$$= (T_{LPAD} T_L T_{RPAD}) (T_{LPAD} T_L^2 T_{RPAD})^{-1} (T_{LPAD} T_L T_{RPAD})$$

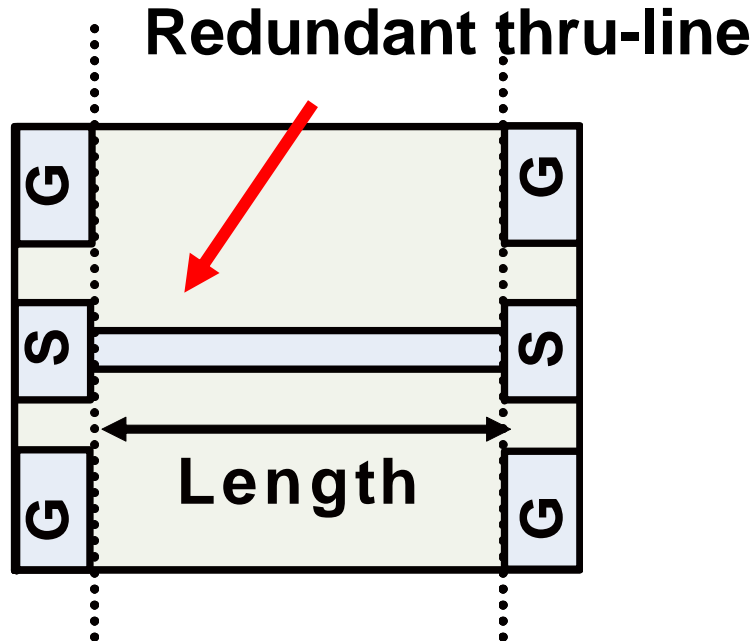
$$= T_{LPAD} T_L T_{RPAD} T_{RPAD}^{-1} T_L^{-2} T_{LPAD}^{-1} T_{LPAD} T_L T_{RPAD}$$

$$= T_{LPAD} T_L T_L^{-2} T_L T_{RPAD}$$

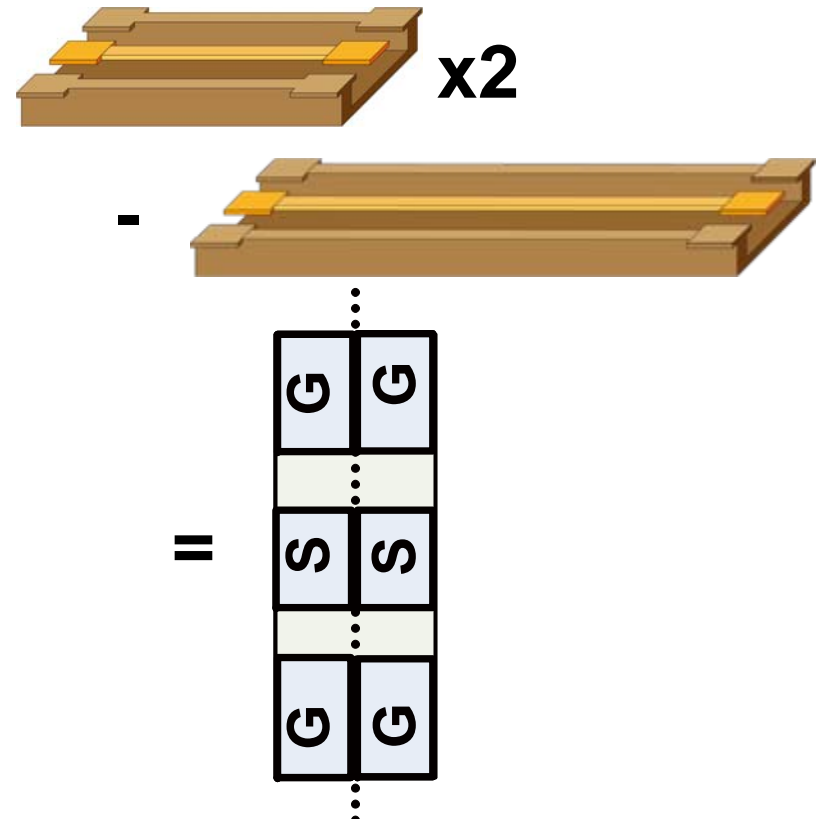
$$= T_{LPAD} T_{RPAD}$$

*J. Song, *et al.*, EPEP 2001

Thru-only method



L-2L method

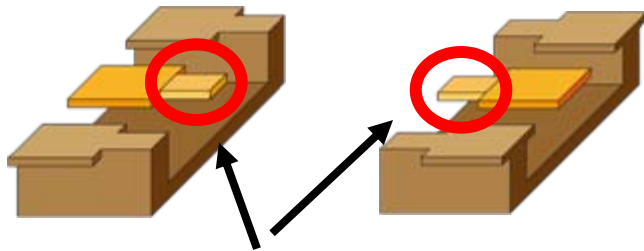


No redundant thru part

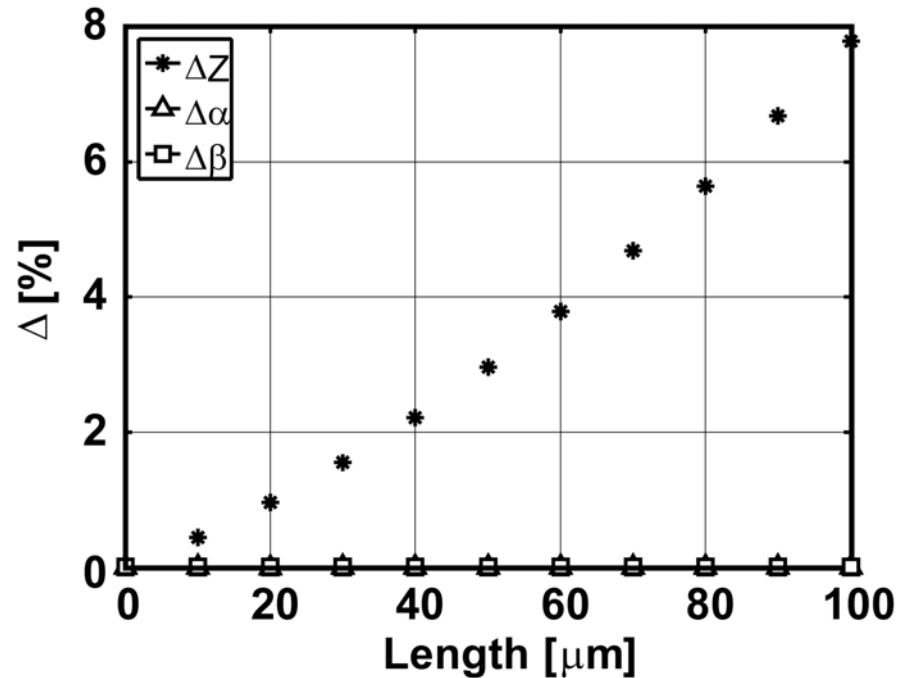
Redundant thru-line causes error at mmW frequencies.

Thru-only method

PAD model for Thru-only method



Redundant thru-line



Error items vs. thru-line length
@60GHz

Z_0 will have more than 2% error.

- CMOS 65nm process
- TL structure
 - Guided Micro Strip
 - $W = 10$ [μm], $H = 8$ [μm], $G = 15$ [μm]
 - Length of TLs : 200, 400 [μm]
- Pad structure
 - Signal pad : 40×60 [μm^2]

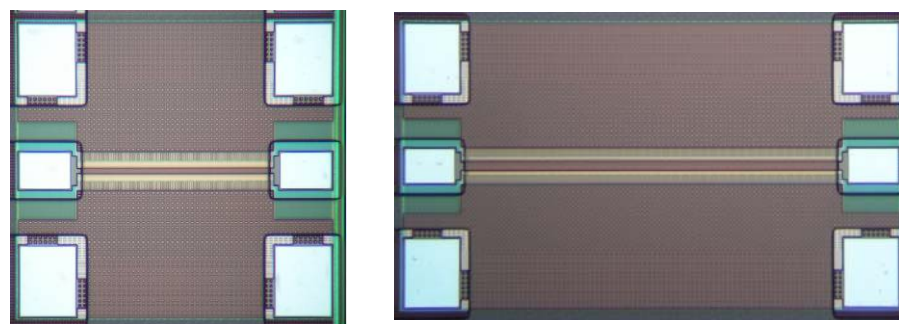
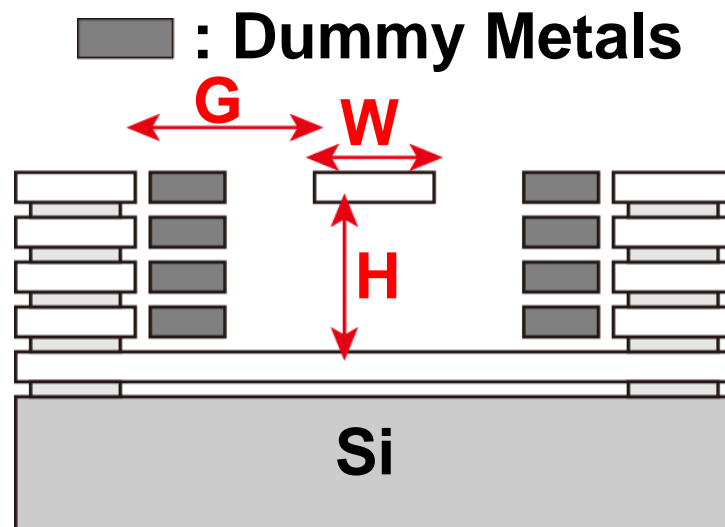


Photo of TLs



Structure of TL

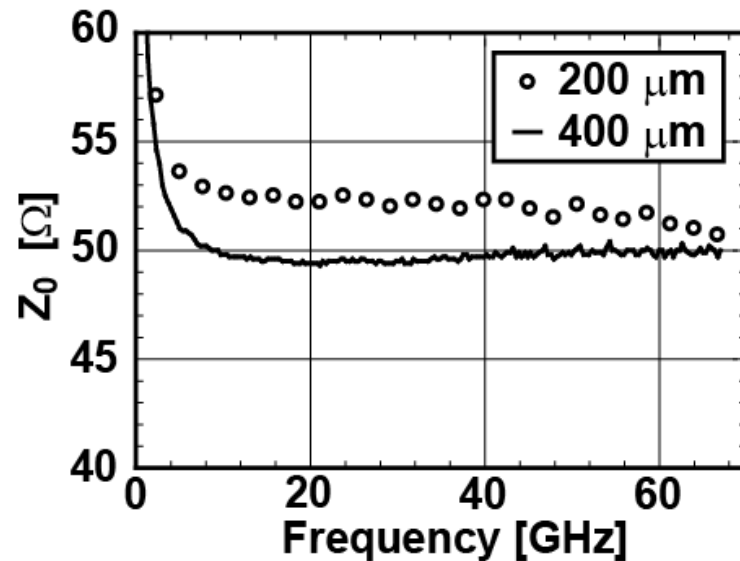
- Make pad models by each method
- De-embedding of different-length TLs
- Calculate Z_0 of TL from S-parameter
- Compare Z_0
 - Calculated from 200 μm -TL
 - Calculated from 400 μm -TL

$$Z_0^2 = Z_{\text{ref}}^2 \frac{(1 + S_{11})^2 - S_{21}^2}{(1 - S_{11})^2 - S_{21}^2}$$

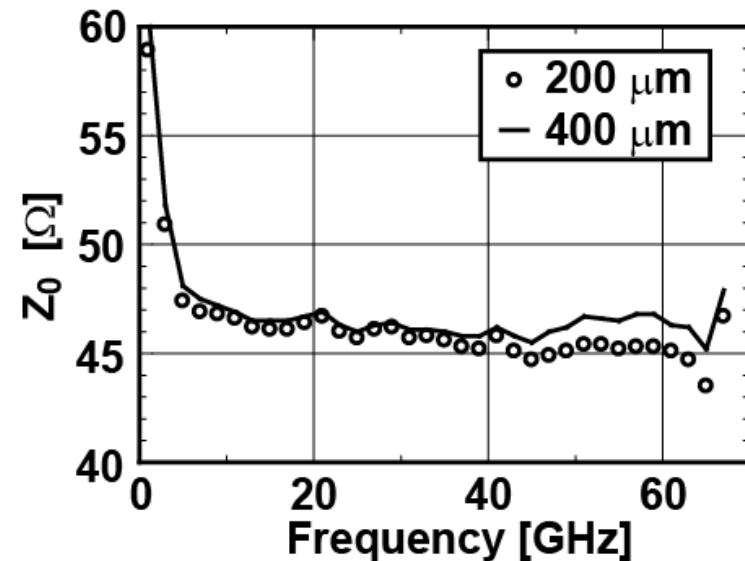
Z_0 : Characteristic Impedance
 Z_{ref} : Normalized Impedance

[1] W. R. Eisenstadt, *et.al.*, "S-parameter-Based IC Interconnect Transmission Line Characterization"

- Open-short method
 - Characteristic impedances of 200 μm and 400 μm do not agree with each other.
- Thru-only method
 - The results are unstable.

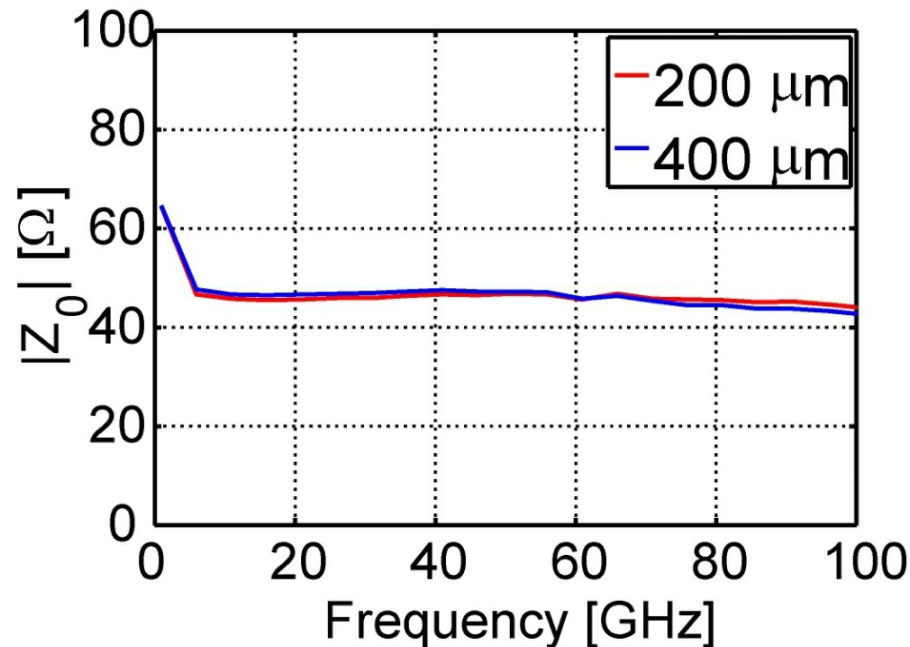


Open-short method



Thru-only method

- **Characteristic impedance of TLs**
 - The impedances of 200 μm and 400 μm agree with each other.
 - The results are stable.



Characteristic impedance

- **Lumped/Distributed de-embedding methods are reviewed.**
- **L-2L method performs very high accuracy at mmW frequency.**
- **The conventional Open-Short fails.**

- **Motivation**
- **Issues for mmW CMOS Circuits**
- **Device Characterization**
- **De-embedding**
- ➔ • **Conclusion**

- **This tutorial reviews mmW-frequency measurement and characterization of CMOS passive and active devices for designing mmW circuits.**
- **Tile-based design is required due to dummy metal and parasitic caps.**
- **Branch and bend are individually characterized.**
- **L-2L de-embedding method is practical at mmW frequency.**

Acknowledgement

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