超低エネルギーアナログ・RF回路技術と新規分野への展開

An ultra-low energy analog and RF circuit technology for emerging applications

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Dept. of Physical Electronics
Graduate School of Science and Engineering

2009/11/30

Matsuzawa & Okada Lab.

Lab. members

TOKYO TECH Pursuing Excellence

Founded in 2004

Professor: Akira Matsuzawa
Assoc. Prof.: Kenichi Okada (RF)
Assist. Prof.: Masaya Miyahara (ADC/DAC)
2 technical staff, 3 secretaries

14 doctor students (3 from corp.)
20 master students
6 undergraduate students
some researchers from corp. **≈50 people**

20 Japanese students and 20 foreign students

Focus of Laboratory

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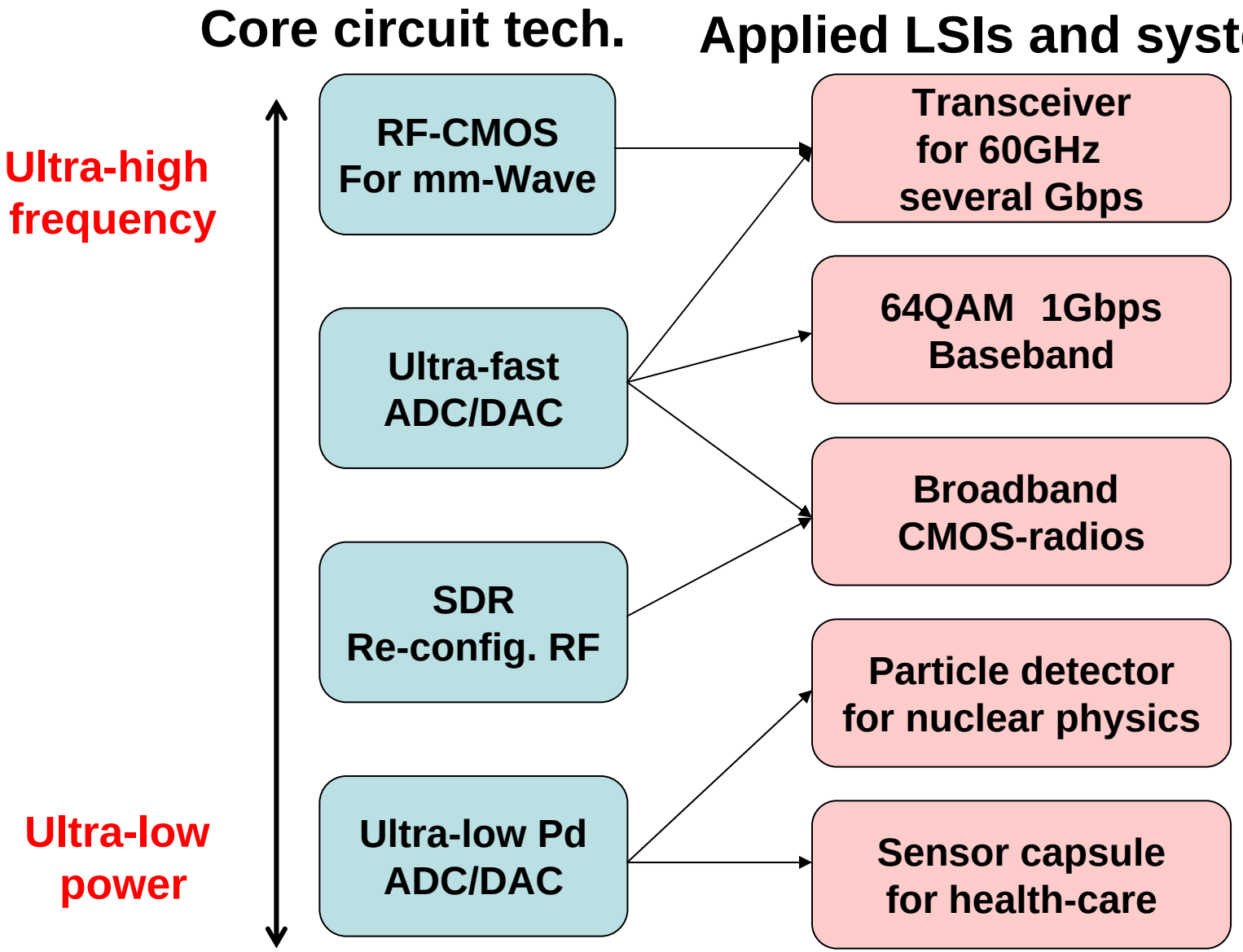

SoCs for mm-wave systems

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We now developing SoCs for mm-wave systems

1. **Long range: 4km Fixed point**
   : 38GHz, 0.6—1.0 Gbps

with JRC and NEC

図 2 東京工業大学大岡山キャンバスの航空写真

2. **Short range: a few meter**
   : 60GHz, 3-10 Gbps

with Sony

Provided by Sony

Long range mm-wave: Fixed point 38GHz,1Gbps

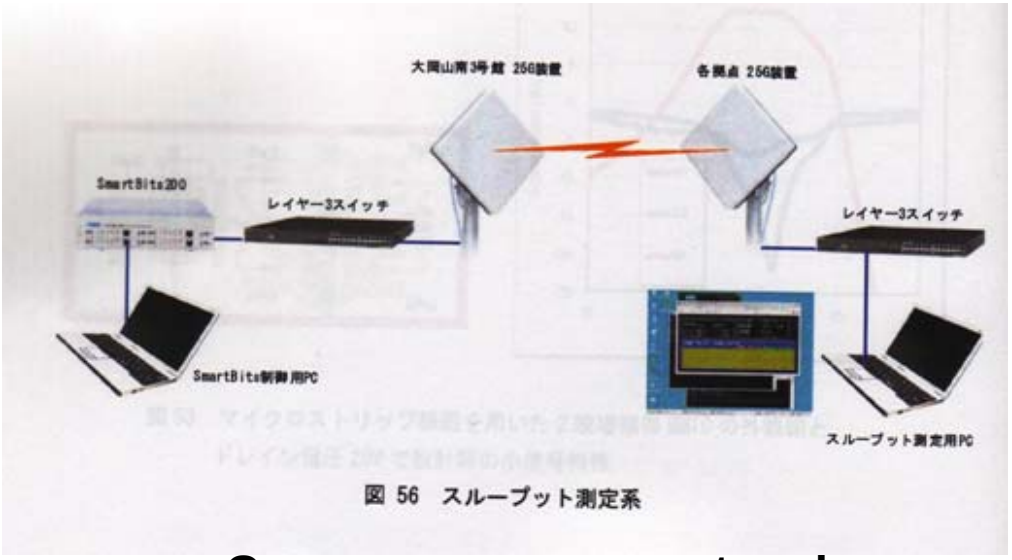
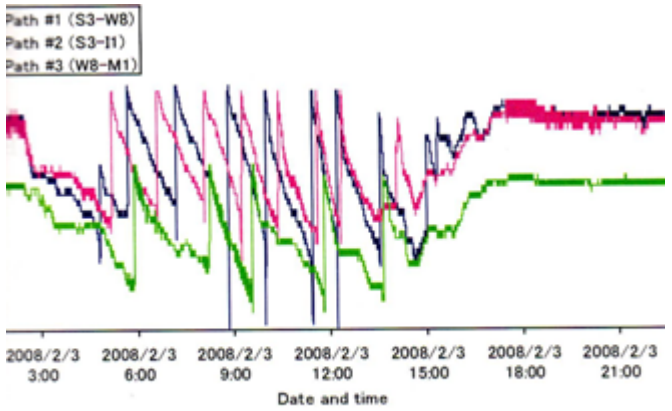


図 56　スループット測定系

Campus mm wave network

Equipment with plane Antenna

Networks durability against rain



(e) 2008 年 2 月 3 日（雪。3 センチほど積もる）

Developing 60GHz mm-wave circuits

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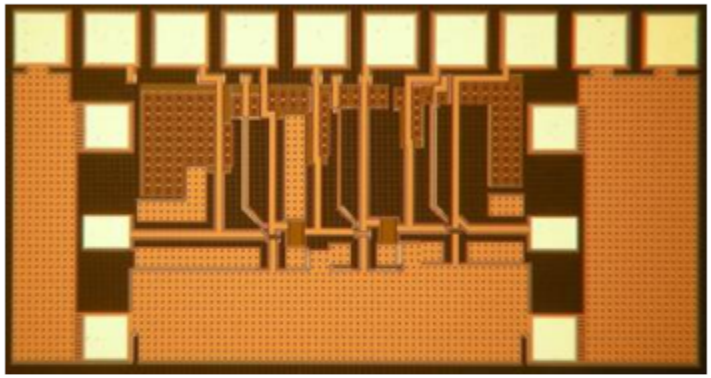
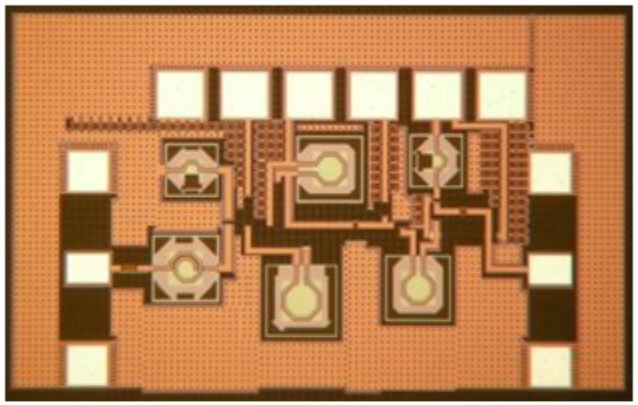
We now developing 60GHz CMOS Transceiver.

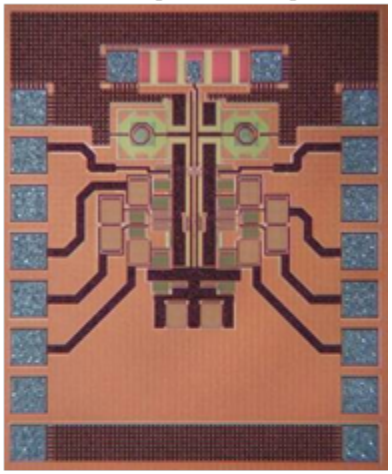
PA (90nm)



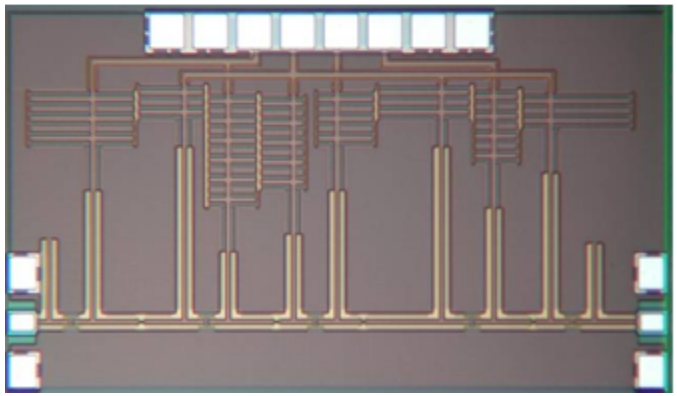
LNA (90nm)



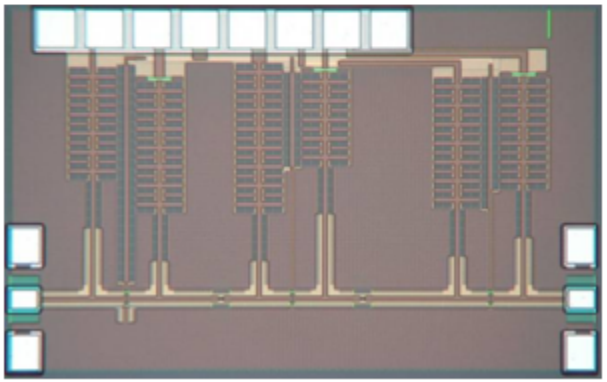
VCO (90nm)



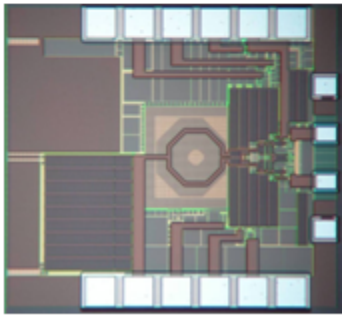
PA (65nm)



LNA (65nm)



VCO (65nm)



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An ultra-low energy analog and RF circuit technology for emerging applications

Matsuzawa & Okada Lab.

Flash ADC architecture

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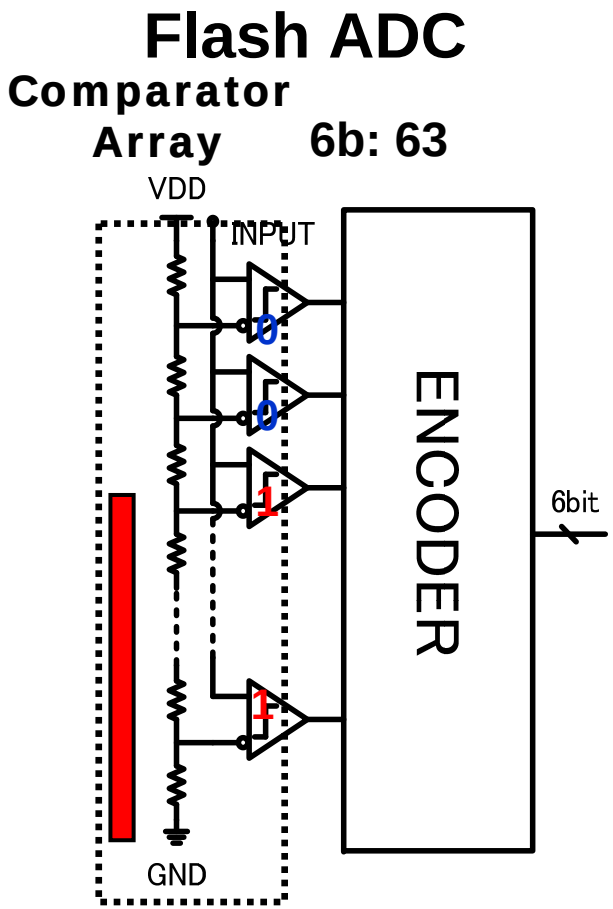
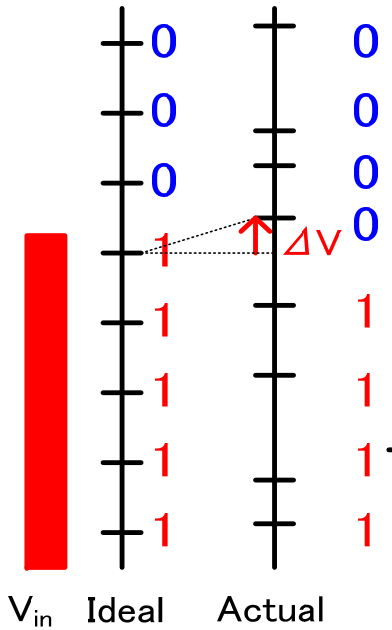
- Expecting highest speed
- Comparator determines the ADC performance

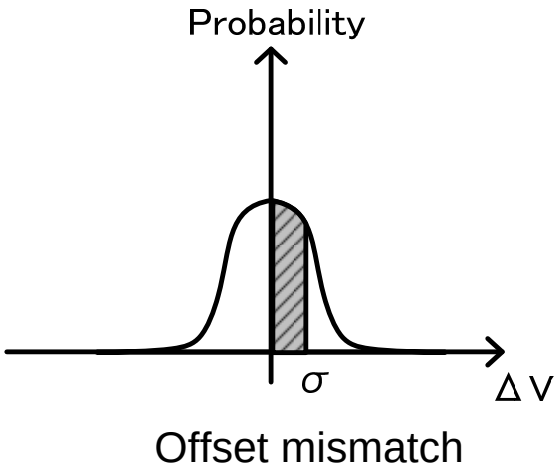
Low offset mismatch and noise are preferable



$$V_q = \frac{V_{FS}}{2^N}$$

V_q=16mV, Mismatch <3mV





Degradation of ENOB

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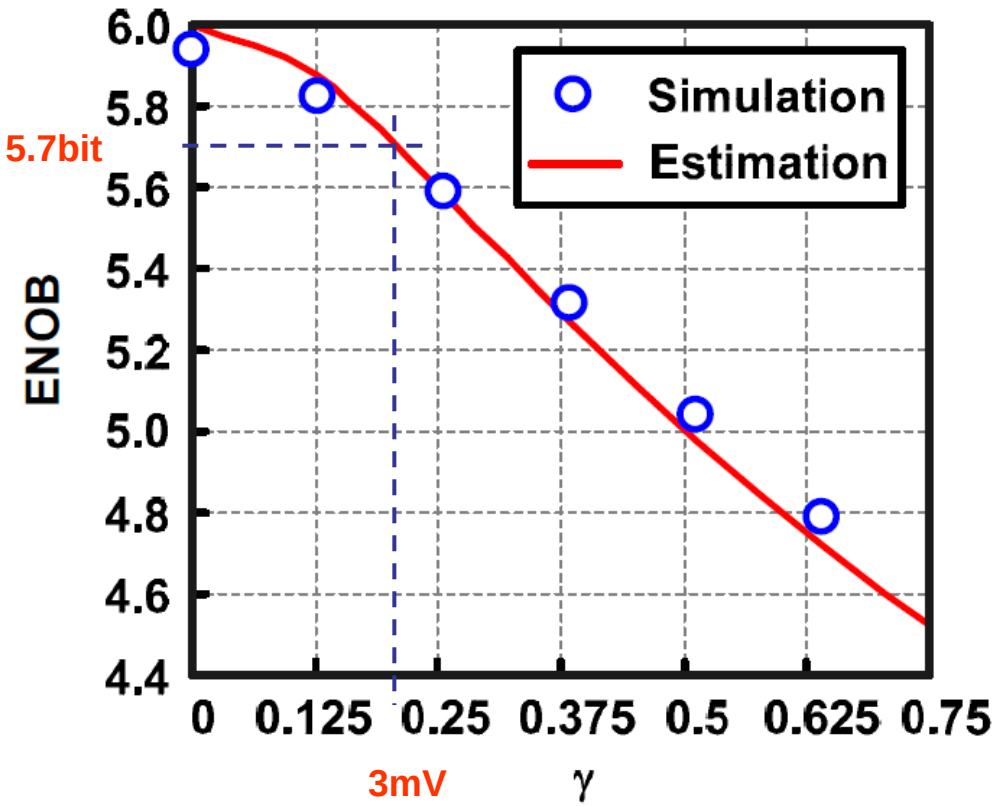
Degradation of ENOB in flash ADC is basically determined by offset mismatch and thermal noise of comparators.



For example; 6bit ADC, ENOB=5.7bit
V_q=16mV, V_{off}<3mV

$$\Delta ENOB = \frac{1}{2}\log_2\left(1+12\gamma^2\right)$$

$$\gamma^2 = \left(\frac{V_{off}(\sigma)}{V_q}\right)^2 + \left(\frac{V_n(\sigma)}{V_q}\right)^2$$

$V_{off}(\sigma)$: Distribution of offset

$V_n(\sigma)$: Distribution of noise

FoM of Flash ADC

FoM of flash ADC is determined by energy consumption of unit comparator and the degradation of effective bit.

Reduction of consumed energy and increase of ENOB are very important

$$FoM = \frac{P_d}{f_s \times 2^{ENOB}} \approx \frac{E_c \cdot f_s \cdot 2^N}{f_s \times 2^{N-\Delta ENOB}} = E_c \cdot 2^{\Delta ENOB}$$

E_c: Energy/Comparator

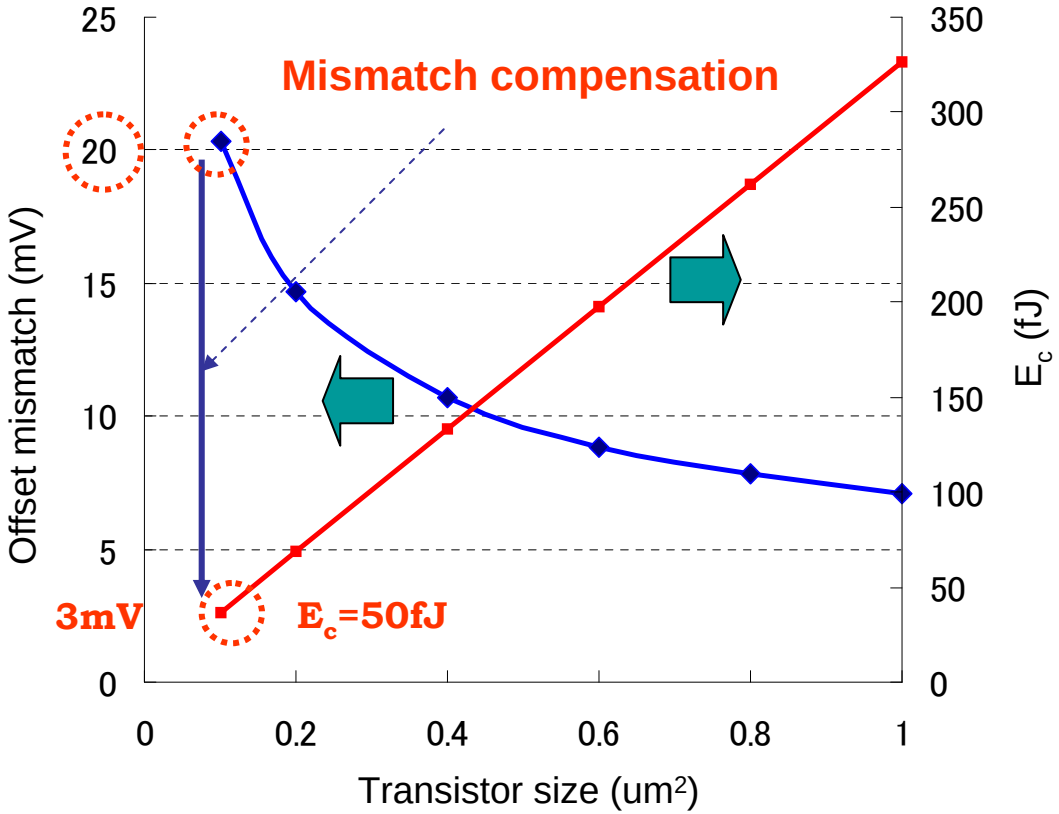
$$E_c = CV_{DD}^2$$

E_c is basically proportional to the capacitance

Tradeoff: mismatch and energy consumption

There is a serious tradeoff between mismatch of transistor and gate area.

Larger transistor is required to reduce mismatch voltage and results in increase of gate area and consumed power.



Example

6bit ADC: V_{off}<3mV
E_C<50fJ→0.1um²→V_{off}=20mV
Needs mismatch compensation
20mV →3mV

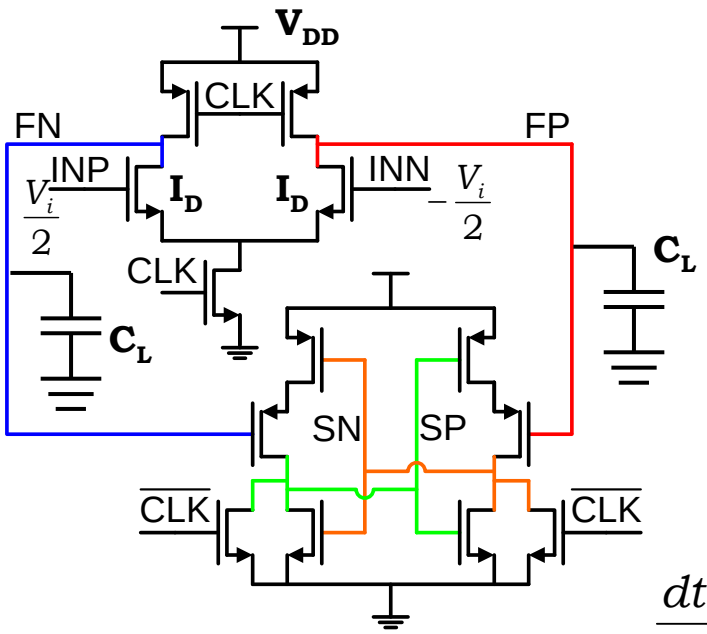
$$V_{offset}(\sigma) \propto \frac{1}{\sqrt{LW}}$$

$$E_c \propto C_c \propto LW$$

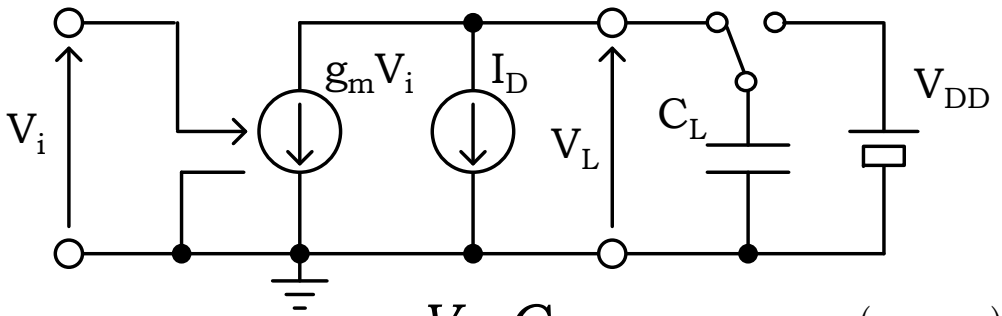
$$E_c \propto \frac{1}{V_{offset}^2(\sigma)}$$

Mismatch compensation of dynamic comparator

The mismatch can be compensated by capacitance and current.



Equivalent circuit of the first stage.

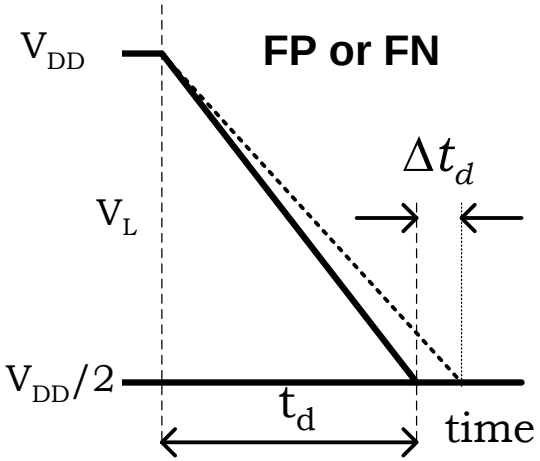


Delay time $t_d = \dfrac{V_{DD} C_L}{2 I_D}$

$I_D \propto (V_{gs} - V_T)^{\alpha} = V_{eff}^{\alpha}$

$g_m = \dfrac{dI_D}{V_{eff}} = \alpha \dfrac{I_D}{V_{eff}}$

$$\frac{dt_d}{dV_i} = \frac{dt_d}{dI_D} \cdot \frac{dI_D}{dV_i} = -\frac{V_{DD} C_L}{2 I_D} \frac{g_m}{I_D} = -t_d \frac{\alpha}{V_{eff}} \qquad \therefore \frac{g_m}{I_D} = \frac{\alpha}{V_{eff}}$$



$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}} \qquad \frac{\Delta t_d}{t_d} = \left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D} \right)$$

$$\therefore \frac{\Delta t_d}{t_d} = \alpha \frac{\Delta V_i}{V_{eff}}$$

$$\Delta V_i = \frac{V_{eff}}{\alpha} \left(\frac{\Delta C_L}{C_L} - \frac{\Delta I_D}{I_D} \right)$$

Digital calibration method

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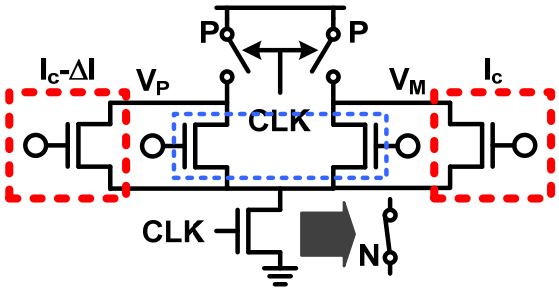
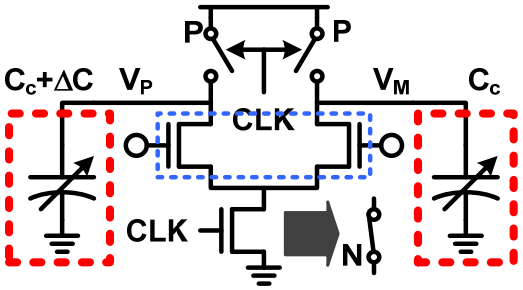
Resistor ladder type

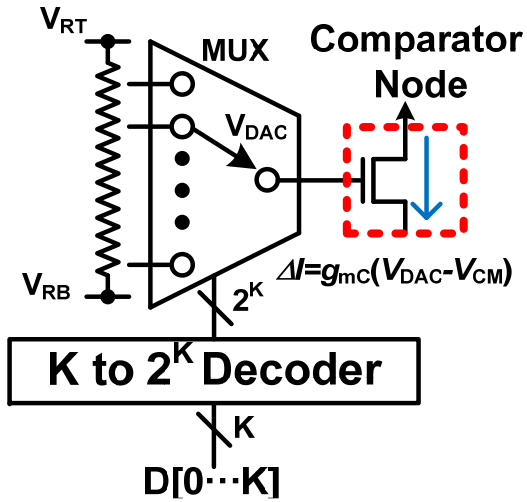


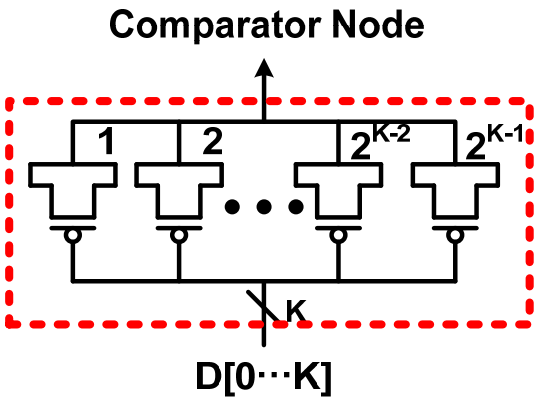
Current calibration

Capacitor array type



Capacitance calibration

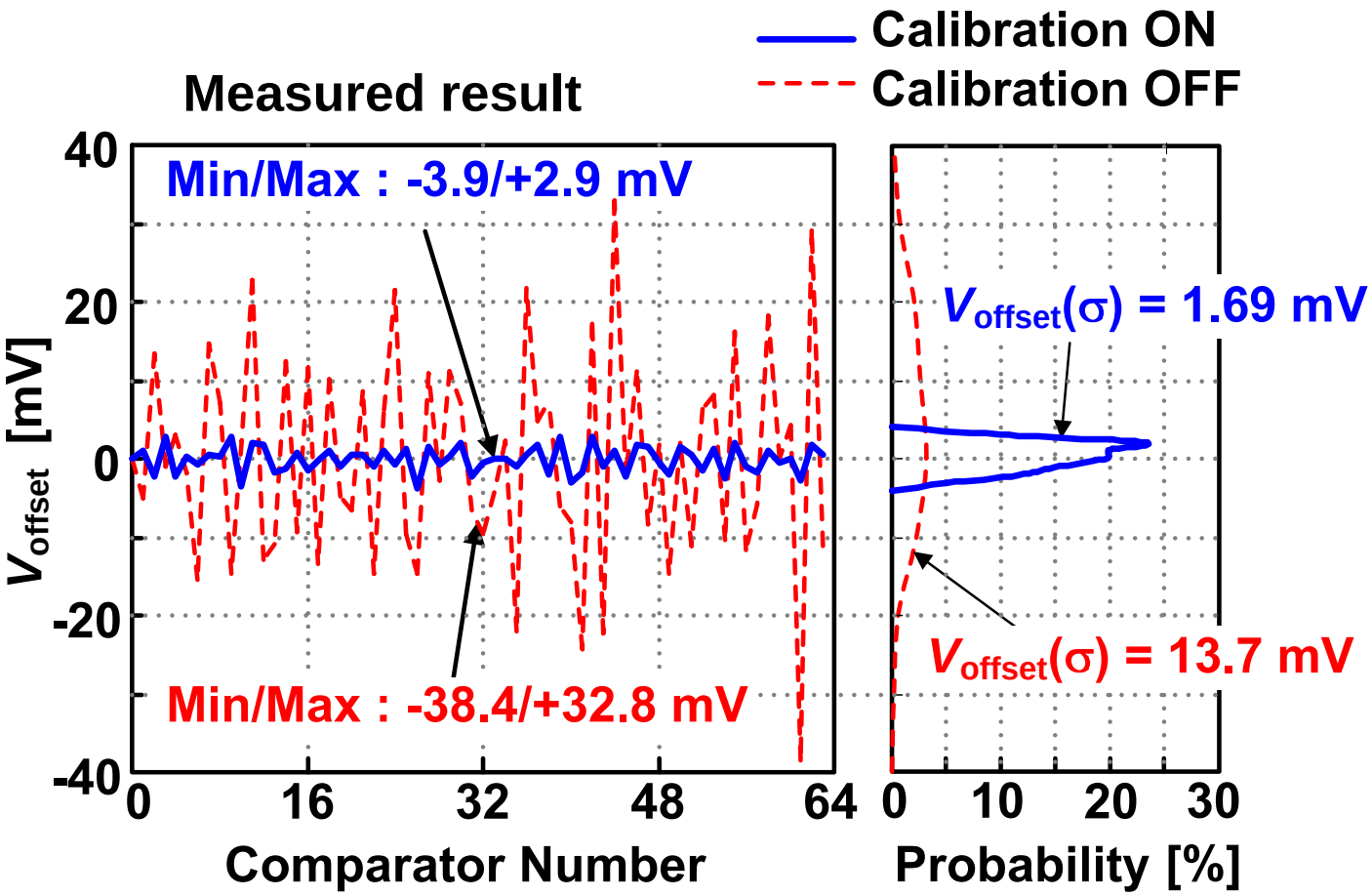




Binary weighted capacitor array

Effect of analog mismatch compensation

We can reduce the mismatch voltage form 14mV to 1.7mV at sigma.



M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Match with noise simulation

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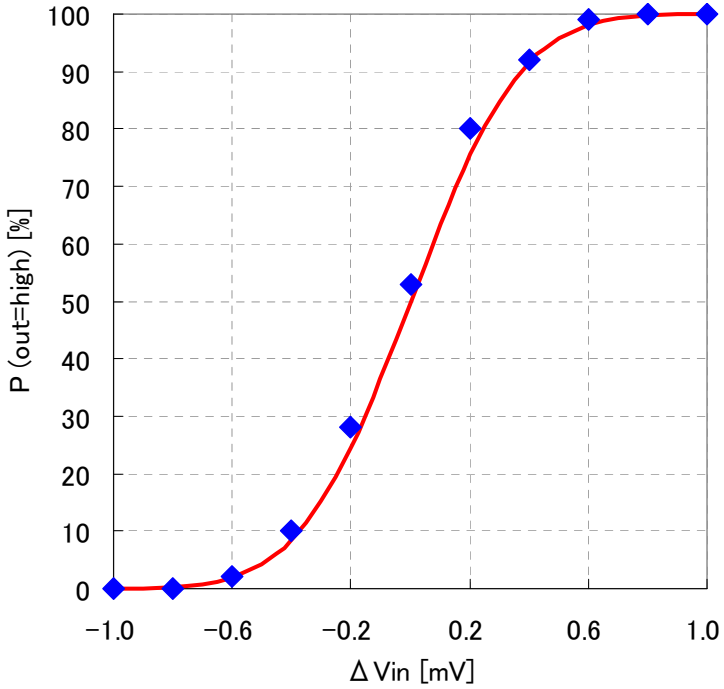
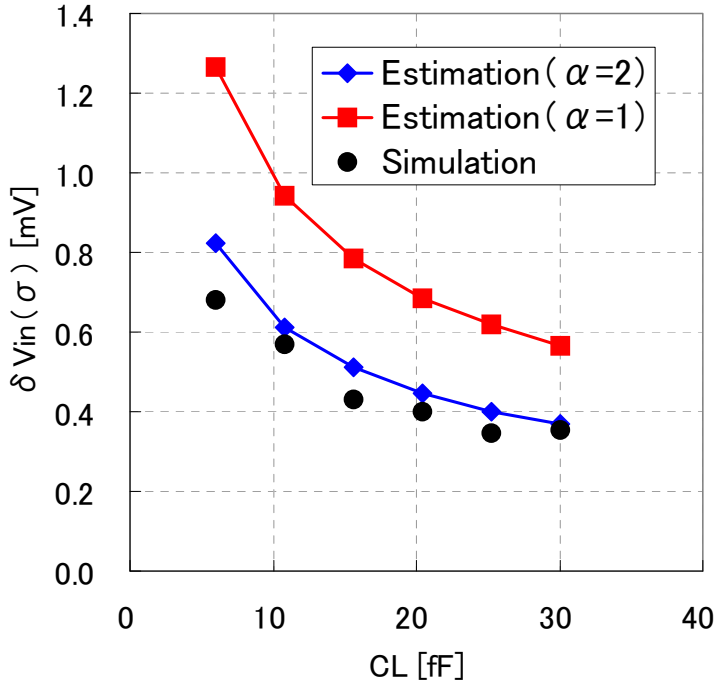
The deduced equation has a good match with simulation.

$$\delta V_{in} \approx 2\sqrt{\frac{kTV_{eff}}{\alpha C_L V_{DD}}}$$

We deduced this noise equation

Noise in comparator





Comparison of comparators

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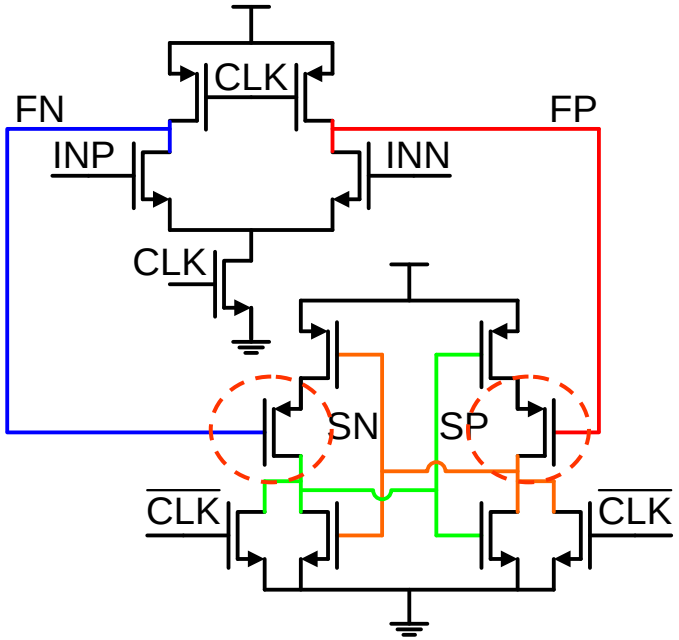
Double clock

NMOS Single gm

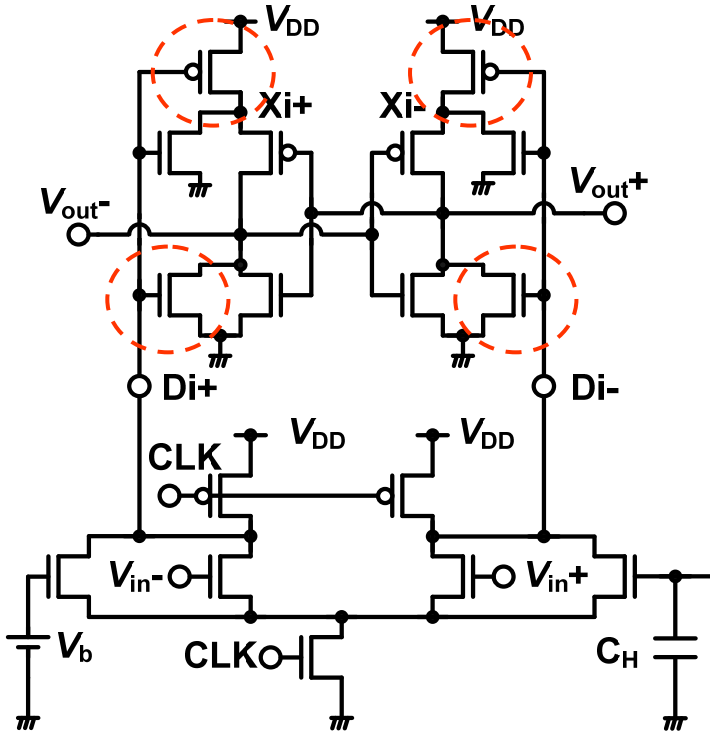


Conventional

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, “A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC,” IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Single clock

NMOS+PMOS Double gm



Our proposed

M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.

Noise reduction of comparator

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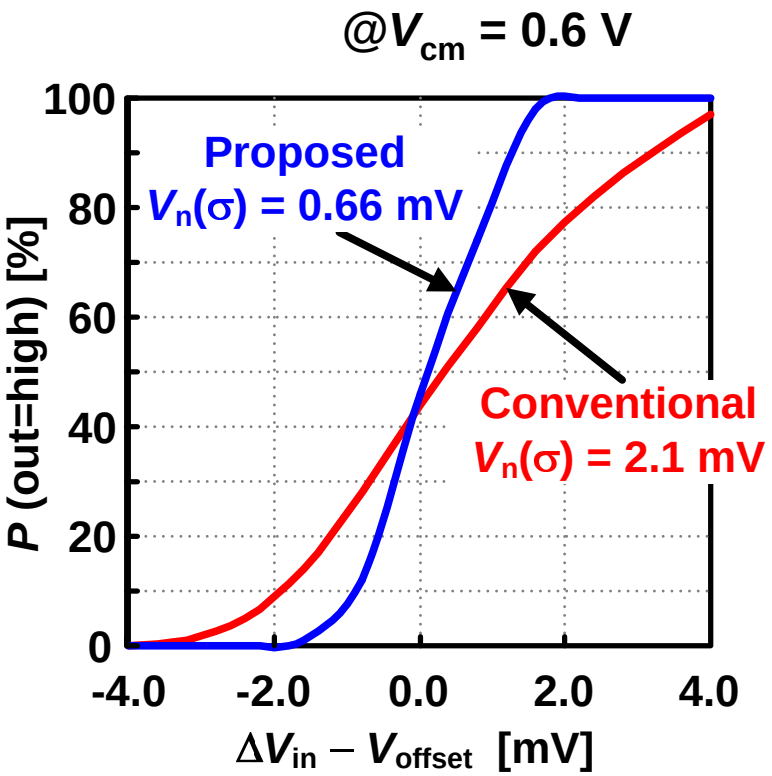
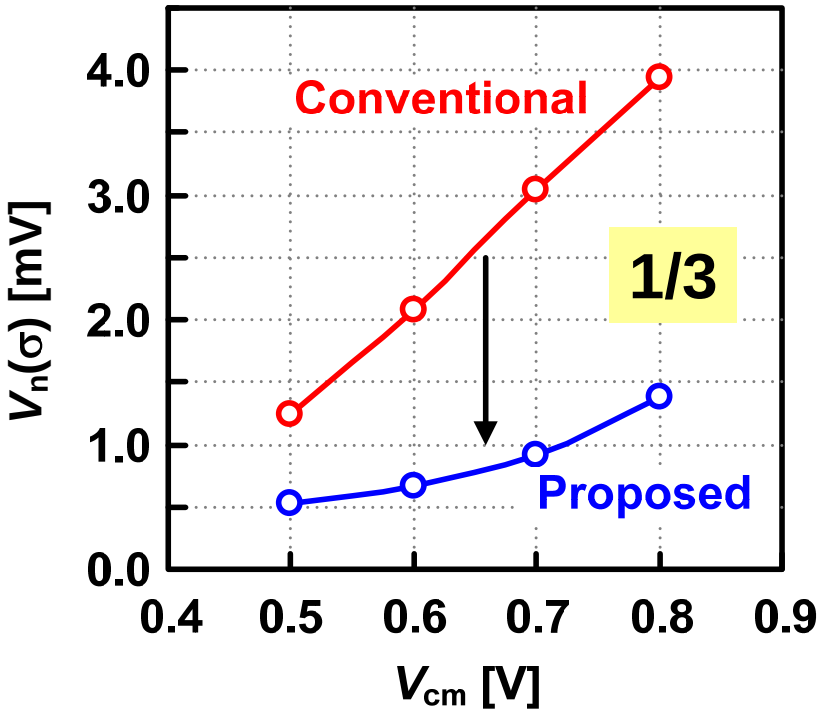
Proposed double-tail latch comparator can reduce noise down to 1/3.

V_{DD} = 1.0 V, *F*c = 4 GHz, Transient-Noise simulations.
(Offset calibration is not used.)

M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A Low-Noise Self-Calibrating Dynamic Comparator for High-Speed ADCs," A-SSCC, Nov. 2008.





6bit, 7mW, 250fJ, 700MS/s Sub-ranging ADC

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Compensation of offset variation with good efficiency

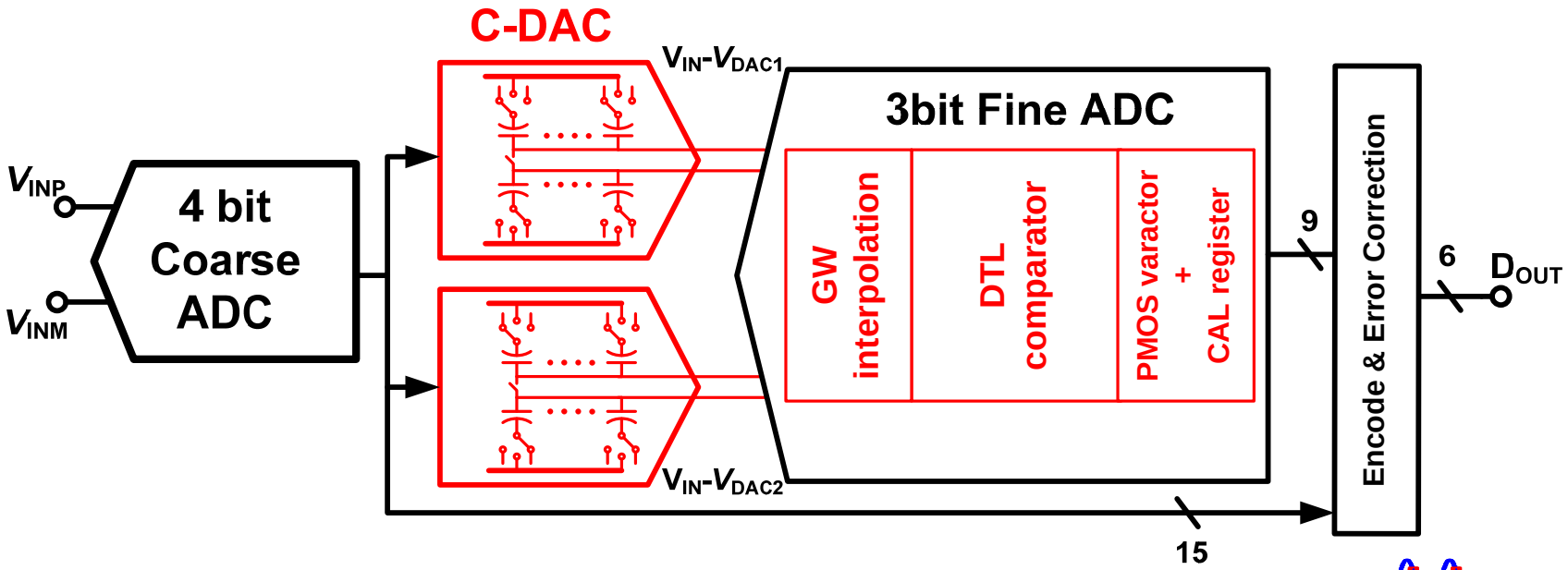
- **A1. Double-tail latched comparator**
- **A2. Digital calibration by capacitance adjusting**

Reference voltage generation of sub-range

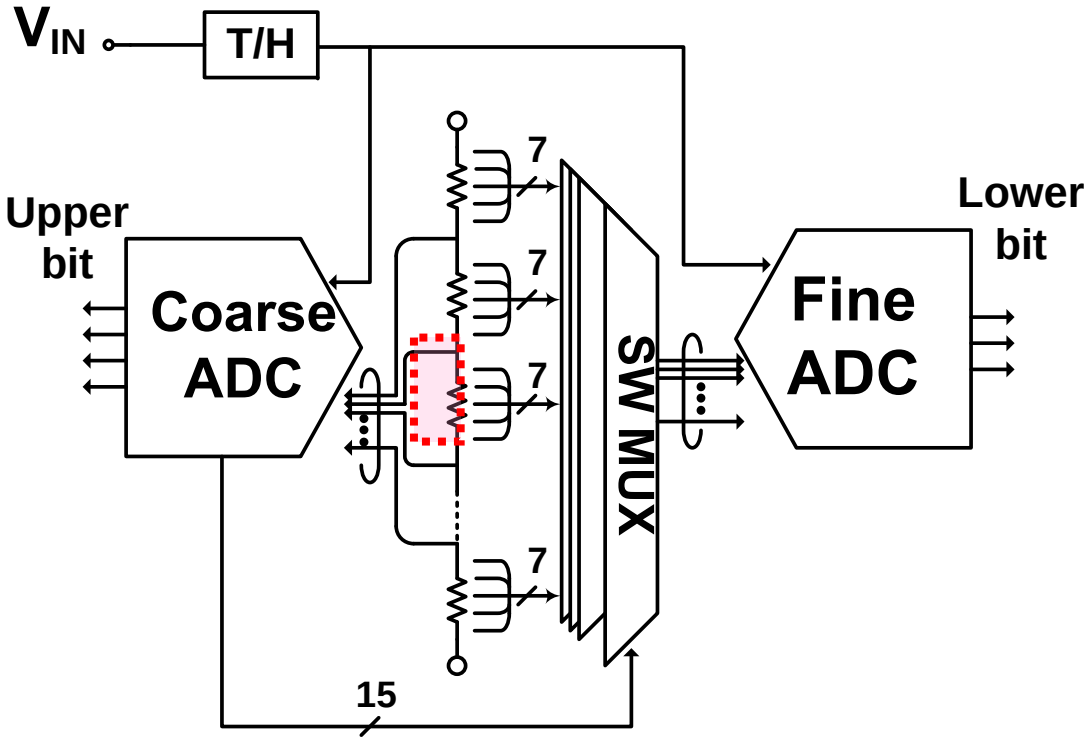
- **B1. Capacitive DAC (C-DAC)**
- **B2. Gate-weighted interpolation**

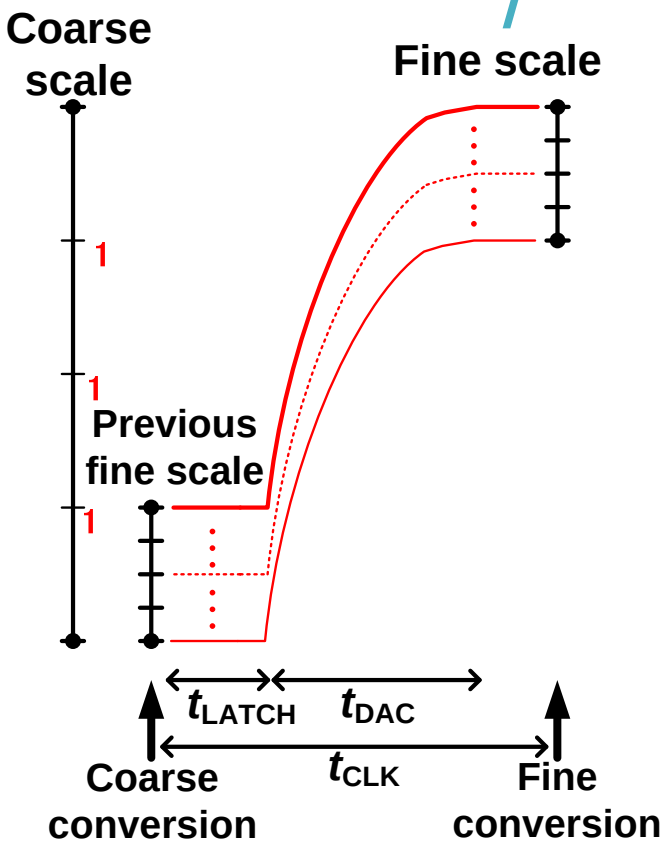
Y. Asada, K. Yoshihara,T. Urano, M. Miyahara and A. Matsuzawa, "A 6bit, 7mW, 250fJ, 700MS/s Subranging ADC" A-SSCC, pp. 141-144, Nov. 2009.

➔Proposed circuits consume no static power.



Issue of reference voltage generation





Resistor ladder + SW MUX:

- **Static power consumption** in resistor ladder
- Trade-off between **settling time** and **power consumption**
- **Many SW** for fine reference

➔ **Power consumption is inevitable with high speed operation.**

C-DAC

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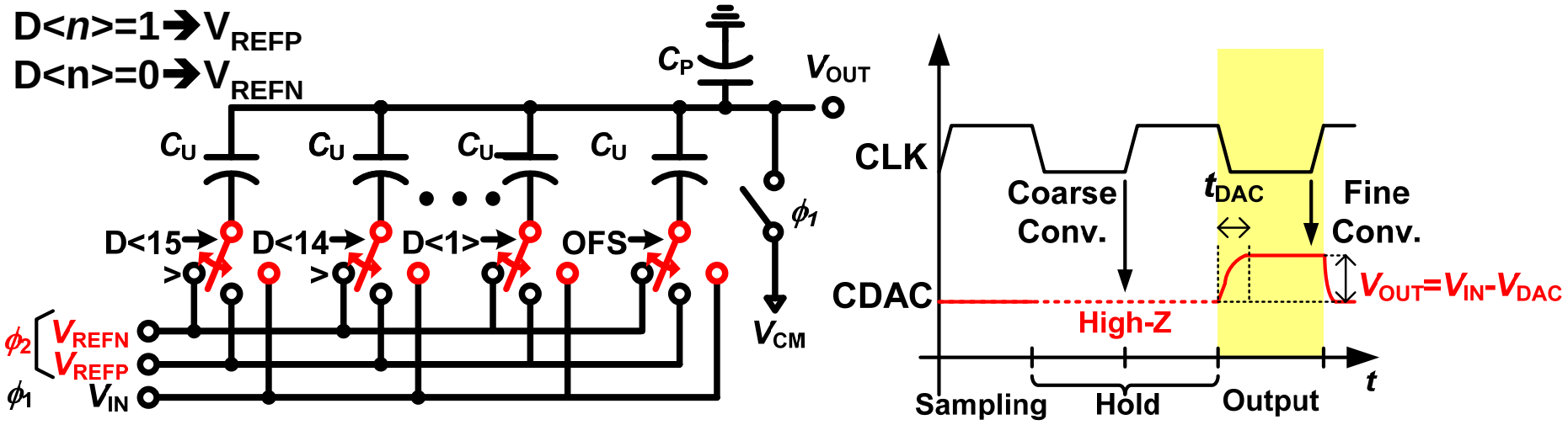
CAD can realize fast operation with low Pd



Advantage :

- Operating as **S/H circuit**
- **No static power consumption** (360μW@1GHz)
- Smaller C_u realize **faster settling time**

(t_{DAC}= 3.4 $r_{on}C_U$ < 80ps @ r_{ON} = 1kΩ, C_U= 15fF)

Interpolation comparator

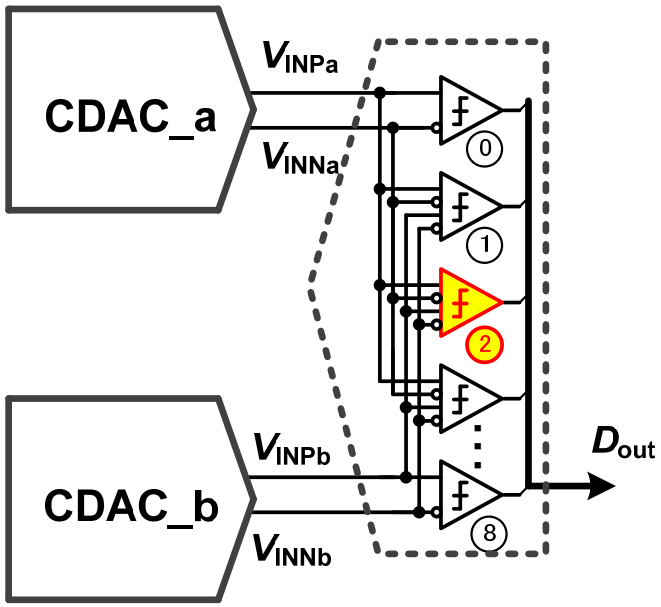
Interpolation can match upper and lower conversion ranges self-consistently.

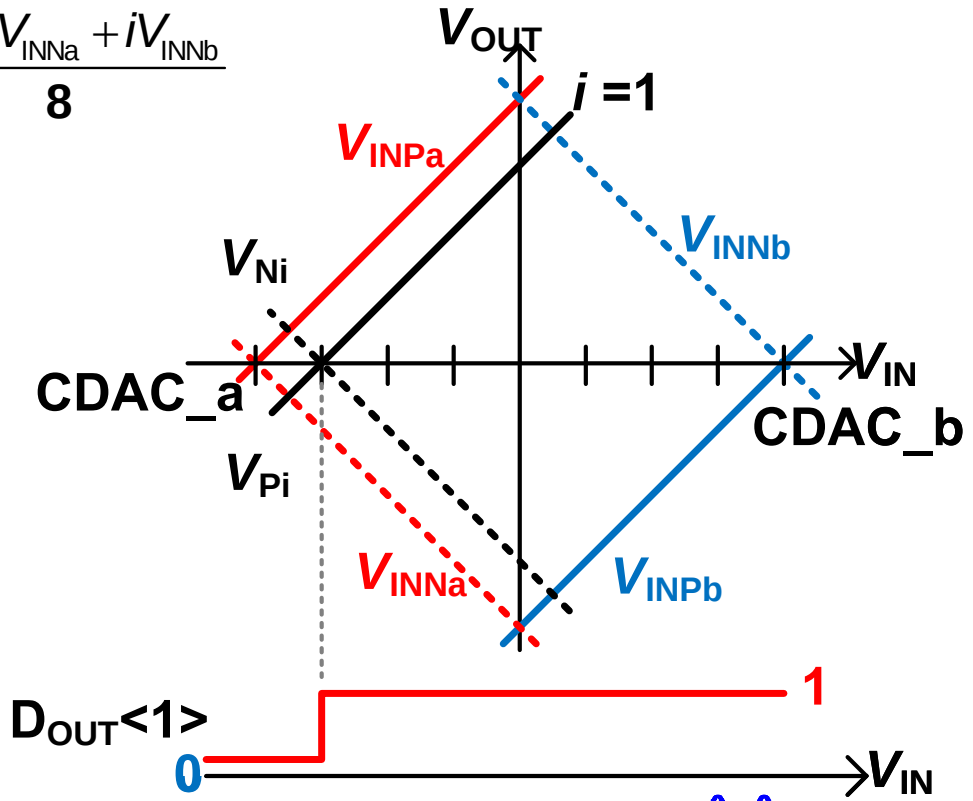
FADC composed of interpolation comparator

Threshold voltage of *i* th comparator is the cross-point of V_{Pi}, V_{Ni}.

V_{Pi}, V_{Ni} : interpolated signal of CDAC outputs.

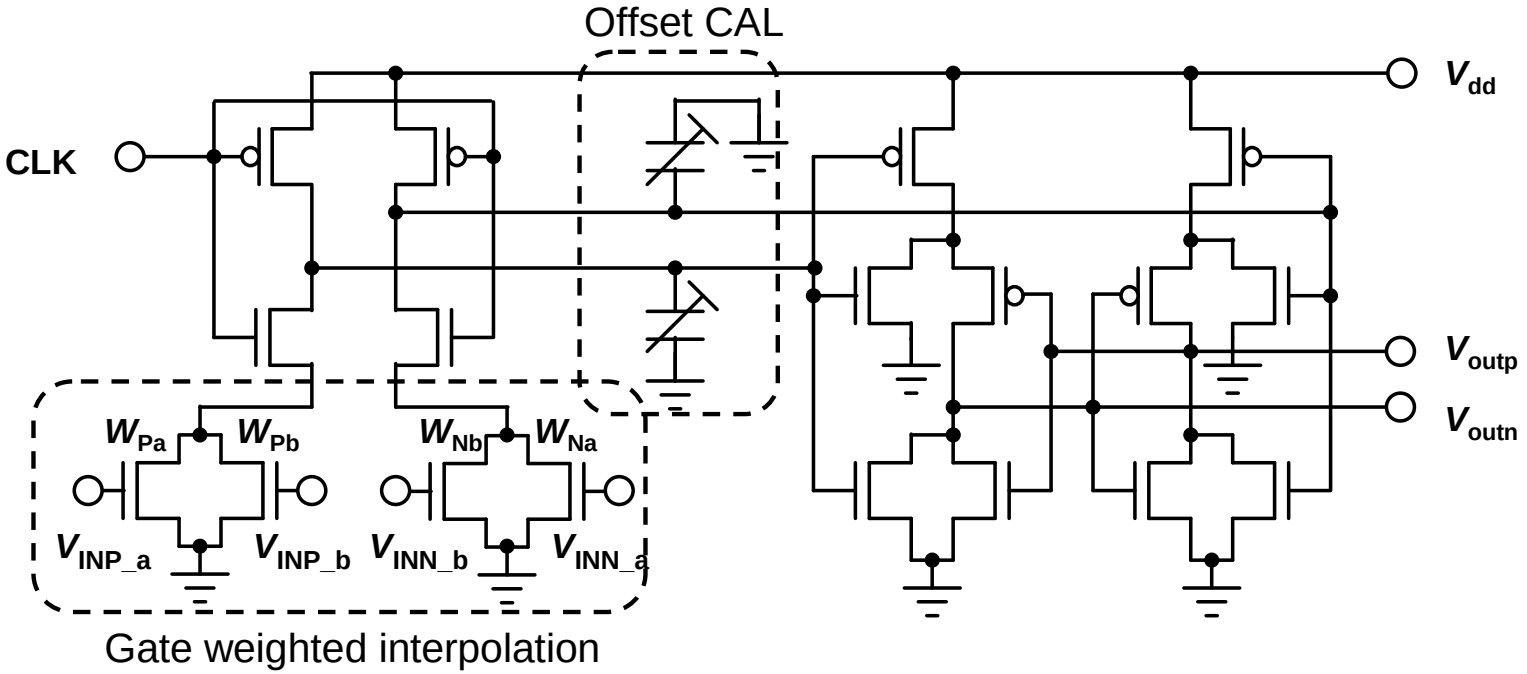
$$V_{Pi} = \frac{(8-i)V_{INPa} + iV_{INPb}}{8}, V_{Ni} = \frac{(8-i)V_{INNa} + iV_{INNb}}{8}$$

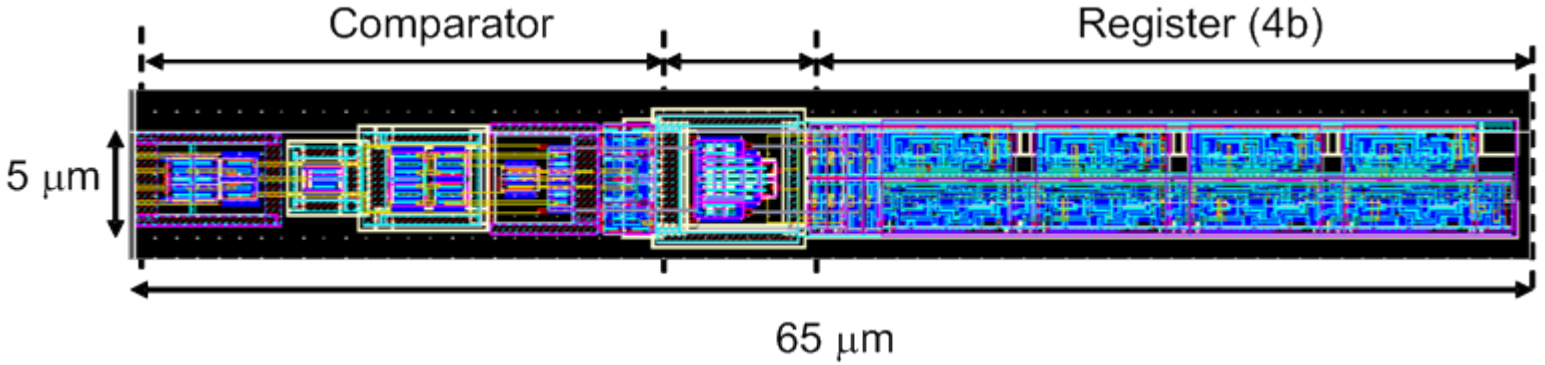




Comparator Circuits

Comparator with offset CAL realizes small area and high accuracy.





Chip photo & Layout

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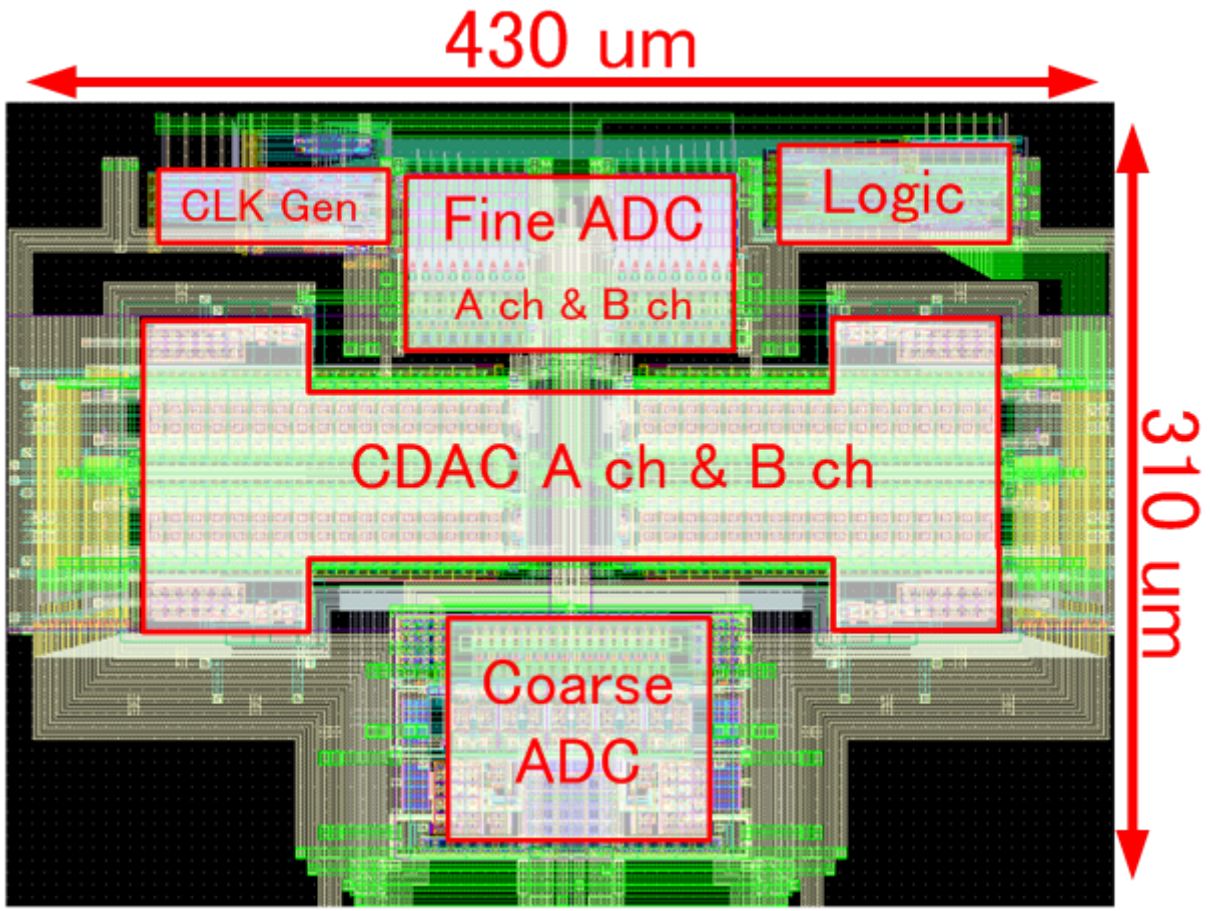
6 bit ADC has been realized in a 90 nm 10M1P CMOS technology with a chip area of 0.13mm^2



Performance Summary

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World lowest FoM ADC!!

Proposed circuits has realized the best power efficiency.

	[1]	[2]	[3]	[4]	[6]	This Work
Resolution(bit)	6	6	6	6	6	6
fs(GS/s)	0.8	1.2	0.7	1.25	1	0.7
SNDR(DC/Nyq.)	35/32	34/33	31/30	34/28	35/33	35/34
Pd (mW)	12	75	24	32	30	7
Active area(mm	0.13	0.43	0.052	0.09	0.18	0.13
VDD(V)	1.2	1.2	1.2	1.2	1.2/1.0	1.2
FoM(pJ)	0.44	2.17	1.31	1.22	0.8	0.25
CMOS Tech.(nr	65	130	130	130	90	90
Architecture	Flash	Flash	Pipeline	2b-SAR	Subrange	Subrange

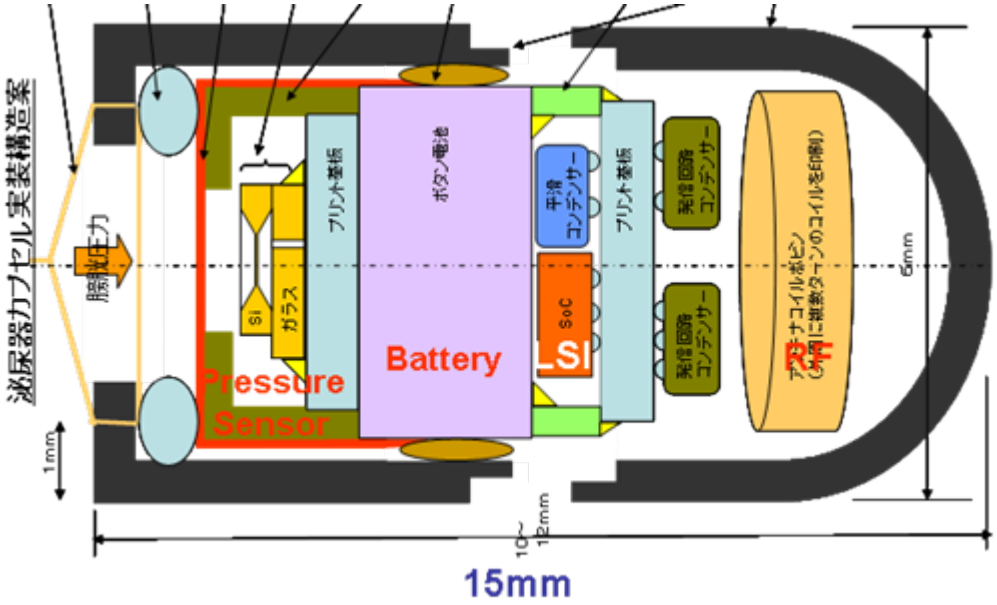
[1] C-Y. Chen, VLSI Circuits 2008.
[2] B-W. Chen, A-SSCC 2008.
[3] F. C. Hsieh, A-SSCC 2008.
[4] Z. Cao, ISSCC 2008.
[6] Y. C. Lien, A-SSCC 2008.

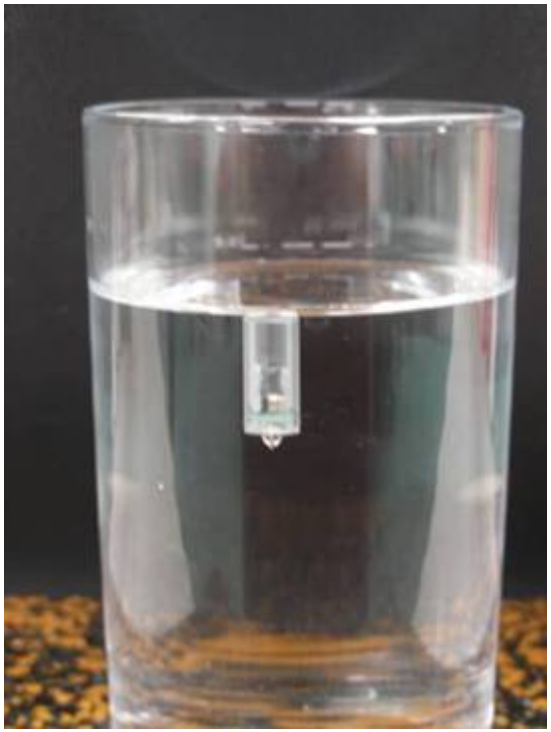
Circuit technology for emerging applications

- **Micro medical systems**
  - **Ultra-low power Capacitance to Digital converter**
  - **Can be applied to micro-sensor networks**
    - **Tire pressure sensor**
- **Nuclear particle detector**
  - **Pixels has an A/D converter in each**
  - **Can be applied to medical imaging devices**
- **Full digital DC/DC converter**
  - **Low power and high speed and resolution ADC**
  - **Every power supply systems**
  - **On-chip power supply**

Capsule to measure bladder pressure

Measure the bladder pressure and send the data in short range (15 cm)





Due to battery life

4 days with total current of 100uA

All analog and RF circuits consumes only 30uA

SAR Capacitance to Digital Converter

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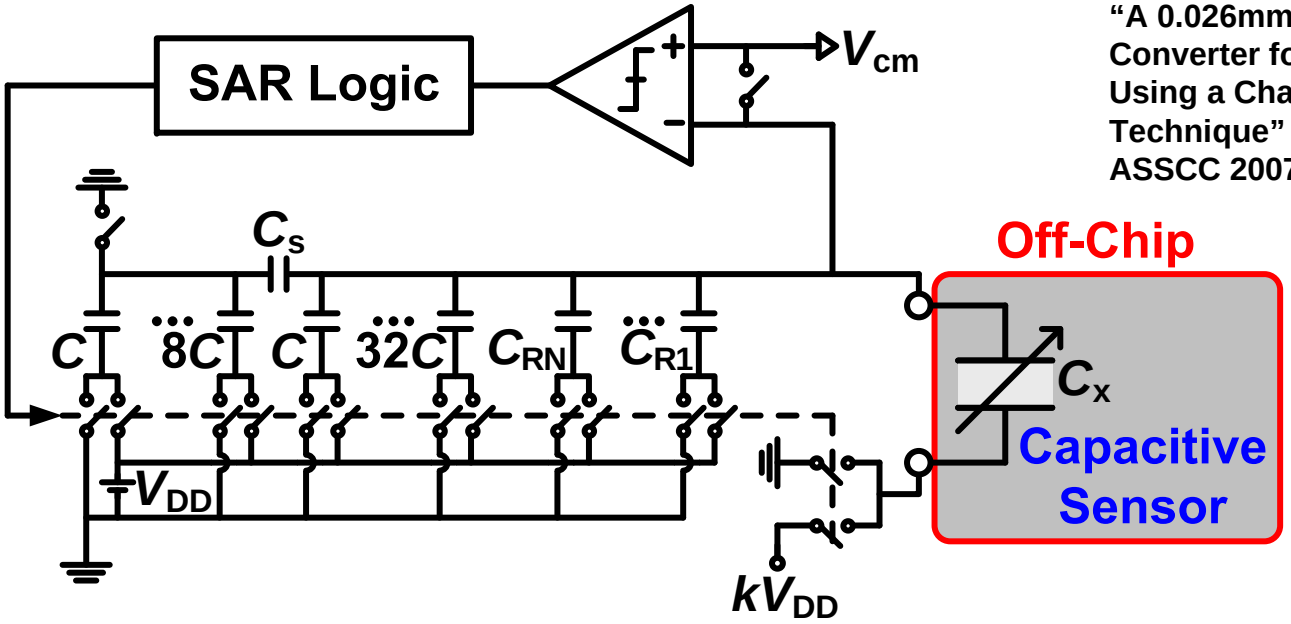
SAR ADC + Capacitive pressure sensor

- Low power
- Can compensate the offset capacitance
- Small area
- Insensitive to operating voltage

Kota Tanaka, Yasuhide Kuramochi, Takashi Kurashina, Kenichi Okada, and Akira Matsuzawa

"A 0.026mm2 Capacitance-to-Digital Converter for Biotelemetry Applications Using a Charge Redistribution Technique"
ASSCC 2007



Ultra-low power CDC

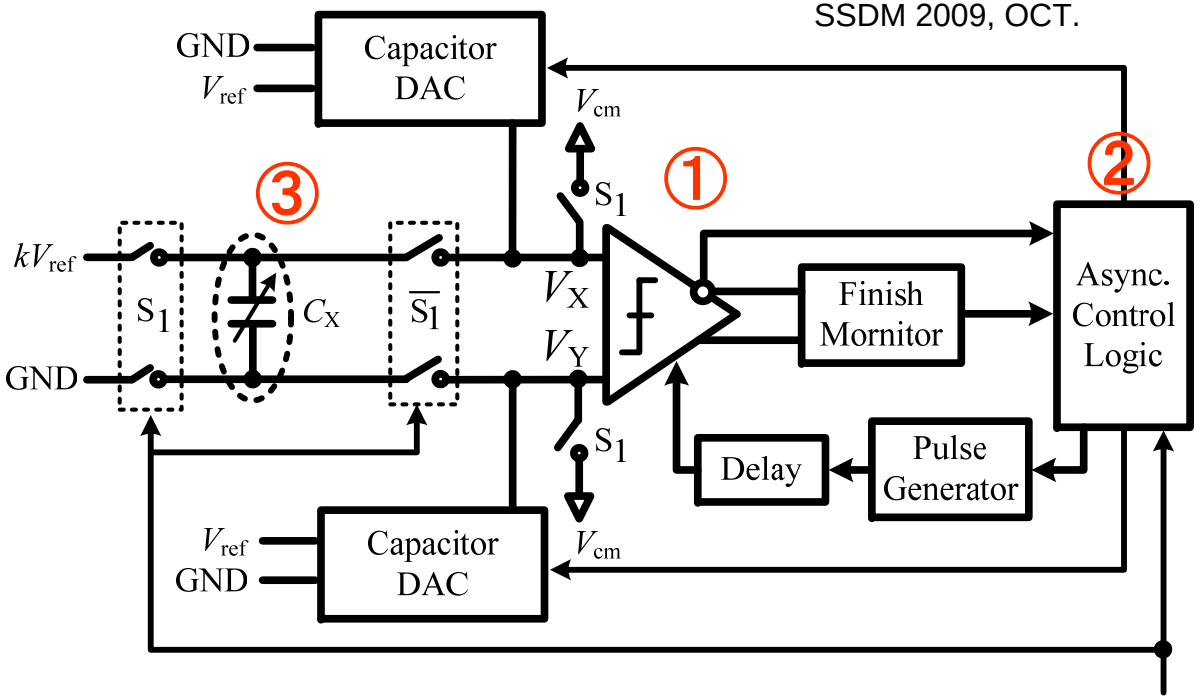
TOKYO TECH Pursuing Excellence

Improved Capacitance to Digital Converter.

1. 10b SAR like architecture
2. Self-clocking
3. Single to differential

3nA @ 30 times/sec

Tuan Minh Vo,Yasuhide Kuramochi, Masaya Miyahara,Takashi Kurashina, and Akira Matsuzawa "A 10-bit, 290 fJ/conv. Steps, 0.13mm22, Zero-Static Power, Self-Timed Capacitance to Digital Converter." SSDM 2009, OCT.



Accuracy

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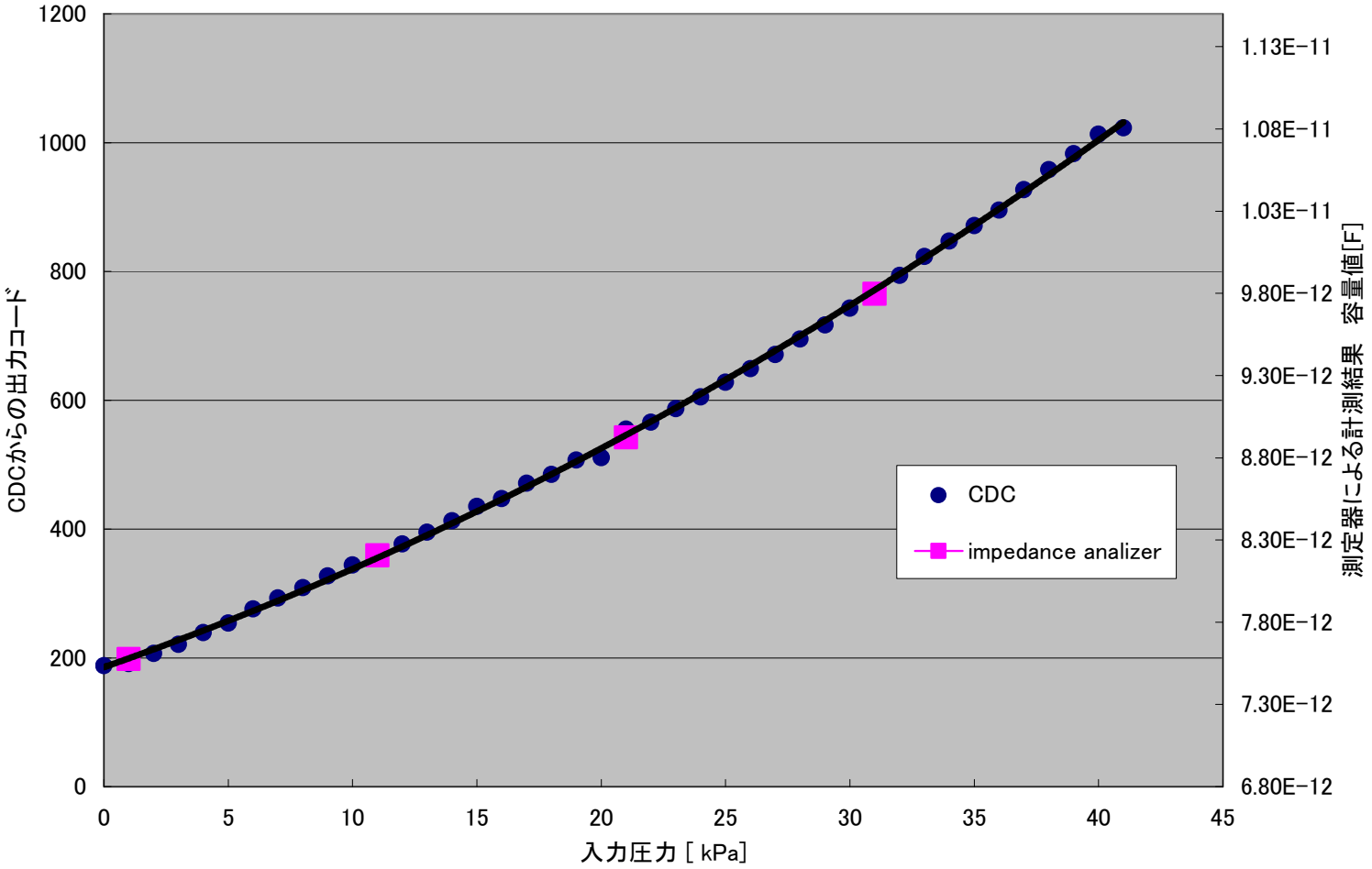
Same accuracy as an impedance meter.



New particle detector for nuclear physics

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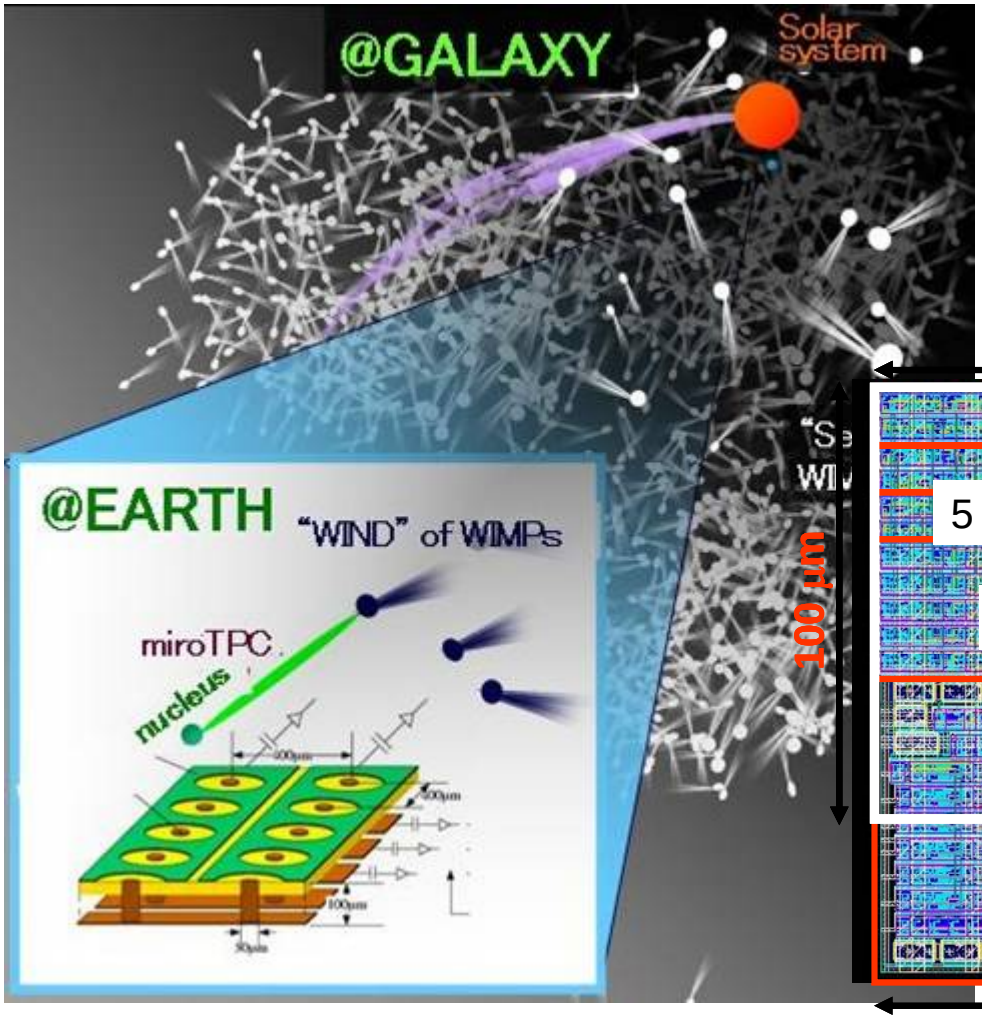
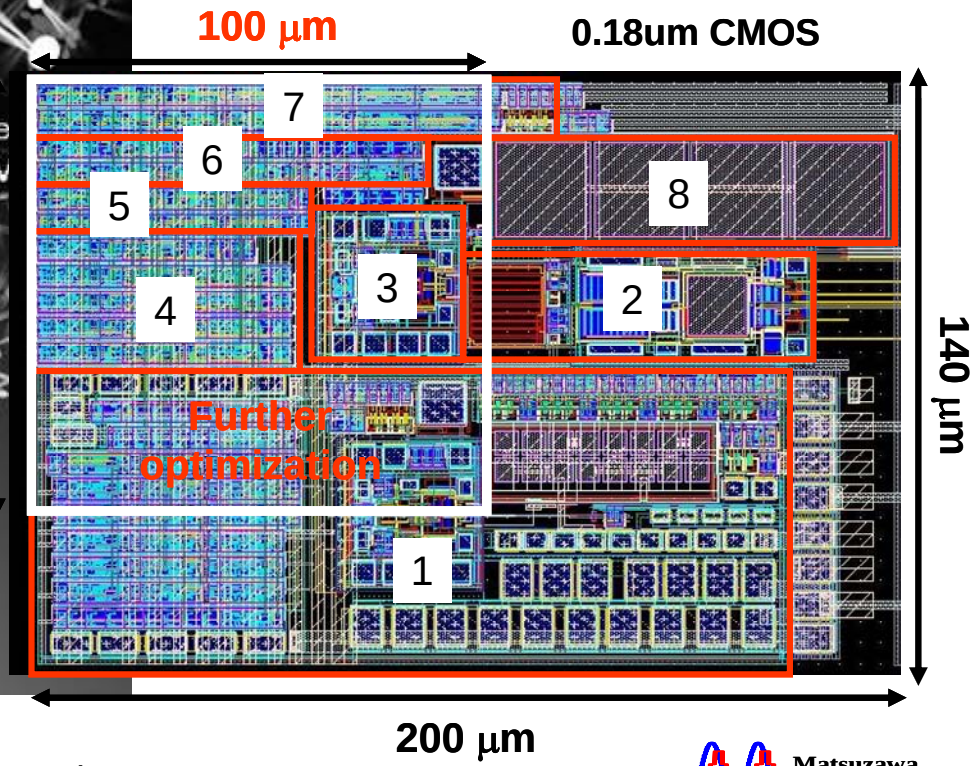
Developing new particle detector for nuclear physics



QPIX

A. Matsuzawa, Vu Minh Khoa, M. Miyahara, T. Kurashina, A. Sugiyama, K. Miuchi, and S. Tanaka, "A new particle detector LSI Qpix: integrating high speed ADC for each pixel", The 1st international conference on Technology and Instrumentation in Particle Physics, March 2009.



Basic functions of QPIX

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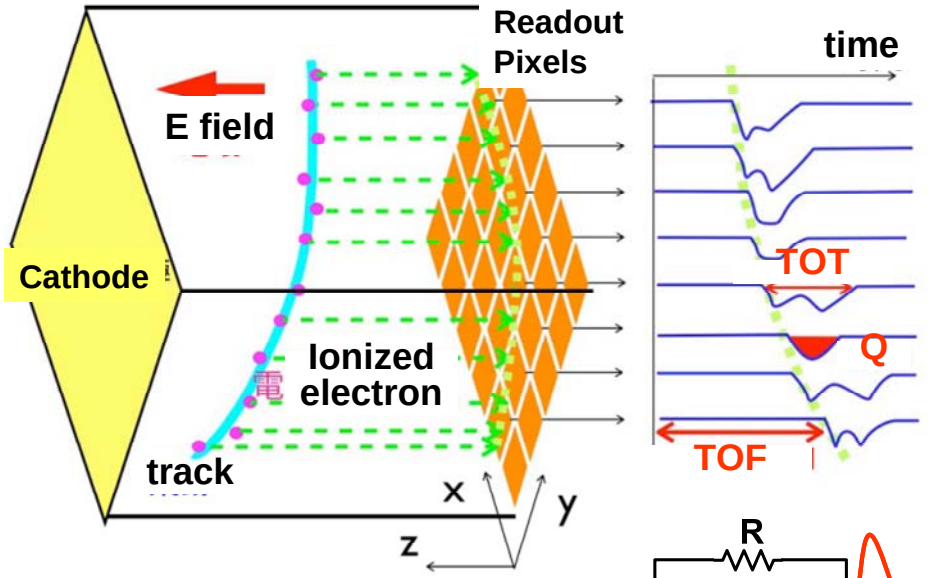
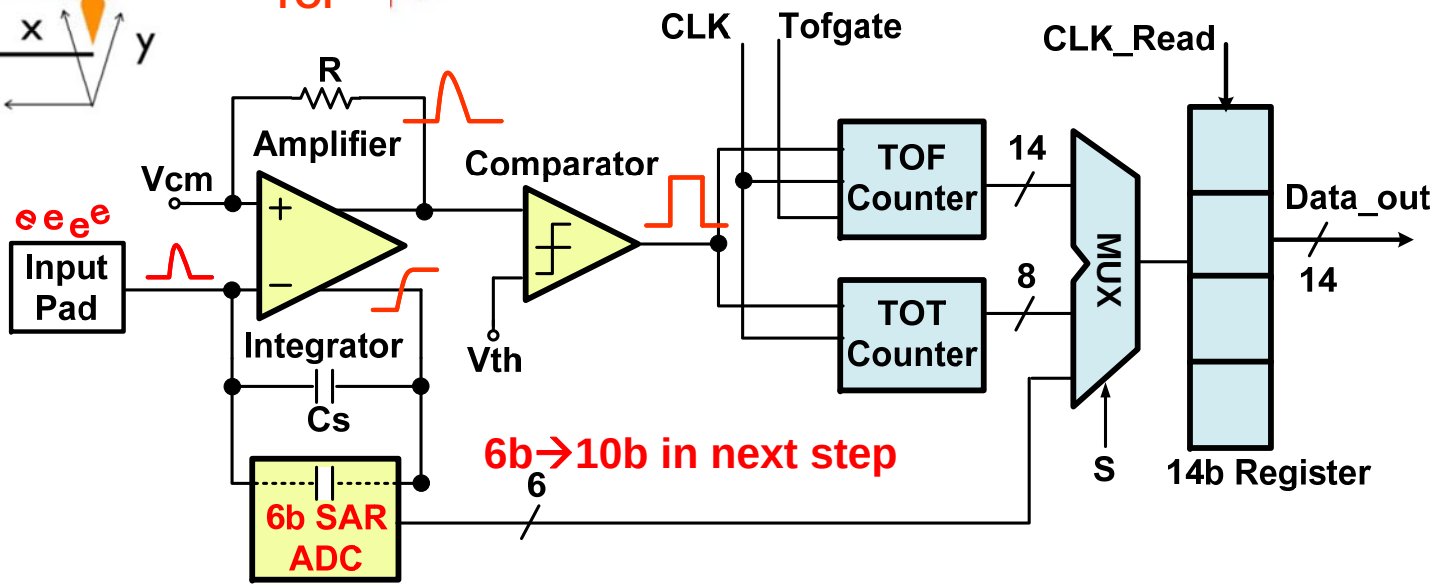
A world first particle detector having an ADC in each pixels.



QPIX can measure the total charge Q , as well as TOF and TOT.



Matsuzawa & Okada Lab.

Experimental setup and measured result

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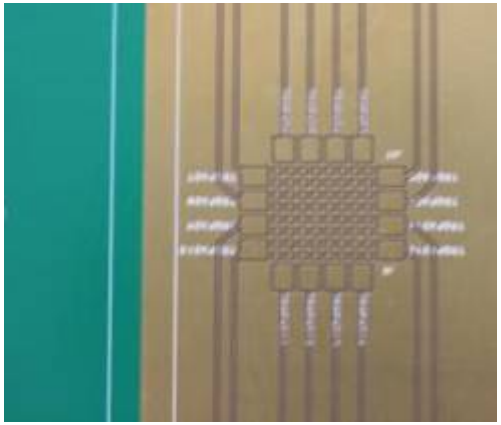
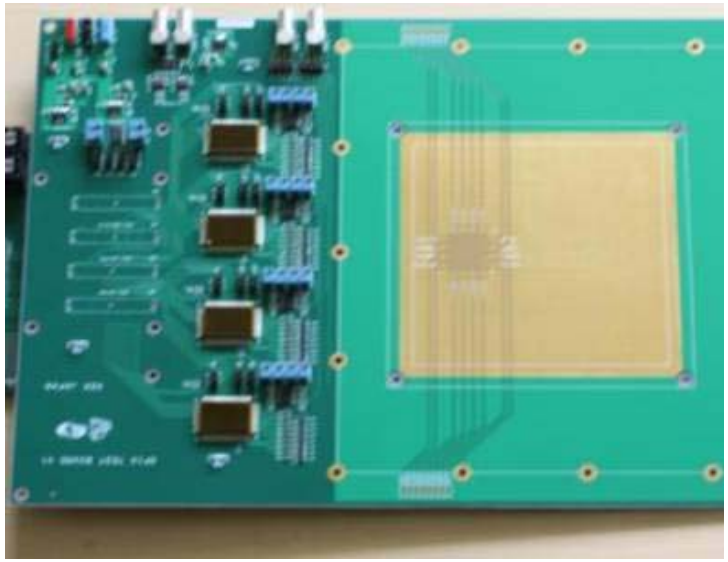
We could detect and measure the nuclear particles

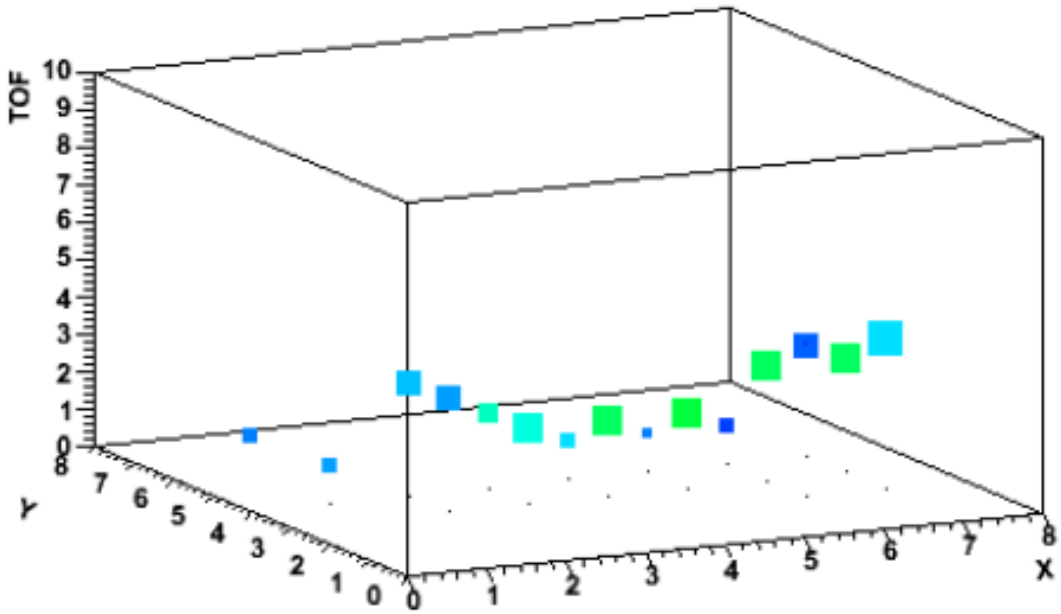




Measuring board

16 pixels

Trajectory of particle



Low voltage LC VCO

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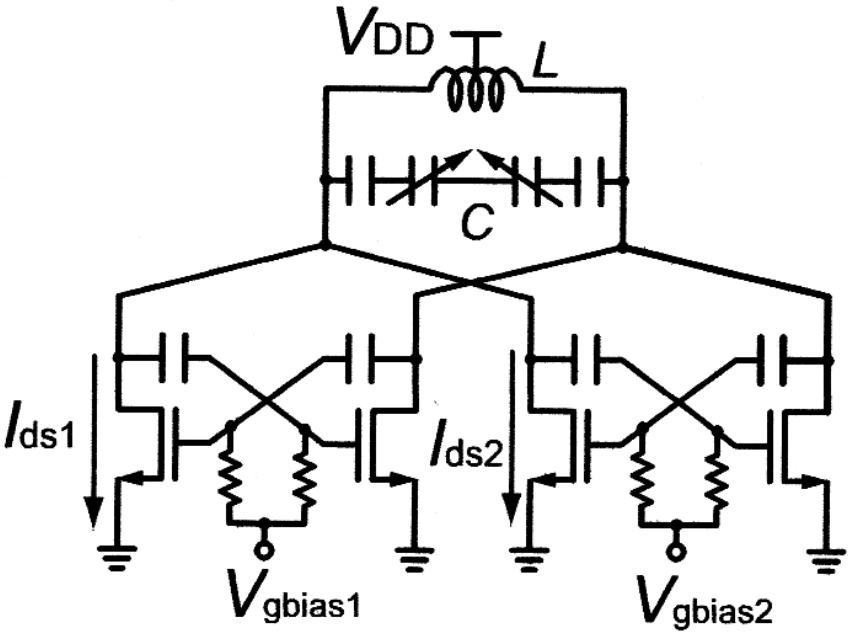
Developed 0.2V LC VCO

Class C with start-up circuit

K. Okada, Y. Nomiyama, R. Murakami, and A. Matsuzawa,
"A 0.114mW Dual-Conduction Class-C CMOS VCO with 0.2V Power Supply,"
Dig. Symp. VLSI Circuits, pp.228-229, June, 2009.



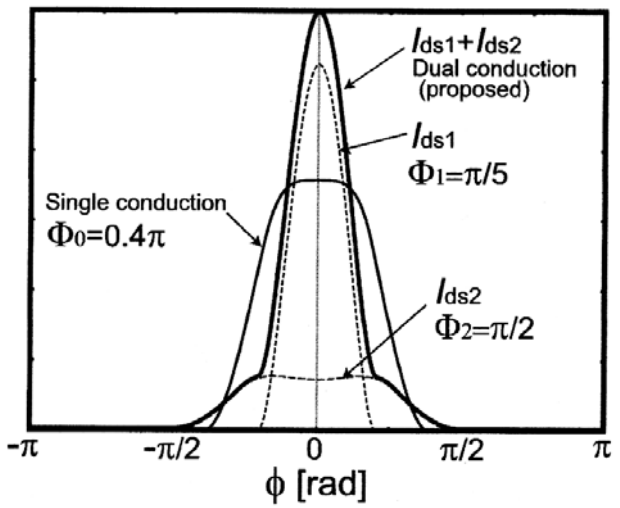


Fig. 2. MOS current waveform of single- and dual-conduction class-C VCOs under the same signal amplitude ($A_t = 3/4 * V_{DD}$, and $V_{th} = 5/2 * V_{DD}$).

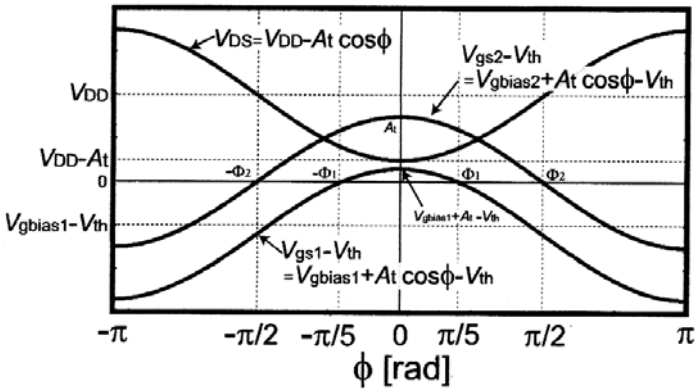


Fig. 3. Voltage waveform of the proposed VCO for drain and both gate voltages.

Performance of 0.2V VCO

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Low power of 110uW at 4.5GHz generation

0.2V、
-104dBc/Hz @1MHz-offset
FoM=187dBc/Hz

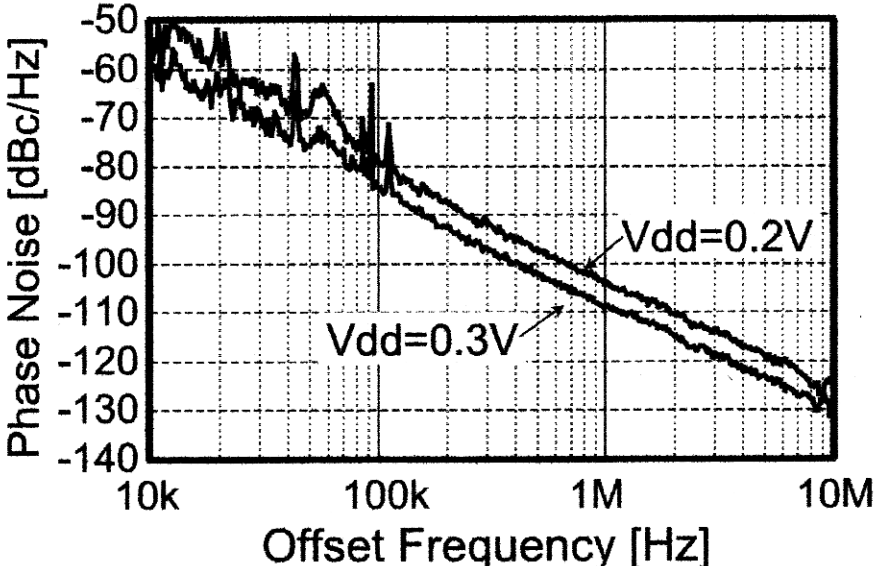

TABLE 1. Performance summary.

	[2]	[1]	[1]	This work	
Technology	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	
Supply voltage	1.0 V	0.5 V	0.35 V	0.3 V	**0.2** V
Power consumption	1.3 mW	0.57 mW	1.46 mW	0.159 mW	**0.114 mW**
Oscillation frequency	4.9 GHz	3.8 GHz	1.4 GHz	4.5 GHz	4.5 GHz
Phase noise	−130 dBc/Hz @3MHz-offset	−119 dBc/Hz @1MHz-offset	−129 dBc/Hz @1MHz-offset	−109 dBc/Hz @1MHz-offset	−104 dBc/Hz @1MHz-offset
FoM	196 dBc/Hz	193 dBc/Hz	190 dBc/Hz	190 dBc/Hz	187 dBc/Hz
Chip area	0.50 mm^2	0.23 mm^2	0.76 mm^2	0.29 mm^2	
Topology	Class-C (single)	TF	TF	Class-C (dual)	

Development of full digital power supply

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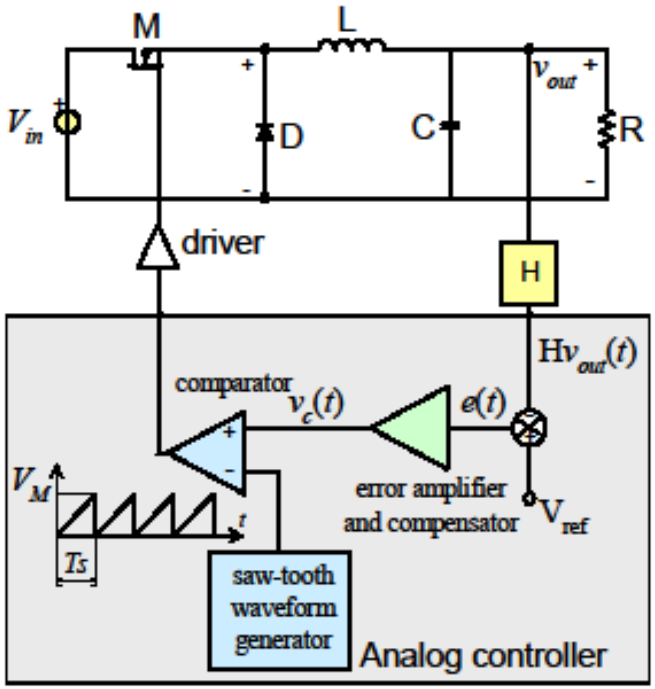
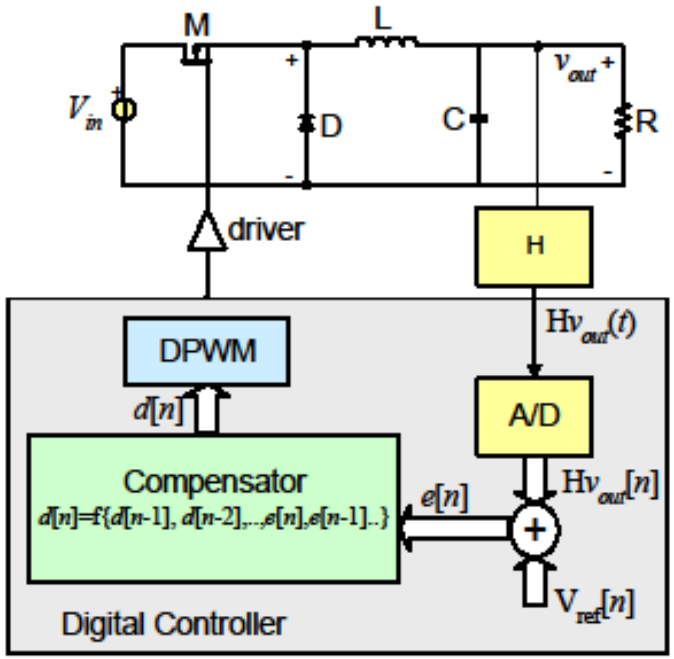
DC/DC converter uses analog control method.
We have started to develop full digital power supply.

Analog Implementation



Digital Implementation



ADC and PWM for full digital power supply

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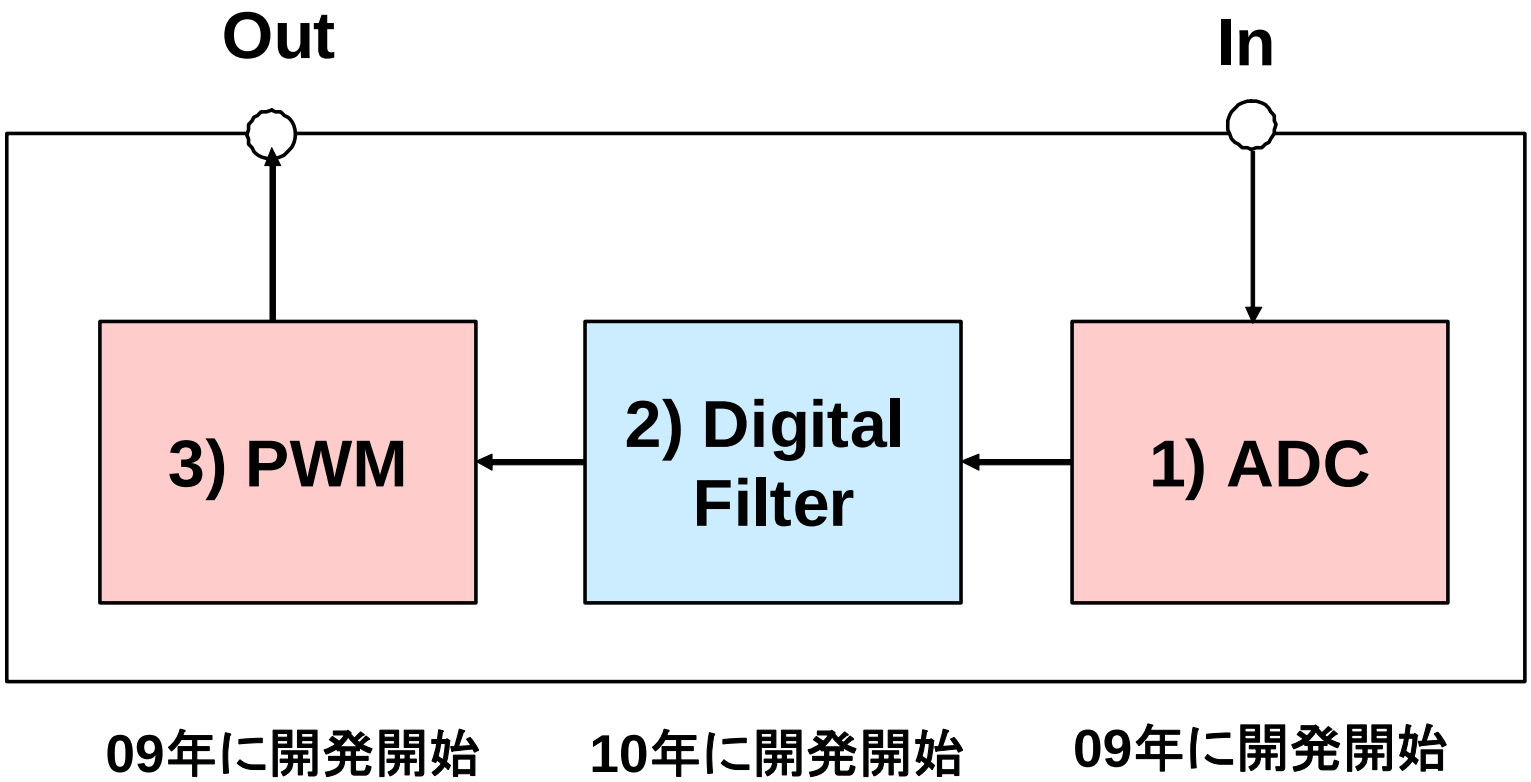
We have started to develop ADC and PWM for the first step

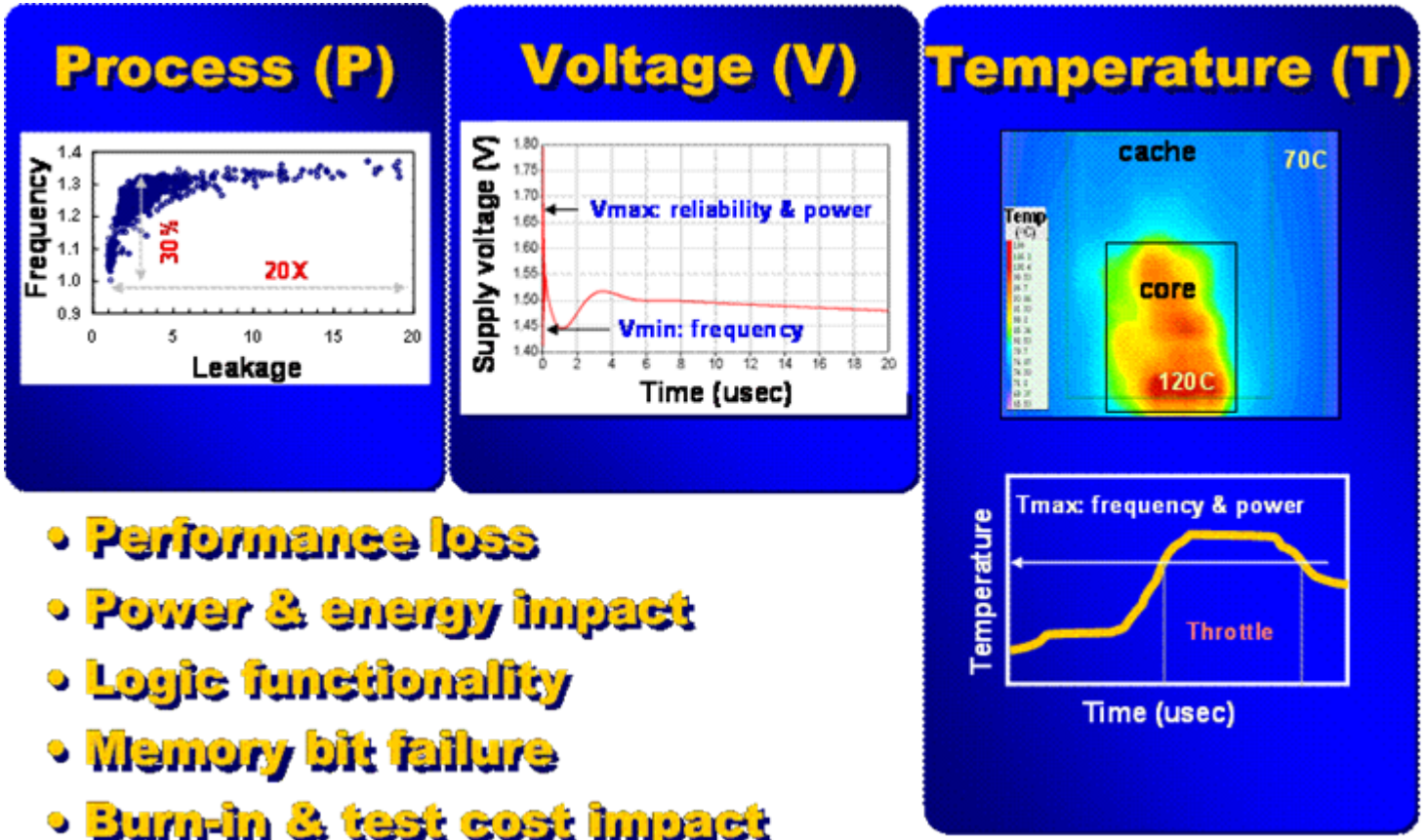
ADC: 12bit, 80MSps, 5mW

has low power mode and high speed mode



Micro-power systems: PVT issues in digital LSIs

Fluctuation of device parameter, stabilization of power supply voltage, and reduction of local heating become serious issues in digital LSIs.



Courtesy
Dr. Vivek De,
Intel

Adaptive Power supply voltage

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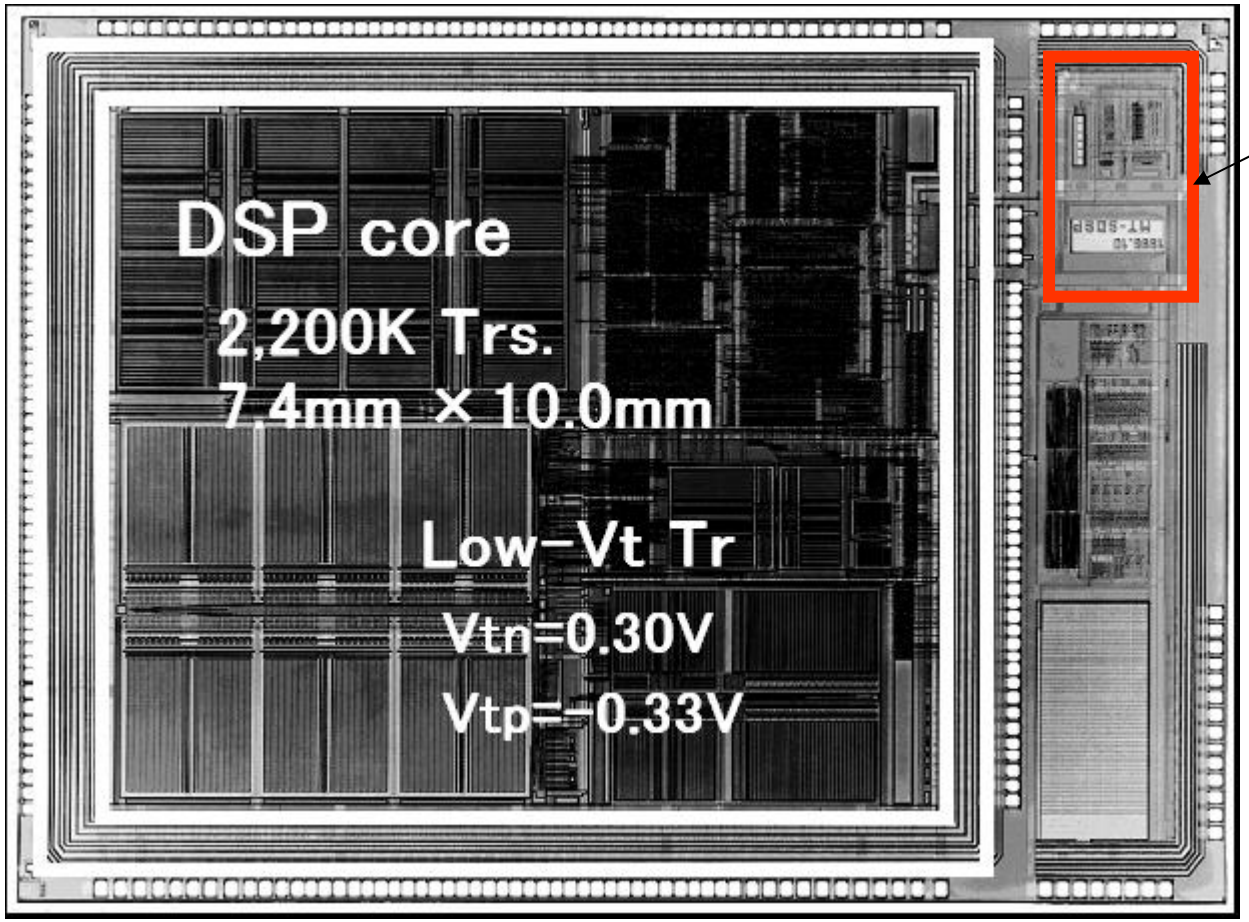
Sakiyama et al., Symp. On VLSI Circuits '97



Adaptive supply voltage control circuits

0.35umCMOS
2.2M Tr
20MIPS
12mW (1.2V, internal)

leak current
500uA: active
1uA: standby

High efficiency and low noise embedded DC/DC

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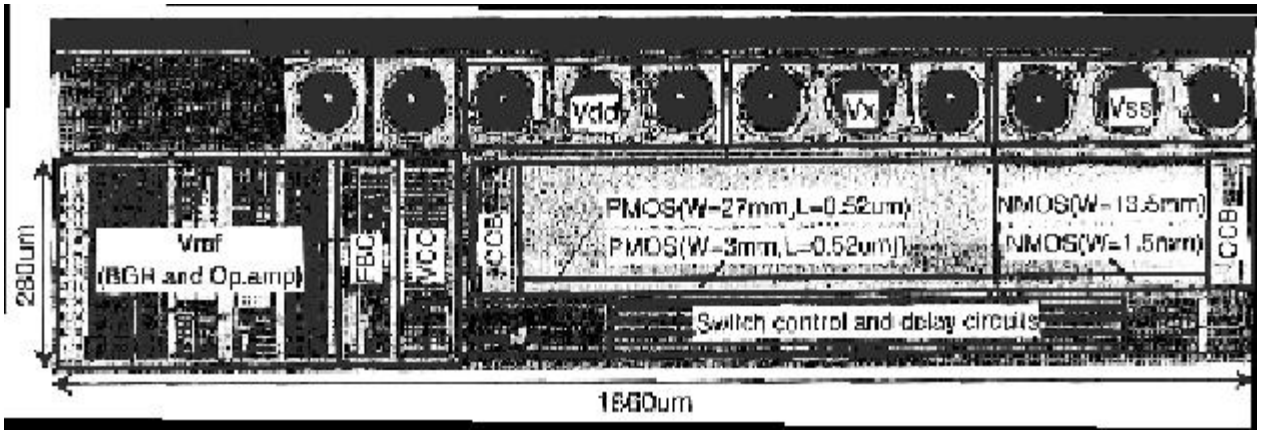
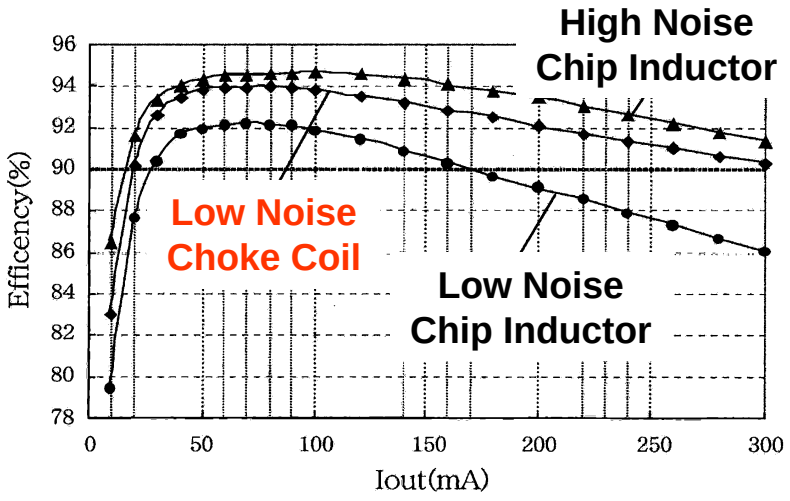
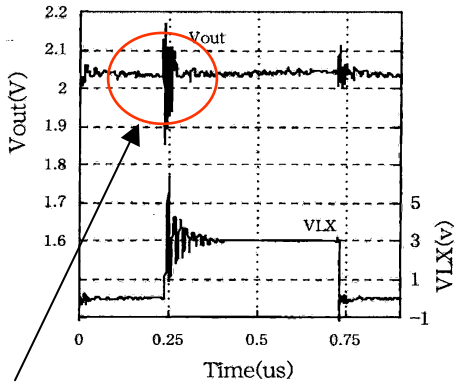
High efficiency of 94% and low noise of 15mVpp.

S.Sakiyama et al., ISSCC99



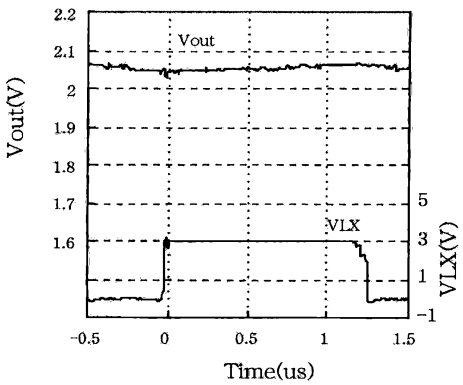


Conventional



300mV

Improved



15mV