A 484-μm^2 21-GHz LC-VCO beneath a Stacked-Spiral Inductor

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***Abstract*— This paper proposes an ultra compact LC-VCO. Due to the speed-up of CMOS digital circuits, jitter of ring oscillators is becoming a critical problem. Even though a LC-VCO has a better phase noise, a layout size of on-chip inductor is a problem as a clock generator. Thus, the proposed LC-VCO consists of a very compact stacked-spiral inductor and active components placed beneath the inductor. The VCO is implemented by a 65-nm CMOS process, and the chip area is only 484 μm^2. This VCO achieves a phase noise of -89.4 dBc/Hz@1MHz, power consumption of 1.92 mW, and FOMA of 206 dBc/Hz.**

I. Introduction

Due to the miniaturization of CMOS process technology, it has obtained higher $f_{\rm T}$ and $f_{\rm max}$. Low power, low noise clock generation is a key technology for wireless applications and high speed communication systems over a gigahertz clock frequency. At the same time, the low-supply voltage, $V_{\rm DD}$, is also needed for the scaled CMOS transistors.

Ring oscillators have usually been used as a clock generator, especially at lower frequencies. The jitter characteristic of ring oscillators is degraded by the low supply voltage, and a larger power consumption would be required to improve the jitter. On the other hand, LC-VCOs have a much lower phase noise and lower power consumption than ring oscillators. Thus, ring oscillators are demanded to be replaced with LC-VCOs. One of the remaining issues as a clock generator is a layout area of LC-VCO, which is usually very large due to an on-chip inductor.

In this paper, an ultra compact LC-VCO is presented, which consists of a very compact stacked-spiral inductor and active components placed beneath the inductor. The stacked-spiral inductor has a multi-layer structure, which realizes a very small size in return for the degradation of quality factor[1]. In addition, the proposed one has active components, such as a bias transistor, cross-coupled transistors, and a varactor, placed beneath the stacked-spiral inductor[2]. Thus, the proposed one can realize an ultra compact size. This paper explains design consideration to minimize the layout area and reduce the influence of the circuit stacking.

II. Stacked-spiral inductor

In this section, downscaling of on-chip inductors is discussed, especially for a stacked-spiral inductor. Then, the influence of downscaling of VCO is analyzed.

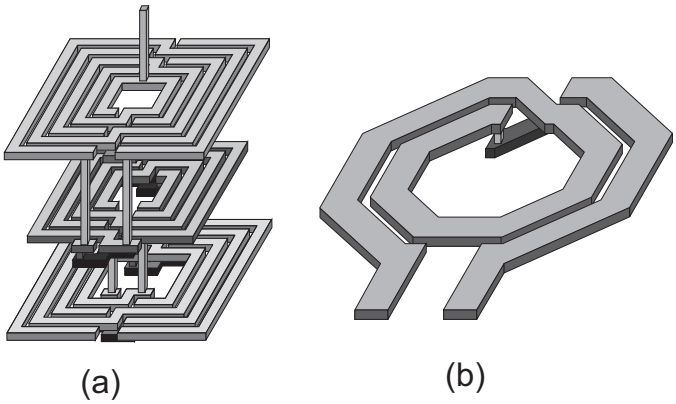

Fig. 1. (a)Stacked-spiral inductor (b)Mono-layer inducor

The phase noise can be derived from the following equation [3]:

$$\mathcal{L}(f_{\rm offset}) = 10\log\left[\frac{2{\rm k}T}{P_{\rm sig}}\left(\frac{f_0}{2Q_{\rm tank}f_{\rm offset}}\right)^2\right] \qquad (1)$$

where k is Boltzmann's constant, T the absolute temperature, $P_{\rm sig}$ the output power, f_0 the oscillation frequency, $f_{\rm offset}$ the offset frequency, $Q_{\rm tank}$ the quality factor of the resonators. According to Eq. (1), $Q_{\rm tank}$ is very important for the performance of VCOs.

Fig. 1 shows structures of on-chip inductors for a 20 GHz LC resonator. Fig. 1(a) is a proposed differential stacked-spiral inductor using 6 metal layers, and Fig. 1(b) shows a mono-layer inductor. The stacked-spiral inductor has 15-μm outer diameter and 0.8-μm line width, and the mono-layer one has 100-μm outer diameter and 8-μm line width.

On-chip inductor models can be simplified as shown in Fig. 2. Table I shows the parameters of the inductors shown in Fig. 1, which are simulated by a 3D electromagnetic simulator HFSS.

The mono-layer inductor has a very low series resistance $R_{\rm s}$ and high quality factor Q due to the wide line width. On the other hand, the stacked-spiral inductor also has a high inductance $L_{\rm s}$. However, a quality factor is not so high, because the resistance $R_{\rm s}$ is high due to a long narrow spiral line. If a LC-VCO uses the staked-spiral inductor, the VCO

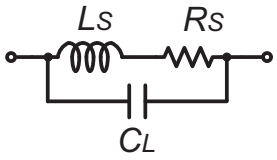

Fig. 2. A simplified model of on-chip inductor.

TABLE I
CHARACTERISTICS OF THE INDUCTORS.

	Stacked-spiral	Mono-layer
L_{S} [nH]	1.16	0.51
R_{S} [Ω]	51.7	4.19
C_{L} [fF]	9.76	18.6
Q	2.82	15.5
Area [$\mu\mathrm{m}^2$]	225	10000

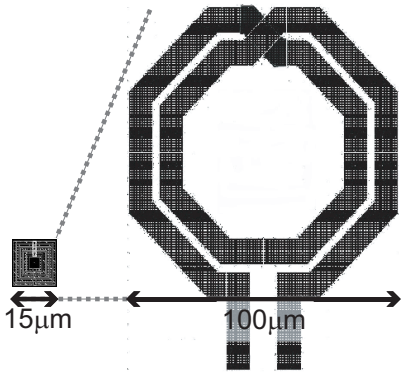

Fig. 3. Comparison of inductor sizes.

consumes more power or has worse phase noise because of the degraded quality factor. On the other hand, the layout area can be dramatically shrank as shown in Fig. 3. The stacked-spiral inductor has 44 times smaller area than the mono-layer inductor.

III. REST PART PLACEMENT BENEATH THE SPIRAL INDUCTOR

Fig. 4 shows a circuit schematic of the proposed LC-VCO, which is a simple NMOS-topology of LC-VCO. The NMOS topology can reduce the layout area while PMOS and CMOS topologies require larger cross-coupled transistors. Even if the layout area of on-chip inductors can be shrank, rest parts like transistors and capacitors remain to be large. A further minimization requires an area reduction of the rest parts. One of the ways is to place the rest parts beneath the inductor as shown in Fig. 5. While this contributes to reduce the total layout area dramatically, it becomes an issue to consider the interaction between the inductor and the rest parts. The rest parts do not only consist of transistors and capacitors but also metal wires. The metal wires might build a loop with transistors and capacitors, so a carefull design is required. The loop causes degradation of inductor in terms of inductance and quality factor, which also causes degradation in VCO

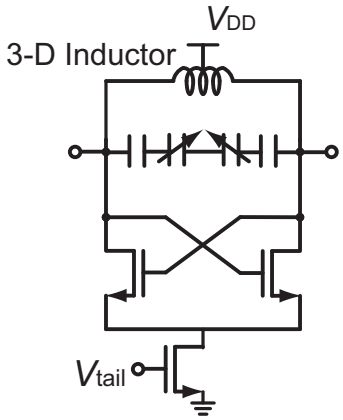

Fig. 4. Circuit schematic of NMOS LC-VCO.

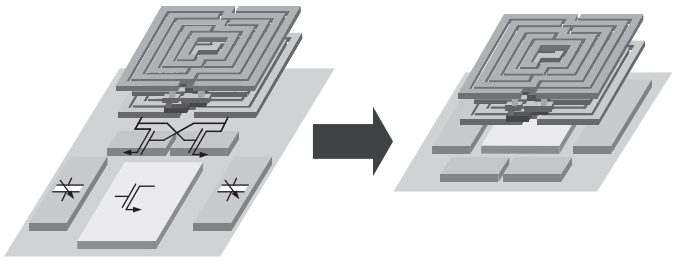

Fig. 5. Circuit stacking beneath the inductor.

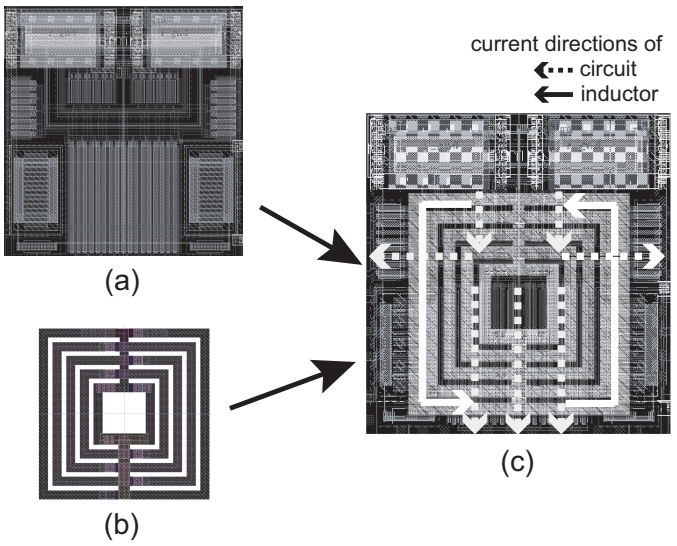

Fig. 6. Layouts of (a)core-circuit, (b)stacked-spiral inductor and (c)total VCO.

performances, *e.g.*, phase noise, output power, and power consumption.

To reduce the influence on L_{S}, transistors should be placed orthogonally to the inductor trace. This influence is simulated by HFSS with a metal-line model. Fig. 7 and Table II show the results of the simulation. The results show that the inductance is barely reduced and the quality factor is degraded by 7-

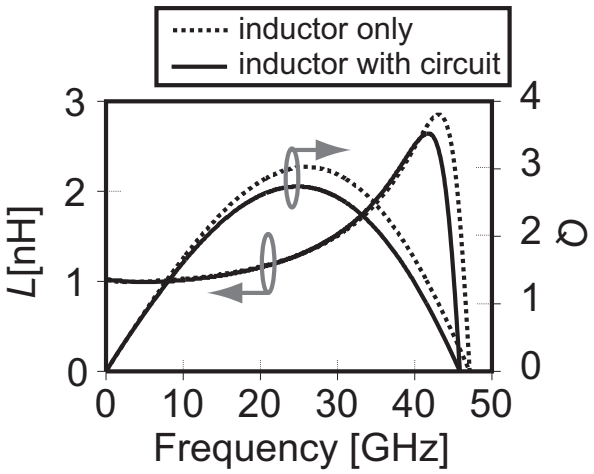

Fig. 7. A comparison of inductance and quality factor.

TABLE II
THE SIMULATED INFLUENCES OF THE CORE CIRCUIT ON L_{S} AND Q

@20GHz	L_{S}[nH]	C_{P}[fF]	Q
Inductor only	1.16	9.84	2.82
With core-circuit	1.15	10.5	2.62

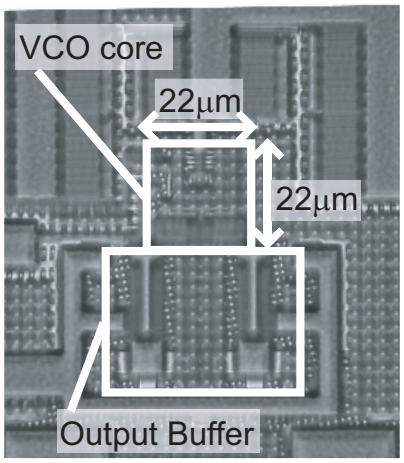

Fig. 8. Chip micrograph.

%, which is equal to 0.6-dB degradation in the phase noise. While the influence of the core circuit on the phase noise is very little, and the benefits of area saving is very larger than the degradation of phase noise. Thus, the proposed technique utilizing both the stacked-spical inductor and beneath-placed devices is practical.

IV. MEASUREMENT RESULT

This proposed LC-VCO is implemented by using a 65-nm CMOS process. Fig. 8 shows the chip micrograph, and the core area is $484\mu\mathrm{m}^2$. It is measured by using a signal source analyzer (Agilent E5052B + down converter E5053A) and an external buffer amplifier. The supply voltage is 0.6 V. The power consumption is 1.92 mW, and the oscillation frequency

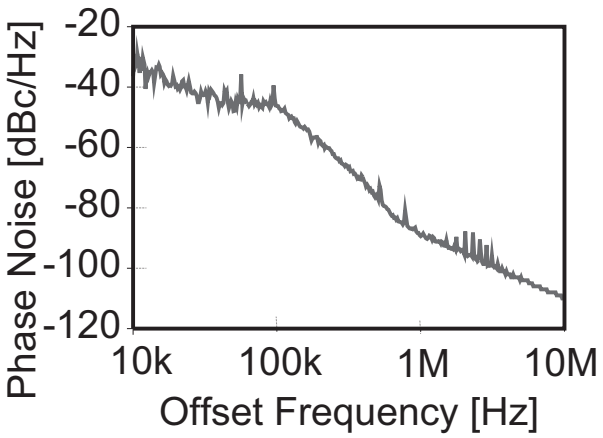

Fig. 9. Measured phase noise.

is 21 GHz with a 0.6-GHz tuning range. Fig. 9 shows the measured phase noise, and it is -89.4 dBc/Hz at 1MHz offset and -110 dBc/Hz at 10 MHz offset.

In general, the figure-of-merit (FoM) is used to evaluate the performance of VCOs. FoM is a normalized phase noise by oscillation frequency, offset frequency and power consumption, which can be defined by the following equation[4],

$$FoM = -\mathcal{L}(f_{\mathrm{offset}}) + 20\log\left(\frac{f_0}{f_{\mathrm{offset}}}\right) - 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right) \quad (2)$$

where P_{DC} is power consumption. The fabricated VCO achieves FoM of 173-dBc/Hz, and it is almost impossible for ring oscillators to achieve FoM of 173-dBc/Hz.

There is a trade-off between the area and FOM, because a larger diameter is required for to obtain a higher quality factor of inductor. VCOs should be evaluated with the figure-of-merit normalized for area(FoMA), it is expressed by the following equation[5].

$$FoMA = FoM - 10\log\left(\frac{\mathrm{Area}}{1\mathrm{mm}^2}\right) \quad (3)$$

The proposed LC-VCO achieves FoMA of 206-dBc/Hz. Table III summarizes the state-of-the-art results of clock generators using CMOS technology. The proposed LC-VCO demonstrates the best FoMA using a stacked-spiral inductor and beneath-placed devices.

V. CONCLUSIONS

This paper proposes an ultra compact LC-VCO using a stacked-spiral inductor with a beneath-placed core circuit. The oscillation frequency of the VCO is 21 GHz and it consumes 1.92 mW. The VCO has only 484-μm^2 chip area. The performance is better than convensional ring oscillators. The proposed LC-VCO achieves FoMA of 206dBc/Hz.

TABLE III

PERFORMANCE SUMMARY.

	Area [μm^2]	Power consumption [mW]	Phase noise [dBc/Hz]	Freq.	V_{DD} [V]	Tech. [nm]	FoMA [dBc/Hz]	Type
[1]	2597	2.8	-103@1MHz	5GHz(20GHz/4)	1	90	199	LC(3D-inductor)+Div.
[6]	2400	9.8	-101@600kHz	0.9GHz	3.3	350	182	Ring
[7]	290000	0.16	-109@1MHz	4.5GHz	0.3	180	195	LC(Dual-conduction)
This Work	484	1.92	-110@10MHz	21GHz	0.6	65	206	LC(3D-inductor)

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