A 484μm^2, 21GHz LC-VCO Beneath a Stacked-Spiral Inductor

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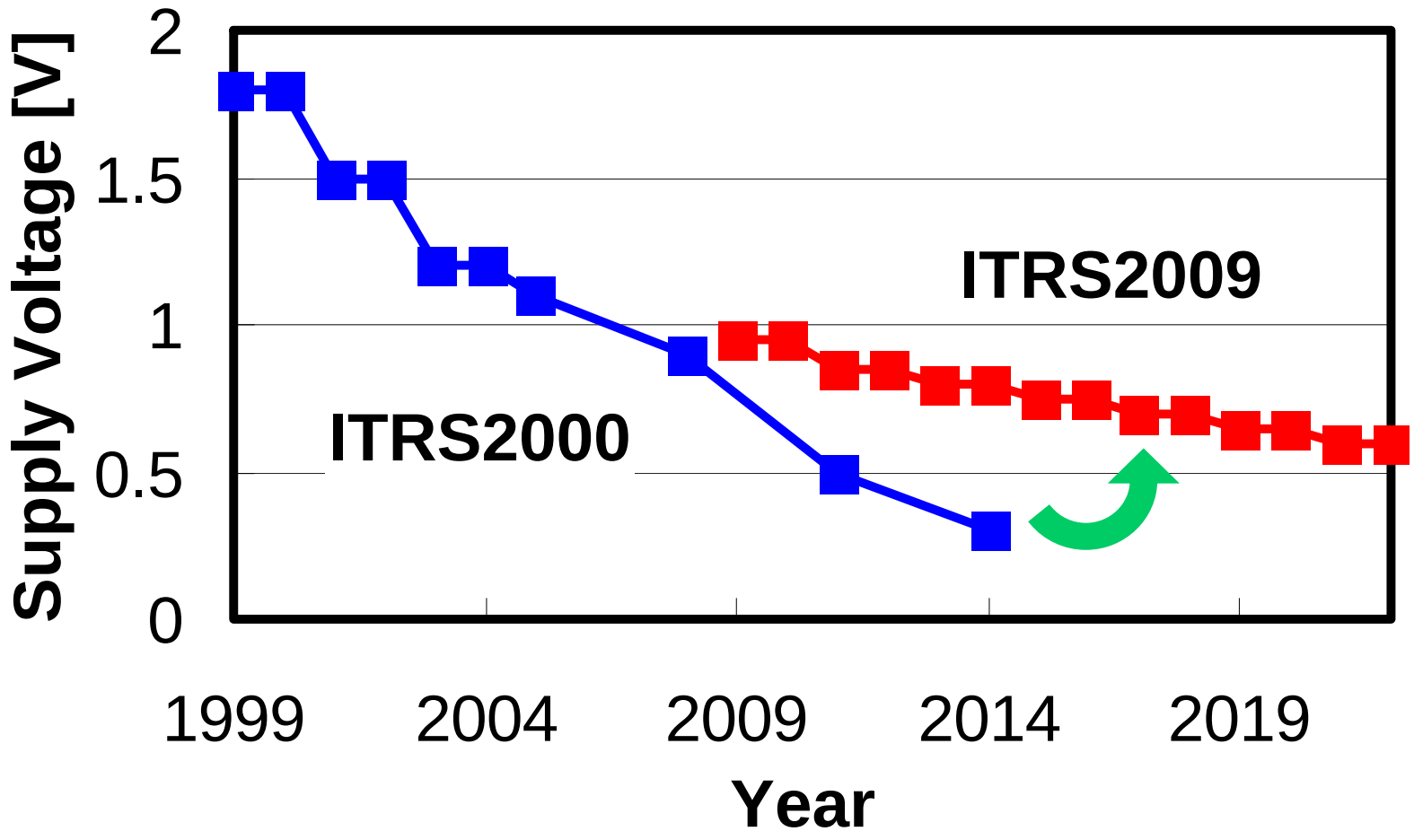
Scaling of Supply Voltage



As supply voltage is scaled down, low voltage circuits are needed.

Jitter (Phase noise) of Oscillators

- LC-VCO [1]

$$L_{LC} = \frac{\omega_0^{\,2}}{\omega_{offset}^{\,2}} \cdot \frac{kT}{V_{DD} I_{bias}} \cdot \frac{1+\gamma_n}{Q^2}$$

k:Boltzmann's constant
T: Absolute temperature
ω_0:freq.
ω_{offset}: Offset freq.
V_{TH}:Threshold voltage
M:Number of stages
Q:Quality factor of LC-tank
I_{bias}:Bias current
γ_n, γ_p:Noise factor

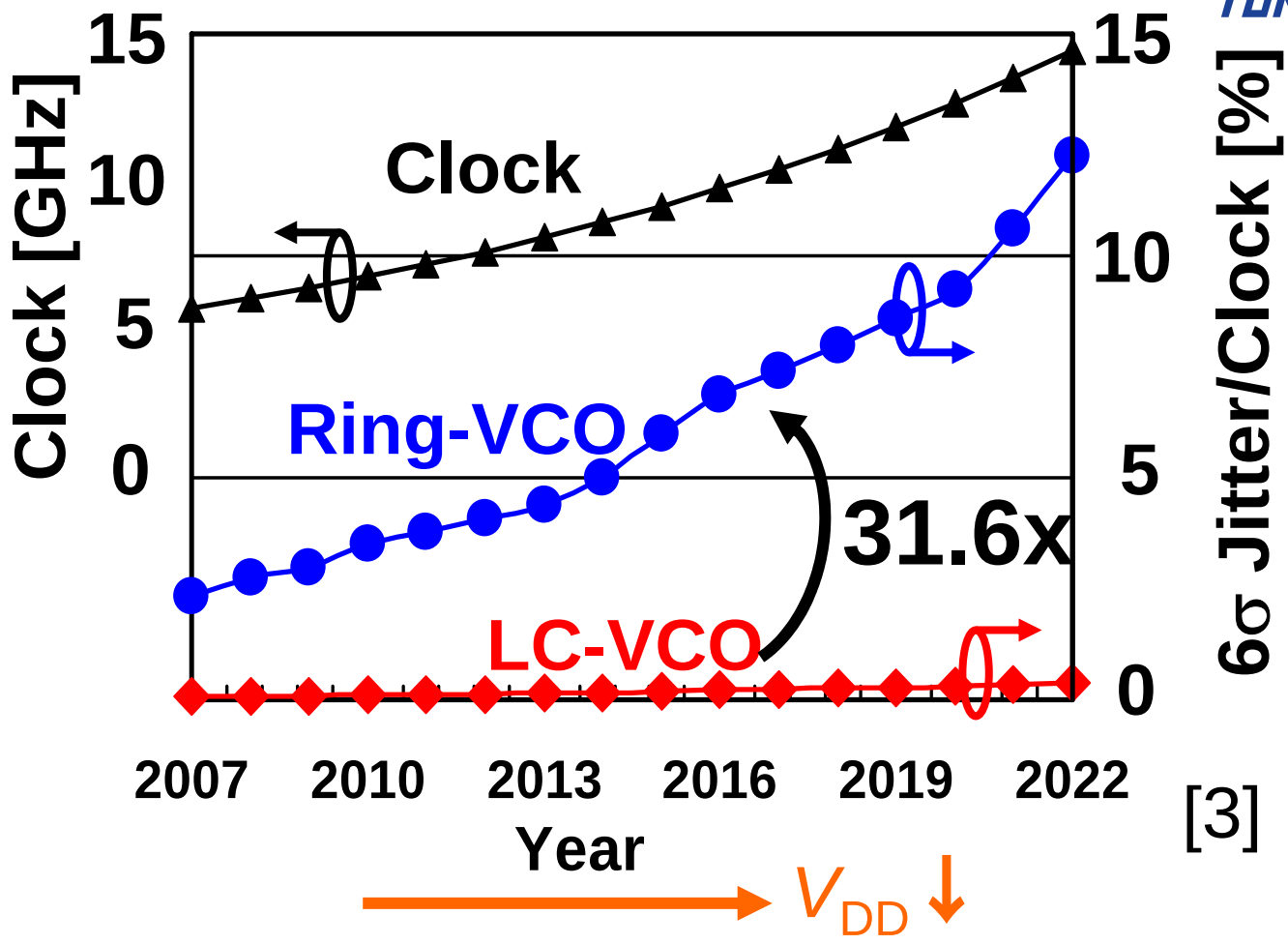
- Ring-VCO [2]

$$L_{Ring} = \frac{\omega_0^{\,2}}{\omega_{offset}^{\,2}} \cdot \frac{kT}{V_{DD} I_{bias}} \cdot 2M\left\{\frac{V_{DD}}{V_{DD}-V_{TH}}(\gamma_n+\gamma_p)+1\right\}$$

- Ring oscillators are more susceptible to the effect of downscaling the supply voltage.

[1]A. Mazzanti, et al., JSSC 2008 [2]A. Abidi, JSSC 2006

Problem of Clock Generator



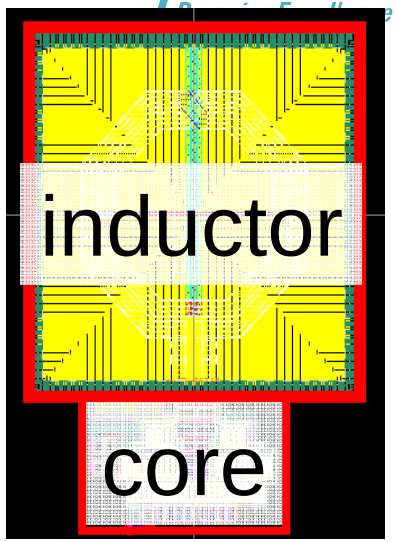
[3]

Ring-VCOs must be replaced with LC-VCOs

[3] K.Okada, *et al., VLSIC 2009*

Comparison of Oscillators

Ring		LC
Bad	Noise	Good
Large	Power cons. @high freq.	Small
Very small	Area	Large



To replace Ring-VCO by LC-VCO

Increasing chip area will become a problem.

A very small LC-VCO is desired.

The inductor occupies the dominant area in a LC-VCO.

→ It is needed to miniaturize the Inductor

Oscillation Frequency

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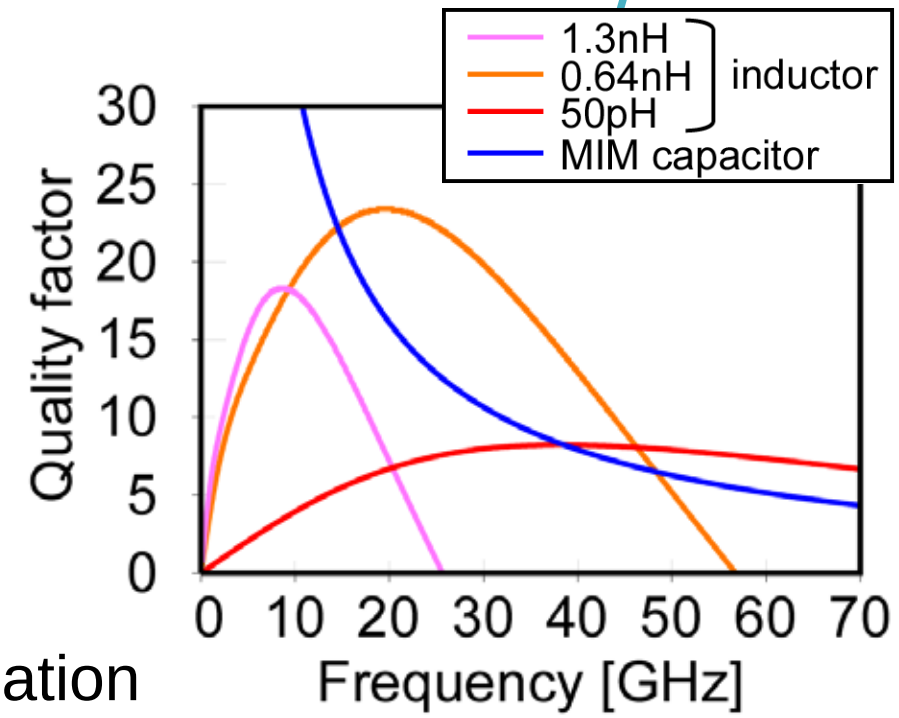
$$\text{frequency} = \frac{1}{2\pi\sqrt{LC}}$$

At a higher frequency, smaller inductance is needed.
VCO can be designed using a small inductor.

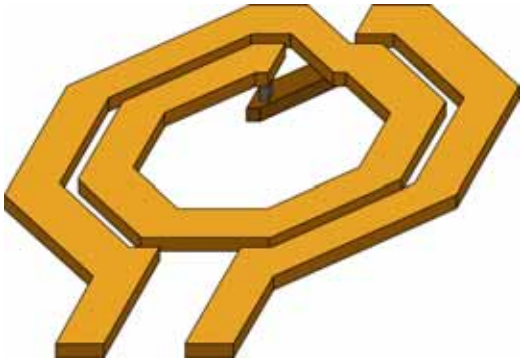


Over 20GHz, quality factor degradation is caused by the skin effect.

- Poor phase noise and high power consumption.

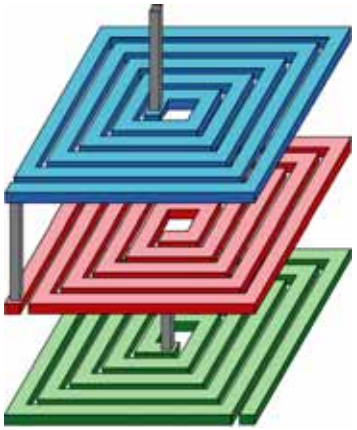
A 20GHz LC-VCO results in a good balance between area and phase noise

Stacked-spiral Inductor



Mono-layer inductor

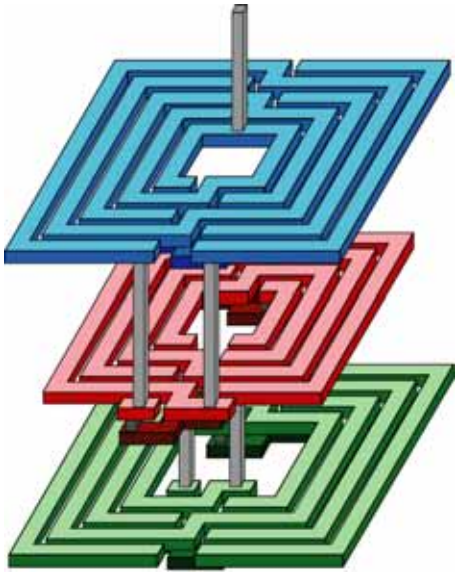
- Single layer
- Wide line width
- Large diameter
- Low R, High Q
- Large area



Stacked-spiral inductor

- Multi layer
- Narrow line width
- Small diameter
- High R, Low Q
- Ultra low space

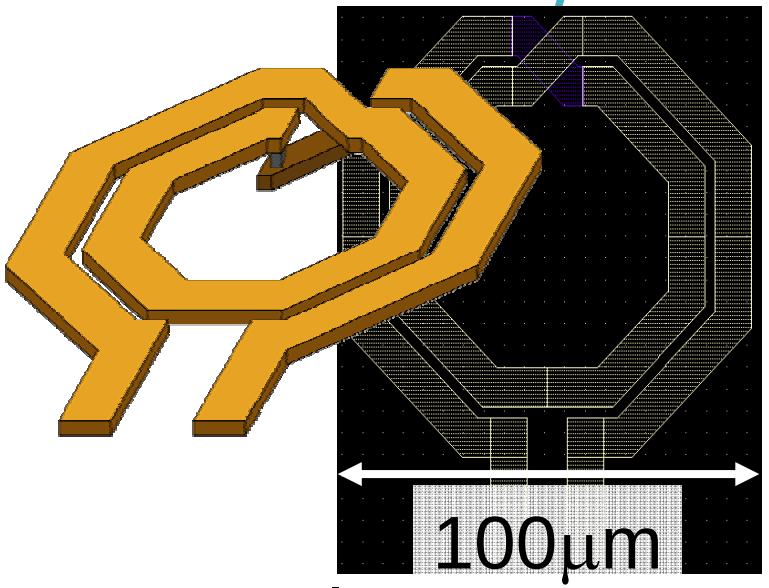
Comparison the Inductors



15μm

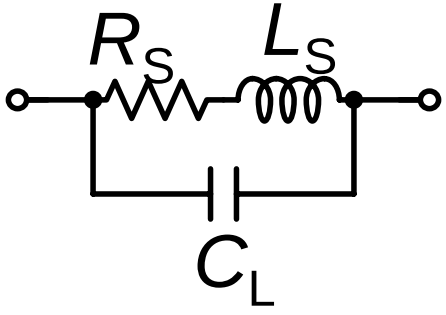
Area

1/44



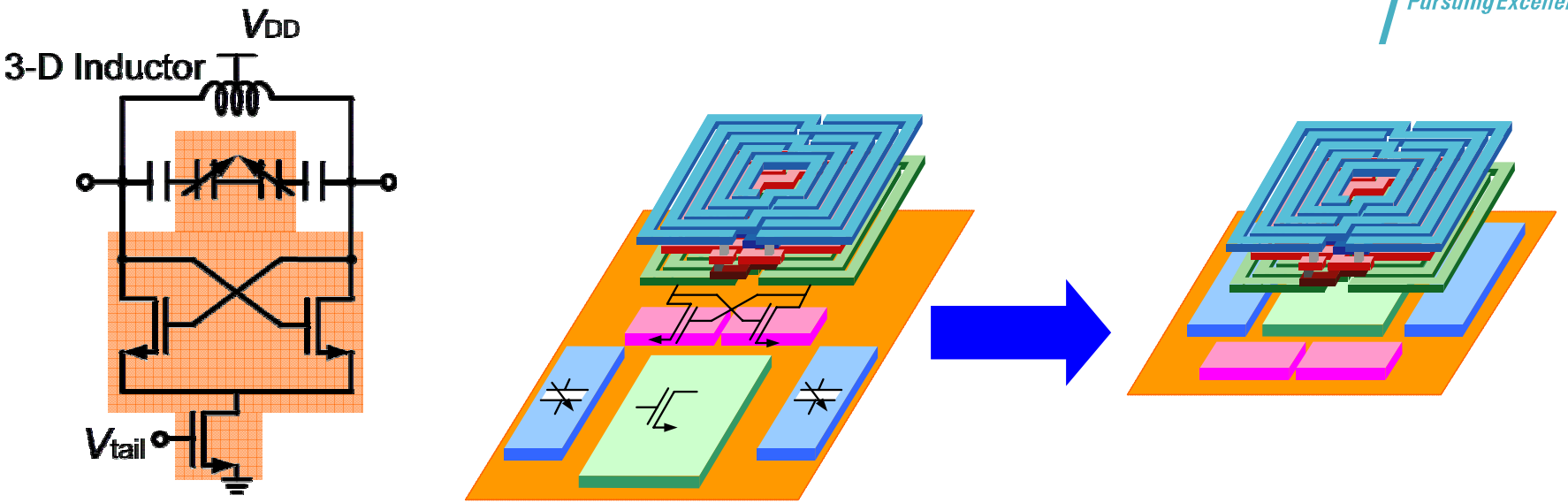
Stacked-spiral

Mono-layer



@20GHz	L_S [nH]	R_S [Ohm]	C_L [fF]	Q
Stacked-spiral	1.16	51.7	9.76	2.82
Mono-layer	0.51	4.19	18.6	15.5

Placement of Core-circuit



When the Inductor is miniaturized, the core-circuit size becomes close to the area of the inductor.

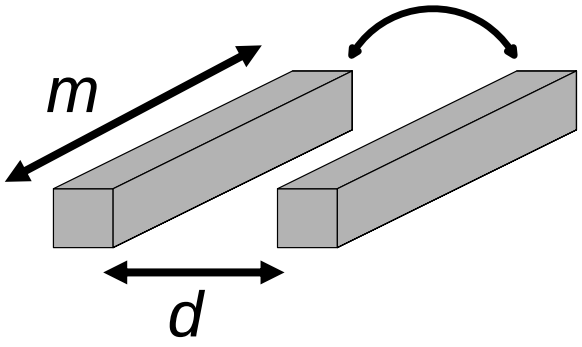
Insert core-circuit under the inductor.

Inductive coupling is a problem.

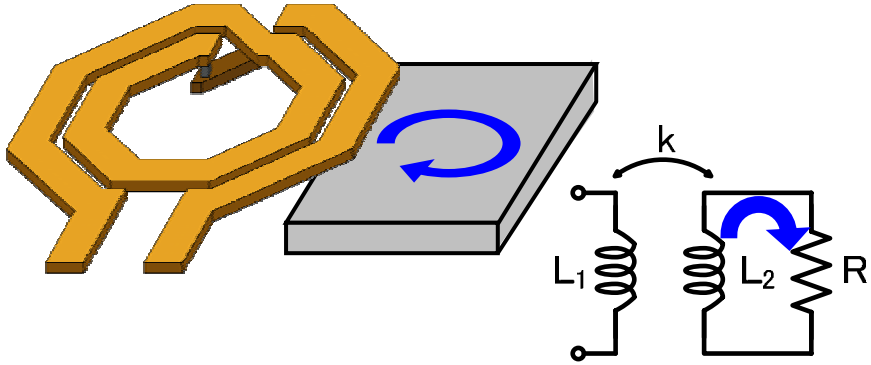
Inductive Coupling

Inductance and quality factor will be degraded by inductive coupling

parallel line



eddy current



$$M = 2m\left(\ln\left(\frac{m}{d}+\sqrt{1+\frac{m^2}{d^2}}\right)+\frac{d}{m}-\sqrt{1+\frac{d^2}{m^2}}\right)$$

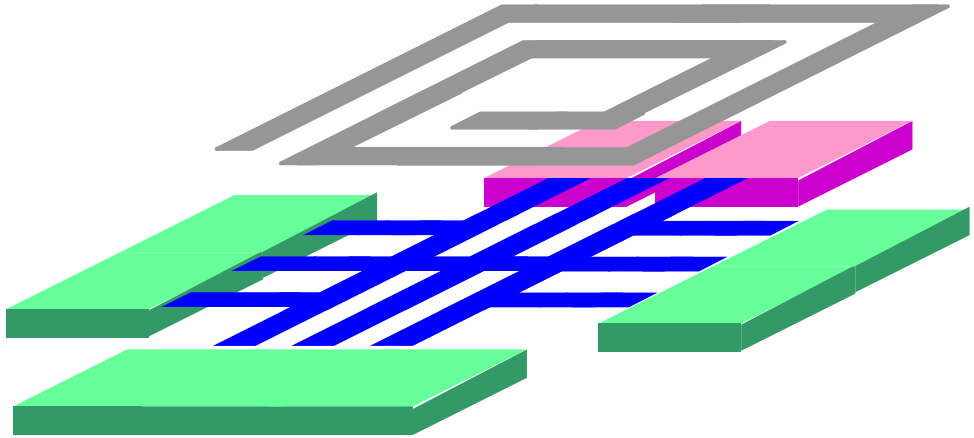
[4]

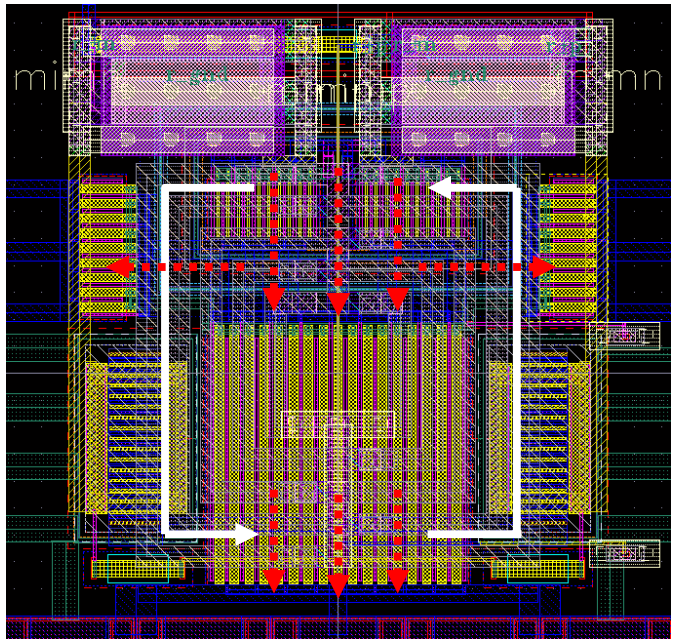
$$L = L_1\left(1-\frac{k^2\omega^2L_2^2}{R^2+\omega^2L_2^2}\right) = L_1\left(1-\frac{k^2Q_2^2}{1+Q_2^2}\right)$$

[4] H.M.Greenhouse, *TOPHAP 1974*

Reducing coupling

To reduce coupling, some layout techniques are applied.





- Slit shaping interconnections
- Placing inductor trace and interconnections orthogonally

Analysis of Interconnection Effects

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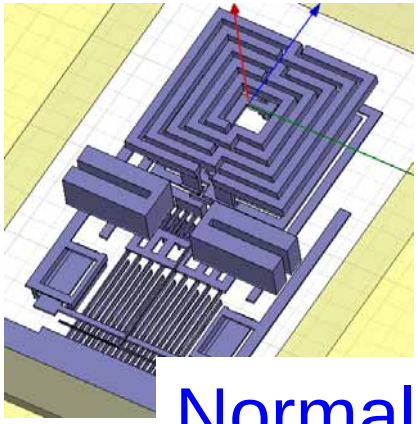
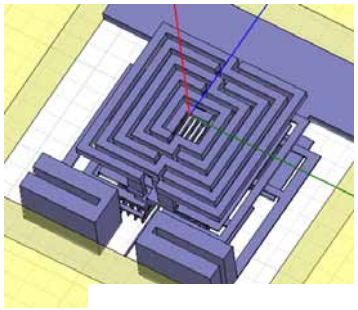
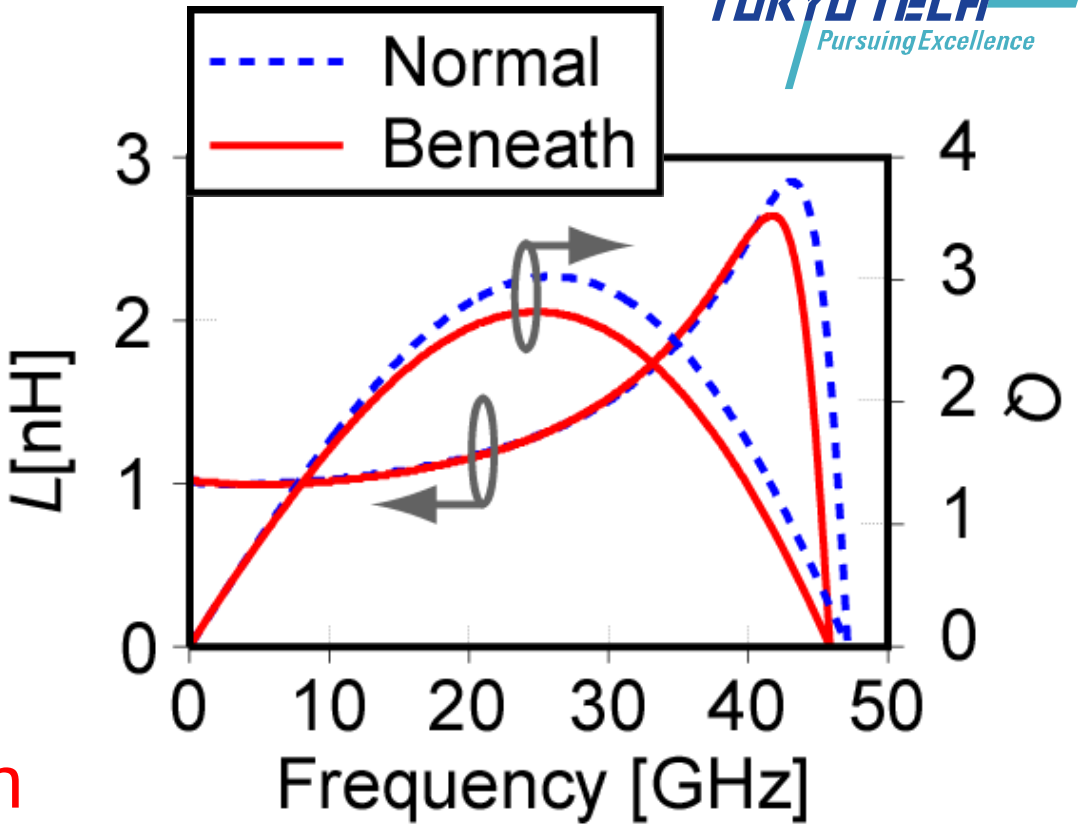
The model of the interconnections is created and simulated the influence on L_S and Q by HFSS.



Normal



Beneath



@20GHz	L_S [nH]	Q
Normal	1.16	2.82
Beneath	1.14	2.67

L_S 3%, Q 5%down

It corresponds 0.4dB in FoM.

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Chip Micrograph(1)

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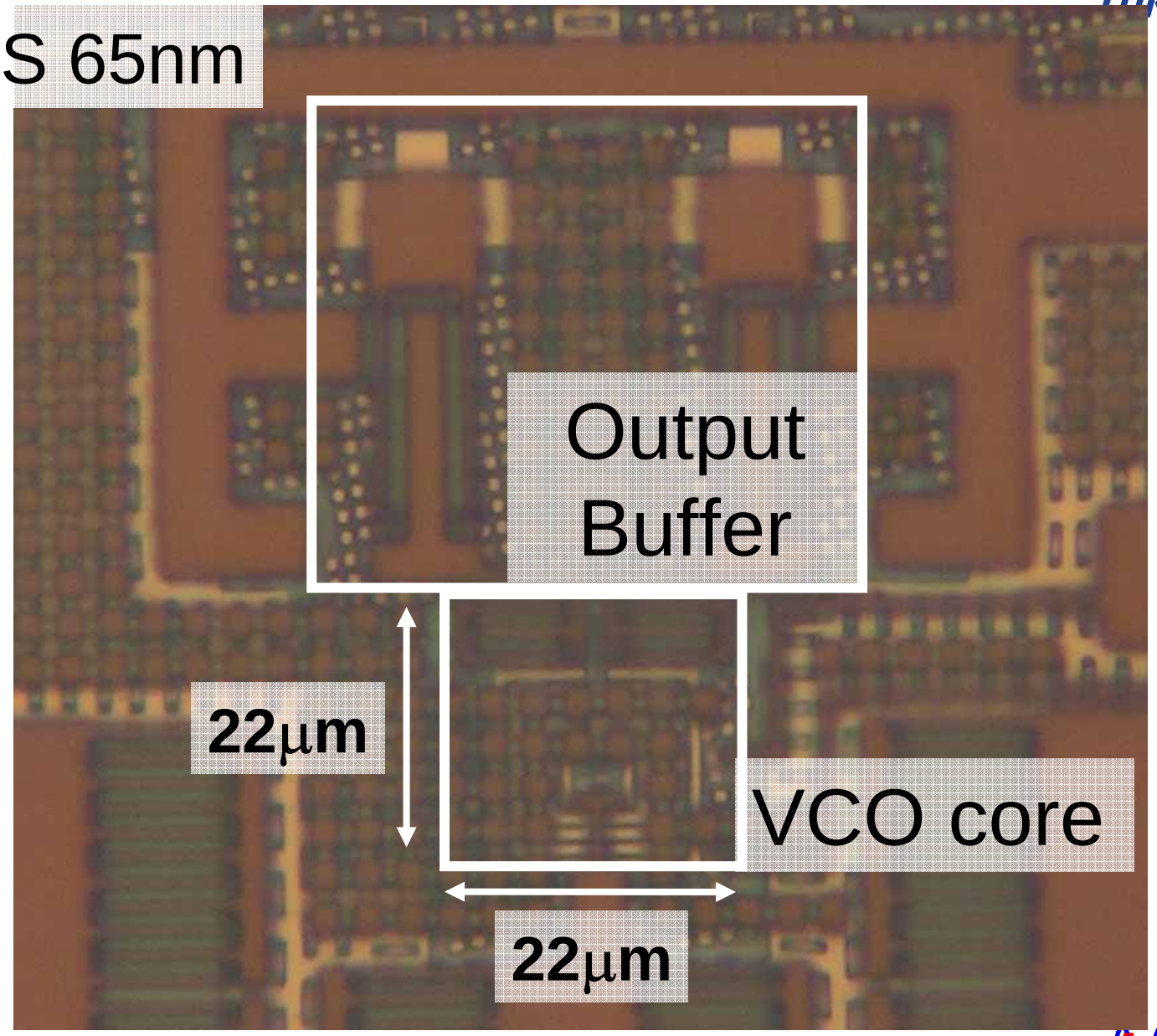
CMOS 65nm



Chip Micrograph(2)

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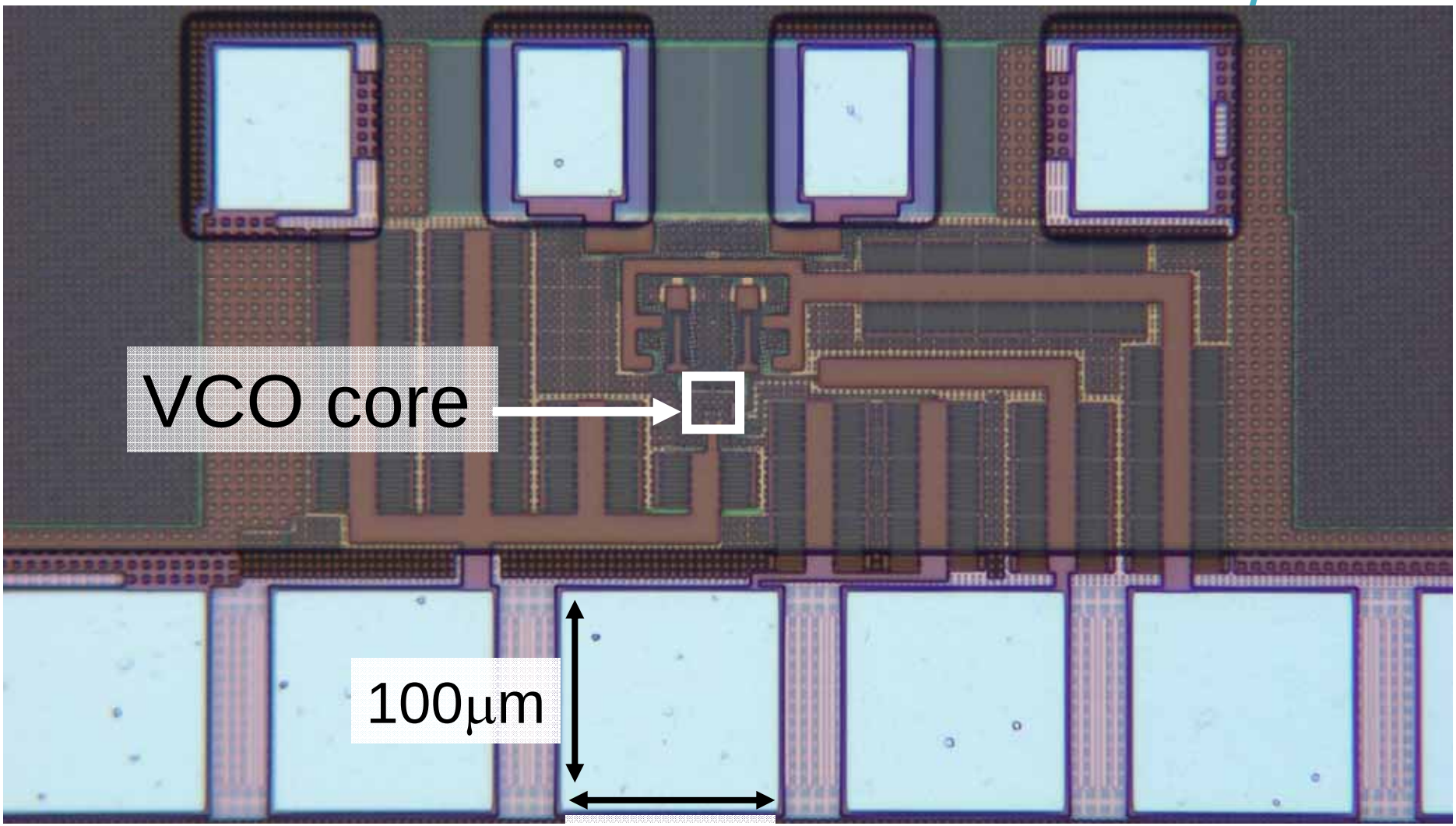
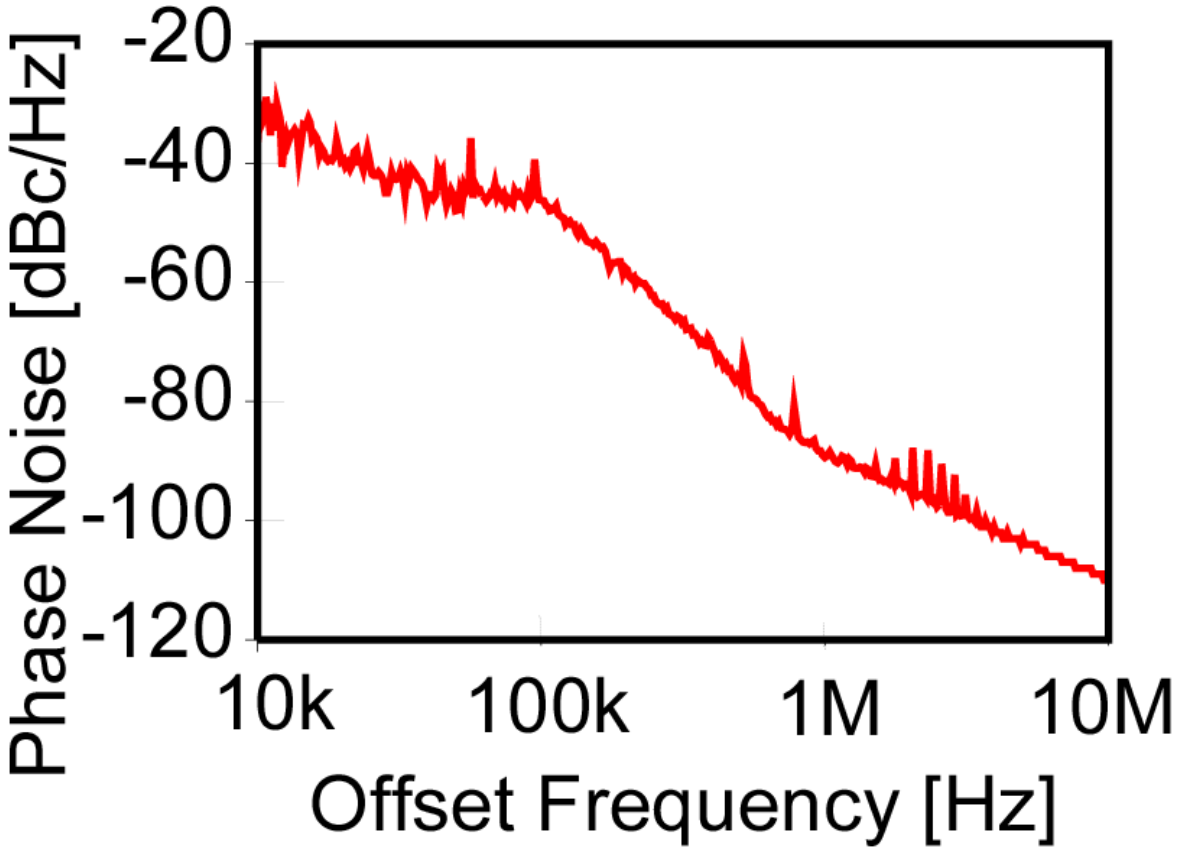


Measurement Result



VDD	0.6V
Freq.	21GHz
power consumption	1.92mW
PN[dBc/Hz]	-89.4@1MHz -110@10MHz
Tech.	65nm
FoMA [dBc/Hz]	206

$$FoMA = -\left(\mathcal{L}\{\Delta f\} - 20\log\left(\frac{f_o}{\Delta f}\right) + 10\log\left(\frac{P_{\mathrm{DC}}}{1\mathrm{mW}}\right)\right) - 10\log\left(\frac{\mathrm{Area}}{1\mathrm{mm}^2}\right) \text{ [5]}$$

[5]Shih-An Yu, *et al.*, *IEEE TCAS-II* 2009

Performance Summary

	This Work	[6]	[7]	[3]
Area [μm^2]	484	2597	2400	290000
Power [mW]	1.92	2.8	9.8	0.16
PN	-110@10MHz	-103@1MHz	-101@600kHz	-109@1MHz
Freq.	21GHz	5GHz (20GHz/4)	0.9GHz	4.5GHz
VDD [V]	0.6	1	3.3	0.3
Tech. [nm]	65	90	350	180
FoM	173	173	154	190
FoMA	206	199	182	195
Type	LC(3D-inductor)	LC(3D-inductor) +Div.	Ring	LC

[6]A.Tanabe, *et al., RFIC* 2009 [7]I.Hwang, *et al., JSSC* 2004
[3]K.Okada, *et al., VLSIC* 2009

Summary

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- A very compact LC-VCO with a stacked-spiral inductor and the core-circuit being placed beneath the inductor is proposed.
- To reduce coupling, interconnections are slit shaped and orthogonalized with the coil trace.
- This VCO achieves a chip area of 484μm^2 equaling ring-oscillator and FoMA of 206dBc/Hz.

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Thank you!!

Matsuzawa & Okada Lab.