A 58-63.6GHz Quadrature PLL Frequency Synthesizer in 65nm CMOS

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***Abstract*—This paper proposes a 60GHz quadrature PLL frequency synthesizer that has a tuning range capable of covering the whole band specified by the IEEE802.15.3c with exceptional phase noise. The synthesizer is constructed using a 20GHz PLL that is coupled with a frequency tripler to generate the 60GHz signal. The 20GHz PLL generates a signal with a phase noise as low as −106dBc/Hz using tail feedback to improve the phase noise. The proposed 60GHz ILO uses a combination of parallel and tail injection to enhance the locking range by reducing the Injection Locked Oscillator (ILO) current at the moment of injection. Both the 20GHz PLL and the ILO were fabricated using a 65nm CMOS process and measurement results show a phase noise of −96dBc/Hz at 60GHz while consuming 77.5mW from a 1.2V supply. To to author's knowledge this phase noise is about 20dB better then recently reported QPLL and about 10dB compared to differential PLL operating at similar frequency.**

I. Introduction

Recently, the demand for high data rate wireless communication is increasing to serve applications like high definition video and multimedia applications. One way to serve this demand was by introducing more complex modulation schemes to increase the throughput. However, phase noise, power consumption and affordability puts an upper limit on the performance gain achievable. To overcome these limitations, one of the promising solutions is to utilize the 60GHz ISM band for high-speed short-range data communication. As defined by the IEEE802.15.3c standard, the band covers the range from 57-66GHz and has four channels each with a bandwidth of 2.16GHz. This bandwidth enables wireless Gbps transfer rates which makes this band very appealing as a next generation wireless standard. Moreover, using an affordable process like CMOS further enhances the advantages of this band specially since, due to miniaturization, CMOS transistors can operate up to a few hundred GHz. Still, a CMOS process has many challenges like higher process variations, lower mobility and lower breakdown voltage which limits the performance and requires novel designs to overcome these obstacles.

The LO frequency synthesizer is the heart of most modern transceivers and plays an important role in setting the final performance. In a synthesizer, the VCO phase noise sets the limit on the usable modulation scheme and transfer rate. Therefore, lowering the phase noise will enable more complex modulation schemes and thus faster data rate. However, to lower the phase noise a higher Q is required but due to large tuning range for the 60GHz band a high Frequency Tuning Range (FTR) is required. Therefore, a wide range of capacitance is needed, which lowers the quality factor since capacitors have significantly lower Q at 60GHz compared to lower frequencies. One solution could be to use two VCOs [1] but due to poor quality factor of the capacitors, the resulting phase noise is not greatly improved compared to a single VCO structure. Another can use a push-push oscillator were frequency is generated at half [2] [3] or one third [4] and then combined to cancel the first in case of a VCO running at half the required frequency or both the first and second in case of a VCO running at one third the frequency. This paper uses a third way in which the frequency is generated at a subharmonic and a frequency multiplier is used to lock to the third harmonic and generate the desired signal in which the phase noise of the up-converted signal depends on the injected signal which can be generated with a low phase noise. In the proposed synthesizer, The VCO employs tail feedback to improve phase noise [5] and the Injection Locked Oscillator (ILO) uses both parallel and tail injection to enhance locking.

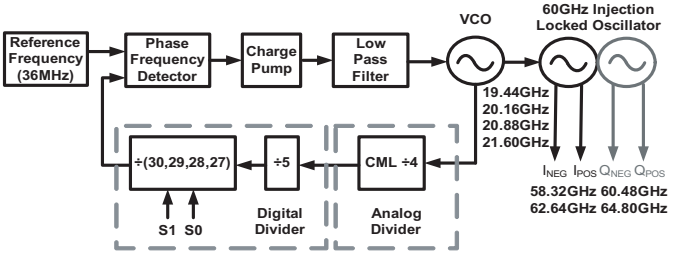

Fig. 1. The proposed 60GHz synthesizer architecture

II. 60GHz LO Synthesizer Architecture

There are many LO synthesizer architectures available when it comes to a direct conversion receiver for a 60GHz transceiver. Each architecture has its advantages in terms of complexity, area, attainable phase noise, and power consumption. Mainly, three main approaches to design the LO synthesizer for a direct 60GHz transceiver are used which are using a VCO running at the fundamental frequency [1] [6] [7], a push-push VCO to generate the frequency at half or one third and then combining the generated signals to cancel the first or first and second harmonic respectively and finally using a subharmonic VCO with a frequency multiplier.

A. Fundamental

Designing a VCO running at 60GHz while having a wide tuning range and low phase noise is as mentioned before very challenging because of the low Q of the capacitors at such high frequency which severely degrades the phase noise and thus data-rate. Also, tuning range is needed to be made much wider then the required one since the VCO is extremely sensitive to parasitics and it is highly likely for the frequency to drift by a considerable amount due to layout parasitics. Finally, designing a divider to operate at this high frequency would be difficult and would result in a high power consumption specially for an inductorless one.

B. Push-Push

Although a push-push oscillator is running at a half [2] [3] or [4] one third of the required frequency and thus require half or one third the required tuning range, its output power is largely compromised due to cancellation of the fundamental harmonic and the use of the second or third harmonic instead. This would require additional amplifications in the buffers that will increase the power consumption. Furthermore, IQ generation is difficult and will require additional circuitry which will introduce a significant loss and mismatch would need to be given extra care to reduce the IQ mismatch as much as possible.

C. Subharmonic VCO and Injection Locked Oscillator (ILO)

The third way would be to use a subharmonic VCO and an injection locked oscillator [8] to super-harmonically lock to the VCO and generate the LO signal. This way would benefit from the lower frequency generation and narrower tuning range but the fundamental would not be cancelled for generating the higher harmonic instead it will be injected to the ILO. The ILO on the other hand can be designed to have a very wide tuning range without paying much attention to lowering the phase noise since the output phase noise is determined by the locking signal's phase noise. The drawback would be the amount of power that the multiplier needs to lock. The proposed system is based on this concept as show in Fig. 1 in which the system consists of a 20GHz PLL that is injection locked to an ILO frequency tripler.

III. 20GHz PLL Synthesizer

As shown in Fig. 1 the system uses a Charge Pump PLL to generate the four required channels as specified by the IEEE standard. Careful matching in both simulation and layout was given to the PFD and charge pump since they contribute a significant amount of phase noise and spurious to the output of the PLL where it can be seen from the measurement results later that spurious were significantly minimized. As for the LPF, a conventional second order filter was used followed by a first order low pass filter to further reduce the ripples however its pole was made much further then the loop main ones in order not to affect the stability. The VCO is shown in Fig. 2 and is designed as a NMOS LC oscillator with three capacitor banks. The capacitor banks utilize switched varactors since they possess higher Q compared to MIM switched capacitors and inverters where used to bias them and to reduce the number of input pins. In order to improve the phase noise, feedback from the output to the tail current source is used since it was shown to improve phase noise [5]. The achieved VCO phase noise can go as low as −107dBc/Hz@20GHz. The divider chain uses two-stage divide-by-2 static CML dividers as high frequency dividers coupled with logic dividers to further lower the frequency down to the 36MHz reference signal. Channel selection was made at the last logic divider using the two signals S0 and S1. Also, to provide enough power for the ILO to lock to the PLL signal, matched output buffers were added and the output impedance was made about 50 Ω since the input impedance of the ILO at 20GHz is close to this value. Due to underestimation of the layout parasitics, the frequency range shifted to a lower value compared to the simulation. As shown in Fig. 3 the tuning range of the VCO ranges from 17.9 to 21.2GHz for a tuning voltage between 0 and 1.2. Moreover, the tuning range in a PLL would be smaller since the charge pump is unable to provide the required current when the voltage output of the LPF is around 0 and 1.2V. Simulation show that the PLL tuning range is only between 0.2 and 1V. This made the PLL only lock to three channels instead of the four required channels and the lower range of the VCO became unusable.

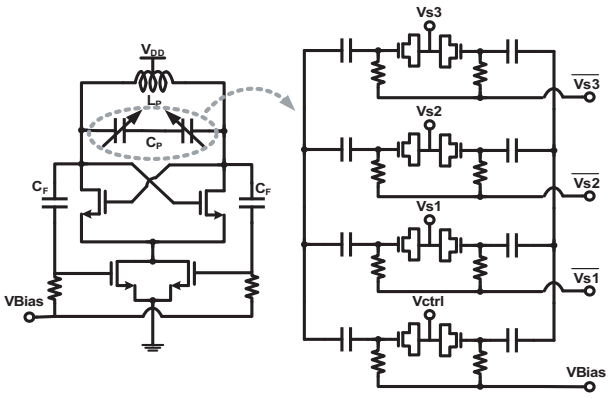

Fig. 2. 20GHz VCO architecture

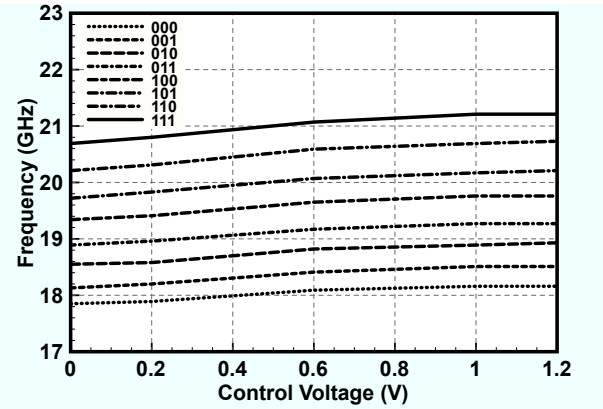

Fig. 3. 20GHz VCO tuning range

IV. The Proposed 60GHz Injection Locked Ocillator

The ILO is needed to lock to the third harmonic of the oscillator to generate the four 60GHz channels. It is designed to oscillate at 60GHz and to have a wide tuning range while providing a quadrature output as shown in Fig. 4(a). It uses two coupled LC oscillators with tail transistor coupling to generate the quadrature output. The inductor is simulated using HFSS to have a Q of 10 and an inductance of 70pH. It was modeled using S-parameters obtained from the measurement of the inductor TEG. Fig. 4(b) shows capacitive tuning that is implemented using a switched varactor for discrete tuning and another varactor for continuous tuning in addition to bias current tuning. 20GHz Injection is provided through two transistors connected in parallel to the output since this topology is most suited for triple injection locking in terms of the third harmonic locking. The proposed ILO introduces another path for the injection through another tail transistor to further enhance the locking range by lowering the current at the branch were the injection occurs. As can be seen from the following equation [9]:

$$\omega_0 - \omega_{inj} = \frac{\omega_o}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \quad (1)$$

By minimizing the I_{osc} in the previous equation, the locking range can be improved. This is achieved by injecting the opposite phase of the differential injecting signal at the tail during injection. Fig. 4(a) shows one of the two oscillators along with the parallel and tail injection transistors. Measurement results indicate a locking range of about 100MHz at 20.16GHz along with a tuning range from 58 to 65.4GHz which is enough to cover all the four required channels.

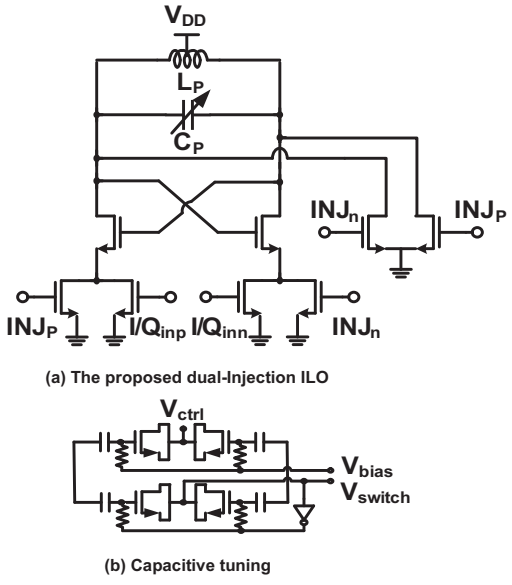

Fig. 4. The proposed 60GHz ILO architecture

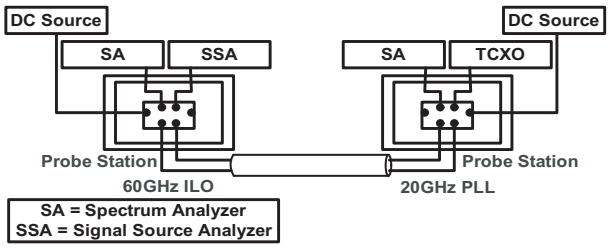

Fig. 5. Measurement setup

V. Measurement Results

Measurements were carried out individually for the 20GHz PLL and the 60GHz ILO to confirm their operation using on-chip probes. For the 20GHz PLL, three out of the four channels required were obtained successfully with a phase noise ranging from −105.8 to −106.2dBc/Hz while consuming 65.5mW which includes the output buffers used to connect to the 60GHz ILO. Underestimated parasitics caused the frequency of the VCO to drop slightly to 21.2GHz which prevented the PLL from locking to the fourth channel at 21.6GHz. The ILO on the other hand has a free running phase noise of −85dBc/Hz with a power consumption that ranges from 17.3mW for the middle channel and up to 63.4mW for the lowest frequency channel. The increase in the power consumption is caused by lower Q factor around 58GHz. The summary of the measurement results for the individual chips are given in Table I.

Fig. 5 shows the measurement setup for the whole synthesizer in which two probe stations were used with cables in between to connect the 20GHz PLL and the 60GHz ILO. The resultant phase noise varies between −93.1 to −96dBc/Hz which is to the knowledge of the author the best phase noise achieved at 60GHz using a PLL synthesizer. The phase noise of the channel at 60.48GHz is shown in Fig. 6 which shows the 20GHz PLL phase noise signal together with the freerun and the locked phase noise of the ILO indicating about 10dB difference between the 20GHz PLL signal and the ILO output phase noise. Due to the loss of the cables (about −7dB) connecting both chips being uncompensated, input power to the ILO was limited and the phase noise worsen at a frequency

TABLE I
Synthesizer Performance Summary

	20GHz PLL	**60GHz ILO**
Technology	65nm CMOS	
Supply [V]	1.2	
Frequency [GHz]	17.9 ~ 21.2	58 ~ 65.4
Power Consumption [mW]	65.5	52.8 (58.32GHz) 14.4 (60.48GHz) 18 (62.64GHz)
Phase Noise@1MHz [dBc/Hz]	−106.2 (19.44GHz) −106 (20.16GHz) −105.8 (20.88GHz)	−85 (Freerun)
Ref. Spur Level [dBc]	−67 ~ −58	-
Division Ration	540, 560, 580, 600	1620, 1680, 1740, 1800
Output Type	Differential	Quadrature

TABLE II
PERFORMANCE COMPARISON WITH OTHER STATE-OF-THE-ART 60GHz PLLs

	This Work	**[1]**	**[10]**	**[11]**	**[6]**	**[7]**	**[12]**
CMOS Tech	65nm	45nm	130nm	130nm	90nm	90nm	130nm
Supply [V]	1.2	1.1	1.2	1.5	1.2	1.2	1.5/0.8
Ref. Frequency [MHz]	36	100	251.3	203.2	234	60	44.8~49.3
Frequency [GHz]	58 ~ 63	57 ~ 66	64.3 ~ 66.2	50.8 ~ 53	58 ~ 60.4	61 ~ 63	46 ~ 50.5
Phase Noise@1MHz [dBc/Hz]	**−96 (60.48GHz)**	−75	−84.1 6	−85.07	−85.1	−80	−72
Power Consumption [mW]	**77.5 (60.48GHz)**	78	72	87	80	78	57
Ref. Spur Level [dBc]	−67 ~ −58@20GHz	−42	−15.2	−59.88	−50.75	−49	−27
Division Ration	1620, 1680, 1740, 1800	512-8184	128	256	256/258	1024	1024
Output Type	**Quadrature**	Quadrature	Differential	Differential	Differential	Differential	Differential

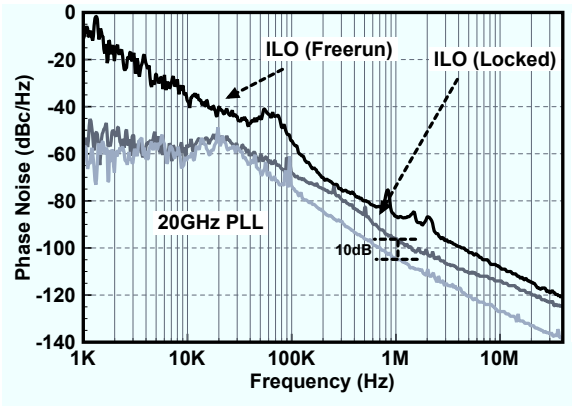

Fig. 6. Measured phase noise at 20.16GHz and 60.48GHz

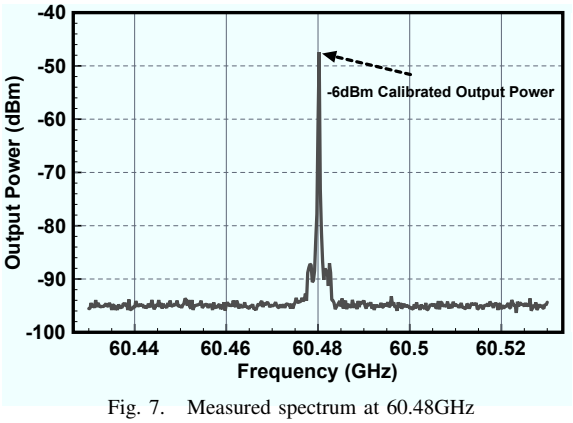

Fig. 7. Measured spectrum at 60.48GHz

above 4MHz. Output spectrum at the same frequency is shown in Fig. 7, which indicates that the output spurious is lower then −47dBc and cannot be exactly measured due measurement equipment limitation. Furthermore, the output power indicated does not account for the external passive down-conversion mixer and cables. Micrograph of both chips are shown in Fig. 8 in which the 20GHz PLL occupies an area of 1400μm×1200μm and the ILO has an area of 1000μm×800μm. Finally, Table II gives a comparison between the presented work and recently published synthesizer papers operating around the same frequency.

VI. CONCLUSION

In this paper, a frequency synthesizer for the 60GHz frequency band using a 20GHz PLL and a 60GHz ILO frequency tripler was presented. It achieves a phase noise as low as -96dBc/Hz at 60GHz while consuming 77.5mW from a 1.2V supply which is to the author's knowledge the best phase noise

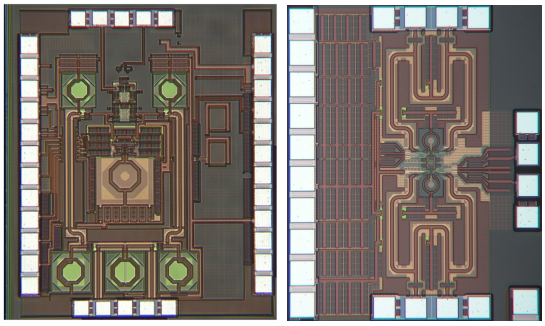

Fig. 8. 20GHz PLL (on the left) and ILO (on the right) chip photos

achieved that is 20dB better then recently reported QPLL at this frequency band using a CMOS process.

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REFERENCES

[1] K. Scheir, G. Vandersteen, Y. Rolain, and P. Wambacq, "A 57-to-66GHz Quadrature PLL in 45nm Digital CMOS," in *ISSCC*, 2009, pp. 494–495,495a.

[2] O. Lee, J.-G. Kim, K. Lim, J. Laskar, and S. Hong, "A 60-GHz push-push InGaP HBT VCO with Dynamic Frequency Divider," *MWCL*, vol. 15, no. 10, pp. 679–681, Oct. 2005.

[3] T. Nakamura, T. Masuda, K. Washio, and H. Kondoh, "A 59GHz push-push VCO with 13.9GHz Tuning Range using Loop-Ground Transmission Line for a Full-Band 60GHz Transceiver," in *ISSCC*, 2009, pp. 496–497.

[4] B. Catli and M. Hella, "A 60 GHz CMOS Combined mm-wave VCO/Divider with 10-GHz Tuning Range," in *CICC*, 2009, pp. 665–668.

[5] S. Hara, K. Okada, and A. Matsuzawa, "A 9.3MHz to 5.7GHz Tunable LC-based VCO Using a Divide-by-N Injection-Locked Frequency Divider," in *ASSCC*, 2009, pp. 81–84.

[6] C. Lee and S. L. Liu, "A 58-to-60.4GHz Frequency Synthesizer in 90nm CMOS," in *ISSCC*, 2007, pp. 196–596.

[7] H. Hoshino, R. Tachibana, T. Mitomo, N. Ono, Y. Yoshihara, and R. Fujimoto, "A 60-GHz Phase-Locked Loop with Inductor-less Prescaler in 90-nm CMOS," in *ESSCIRC*, 2007, pp. 472–475.

[8] W. Chan and J. Long, "A 56-65 GHz Injection-Locked Frequency Tripler With Quadrature Outputs in 90-nm CMOS," *JSSC*, vol. 43, no. 12, pp. 2739–2746, Dec. 2008.

[9] B. Razavi, "A Study of Injection Locking and Pulling in Oscillators," *JSSC*, vol. 39, no. 9, pp. 1415–1424, Sept. 2004.

[10] K.-H. Tsai, J.-H. Wu, and S.-I. Liu, "A Digitally Calibrated 64.3-66.2GHz Phase-Locked Loop," in *RFIC*, June 2008, pp. 307–310.

[11] C. Lee, L.-C. Cho, J.-H. Wu, and S.-I. Liu, "A 50.8–53GHz Clock Generator Using a Harmonic-Locked PD in 0.13um CMOS," *TCASII*, vol. 55, no. 5, pp. 404–408, May 2008.

[12] C. Cao, Y. Ding, and K. O, "A 50-GHz Phase-Locked Loop in 130-nm CMOS," in *CICC*, 2006, pp. 21–24.