A 0.5-V, 0.05-to-3.2 GHz, 4.1-to-6.4 GHz LC-VCO using E-TSPC frequency divider with forward body bias for sub-picosecond-jitter clock generation

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***Abstract*—This paper investigates the adoption of LC-VCO to replace ring VCO for ultra-low-voltage sub-picosecond jitter clock generation in future 0.5-V LSI and power aware LSI. A 0.5-V LC-VCO using E-TSPC frequency divider with forward body bias technique is proposed and implemented. Significant performances, in terms of 0.6-ps jitter, 50MHz-to-6.4GHz frequency tuning range with 2 bands and sub-1mW P_{DC}, have been achieved in the measurement results.**

I. INTRODUCTION

As device scaling of the feature size in the CMOS technology continues, the increasing need in the reduction of power dissipation on electronics devices, especially on power aware LSI such as implantable medical devices and portable mobile devices, has become one of the main design concerns in today's radio frequency integrated circuits (RFICs). To reduce the power dissipation of a system, ultra-low-voltage operation has become one possible solution, especially for digital circuits where supply voltage has been reduced below the threshold voltage [1]. However, it is difficult to achieve ultra low voltage operation in analog and RF circuits since the signal-to-noise ratio (SNR) and system performances would decrease significantly, under the restrictions of signal amplitude. This is especially true for clock generator in high performance ADC/DAC, digital integrated circuits and microprocessors.

Conventionally, in the area of clock generators, ring VCOs are widely adopted due to their low power consumption, small chip area and wide tuning range compared with LC-VCOs. However, along with the scaling of the supply voltage, a practical design issue arises for ring VCOs. As explained in table 1, admittedly, for $V_{dd} = 1.2V$, the performance of ring VCOs is reasonable in certain specifications. Nevertheless, along with V_{DD} reducing to as low as 0.5-V, ring VCOs become infeasible due to too large jitter and unbelievable power consumption, which highlight the necessity of adopting LC-VCOs as clock generators in future 0.5-V LSI and power aware LSI application [2]. Unfortunately, as the power supply dropped to 0.5-V, conventional LC-VCOs suffer from fair power consumption, large chip area, and especially, their limited tuning range [5][6][7][8] which is key issue for clock generation circuits to deal with different computing complexity applications and compensate the variations in supply voltage, temperature and process (PVT). Based on the previous analysis, there has been pressing demand for 0.5-V LC-VCOs with low jitter, low power consumption, small chip area and wide frequency range for clock generation circuits.

In this paper, a 0.5-V, 0.05-to-3.2 GHz and 4.1-to-6.4 GHz tuning range, 0.6-ps jitter, 0.15mm^2, and sub-1mW LC-VCO using E-TSPC frequency divider with forward body bias for sub-picosecond jitter clock generation is proposed and implemented. Besides the optimization of jitter, power consumption, chip area and frequency range for 0.5-V clock generation circuits, this paper also addresses design methodologies overcoming the most challenging issues raised by voltage scaling. This paper is organized as follows. In section II, the analysis of VCO architecture and design of circuits are presented. The following section describes the measurement results of the VCO. Finally, conclusion is summarized in Section IV.

II. ANALYSIS AND DESIGN OF VCO ARCHITECTURE

Inherently, VCOs for clock generation in digital integrated circuits or microprocessors have to deal with different computing complexity applications, such as audio, video, image, text, etc. Thus, clock generators are demanded to generate wide frequency range from several MHz to multi-GHz. Besides, due to the compensation to the variations in supply voltage, temperature and process (PVT), VCOs are also required to ensure a wide operation frequency even if the target frequency range is narrow [3]. However, it is considerably difficult for typical LC-VCOs to achieve wide frequency range under ultra-low-voltage operation.

In this paper, a 0.5-V VCO, which is capable of operating in two widely used bands, is investigated in depth for clock generation. As shown in Fig.1 the proposed wide band circuit is composed of a core VCO, divider stage 1 and stage 2. The stage1 is a switchable divider whose divide ratio can be control to 2 and 3. The stage 2 consists of 6 successive asynchronous dividers with divide ratio of 2. Frequency

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TABLE I SCALING OF JITTER BETWEEN LC AND RING VCO

V_{DD}	Type	P_{DC}	Phase Noise +10dB margin @ 1MHz	Peak-to-Peak Jitter
1.2V	LC	1mW	-121.6 dBc/Hz	0.16ps
	Ring	1mW	-91.6 dBc/Hz	5.0ps
0.5V	LC	0.17mW	-114.0 dBc/Hz	0.38ps
	Ring	0.17mW	-84.0 dBc/Hz	**12.0ps**
		174mW	-114.0 dBc/Hz	0.38ps
Assumption for jitter comparison: Q=10, γ_n= γ_p=2/3, V_{th}=V_{dd}/4, and M=3				
Q: unload quality factor of resonator at f_o γ_n, γ_p: MOS channel noise factor M: stage number of ring VCOs				

planning of the proposed architecture is also illustrated in Fig.1. The fundamental frequency f_0 is output of core VCO, which can be tuned from 4.1-to-6.4GHz. $1/2f_0$ and $1/3f_0$ are generated by the switchable divider stage 1, which means, the continuous tuning range of 2.05-to-3.2GHz and 1.37-to-2.13GHz can be obtained with the divide-by-2 and divide-by-3 operation, respectively. Lower frequency range from 0.05-to-1.37GHz can be generated by the divider stage 2. As a result, the architecture yields two bands distributed from 0.05-to-3.2GHz (band I) and 4.1-to-6.4GHz (band II), minimizing power consumption and undesired sidebands.

A. 0.5-V divider design

This paper proposes E-TSPC frequency dividers using forward body bias technique for 0.5-V divider stage design.

Divider stage 1 is regarded as one of the most crucial and challenging building block in this proposed VCO architecture. Three strict requirements for divider stage 1 make it challenging to design such kind of divider:

1.) Divider stage 1 needs to be able to operate under the power supply as low as 0.5-V with minimizing power consumption.
2.) Divider stage 1 needs to operate as high as output frequency of core VCO (more than 7GHz).
3.) Divider stage 1 needs to possess wide operation frequency range as large as the tuning range of core-VCO (more than 3GHz).

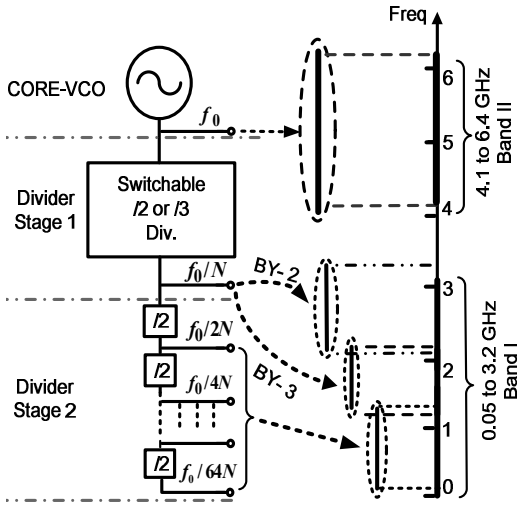

Fig.1 Frequency plan and proposed architecture

Conventional high-speed frequency dividers, which could operate at multi-gigahertz frequencies, are mainly based on current mode logic (CML), injection-locked topology and true single phase clock (TSPC) logic/extended true single phase clock (E-TSPC) logic. Typically, at high power supply, CML dividers and injection-locked divider can operate as high as 20GHz. However, as the supply voltage drops to 0.5-V, both the two implementation styles could not fulfill the requirements mentioned previously. For CML latch, since all FETs must be biased in the saturation region, the performance degrades significantly at ultra low voltage operation, or even fails to function at high frequency up to several GHz. For injection-locked topology, the locking range could not reach the requirement at the power supply of 0.5-V. Consequently, the exclusive hope for 0.5-V divider with high maximum working frequency and wide working frequency is TSPC/E-TSPC logic.

Conventionally, an E-TSPC [4] logic uses two transistors in each stage while a TSPC logic employs three transistors. Thus, E-TSPC logic with supply voltage above 1-V, the avoiding of stacked MOS structure allows higher operation frequency, which serve as better solution for low-voltage operation compared with TSPC logic. However, as the supply voltage drops to 0.5-V, the E-TSPC logic may do not work. This is because a PMOS device can only be turned on when an input signal is low enough ($V_{in} < V_{dd} - |V_{tp}|$). Similarly, a NMOS can only be turned on when a input signal exceed its threshold voltage ($V_{in} > V_{tn}$). As a result, there would be a dead-zone region ($V_{tn} > V_{in} > V_{dd} - |V_{tp}|$) if the voltage supply is not high enough ($V_{dd} < V_{tn} + |V_{tp}|$). In this dead-zone region, E-TSPC logic would fail to function. Thus, the minimum supply voltage for E-TSPC should be larger than $V_{tn} + |V_{tp}|$. As an example, for standard 90nm CMOS process, V_{tn}=0.35-V, $|V_{tp}|$=0.33-V, and the minimum supply voltage is 0.68-V. In addition, the minimum supply voltage can only provide the condition which E-TSPC logic could work. Higher power supply or lower threshold voltage is necessary to obtain maximum operation frequency (f_{max}).

Based on analysis above, it can be naturally to employ E-TSPC logic using forward body bias technique (FBB) to design a divide-by-2/3 circuit as divider stage 1 and divider-by-2 circuit as one cell of divider stage 2. The schematic of the divider stage 1 and divider stage 2 based on E-TSPC logic are shown in Fig.2 and Fig.3, respectively. A 0.5-V FBB technique is applied to all NMOS to have a V_{tn} induction of 110-mV. Similarity, A 0-V forward body bias is applied to all PMOS to have a $|V_{tp}|$ induction of 100-mV. No additional biasing circuits are needed since the body of NMOS is directly connected to power supply and the body of PMOS is directly connected to ground. Maximum operation frequency should be improved by applying forward body bias technique.

B. 0.5-V core-VCO design

This paper employs an LC-VCO using forward body bias technique and gate-biasing technique for 0.5-V core-VCO design.

There are four main considerations for 0.5-V core-VCO design. First of all, a stacked NMOS-PMOS-coupled LC-VCO is adopted as core-VCO, as shown in Fig.4. Low phase noise with high power efficiency can be achieved in the core-VCO since both NMOS and PMOS cross-coupled pairs provide negative resistance. In addition, forward body bias technique is employed to decrease the threshold for NMOS and PMOS of core-VCO and switch transistors of capacitor bank. For NMOS and PMOS in the core-VCO, the decreasing of threshold voltage directly leads to the increasing of transconductance of the cross-coupled transistors. As a result, the core-VCO can meet the startup constraint at the power supply of 0.5-V. For switch transistors of capacitor bank, the decreasing of threshold voltage brings the increasing of V_{gs}. Thus, the turn-on resistance of switch transistors would be reduced, which in turn, decrease the parasitic capacitance and enlarge the tuning range. The third consideration is gate-bias technique. As depicted in Fig.4, gate bias voltage V_{b1} and V_{b2} are added to gate nodes of cross-coupled transistors through large resistance, which guarantee the transistors operated at moderate or strong inversion region. Finally, tail-feedback technique [10] is applied to the core-VCO to improve the phase noise with the reduction of 1/f noise.

III. Measurement Results

Without applying FBB technique, at the power supply of 0.5-V, the divide-by-2/3 circuit fails to response according to simulation results. As the power supply increasing to 0.7-V, the divide-by-2/3 circuit starts to work and the maximum operation frequency is 4GHz. By applying FBB technique, at the power of 0.5-V, measurement results show that the divide-by-2/3 circuit works properly and the maximum operation frequency is 7.2GHz, which could meet the requirement of divider stage 1. Fig.5 shows the measured input sensitivity of divider stage 1 in divide-by-2 operation. The effects of FBB technique on performance of divider stage 1 are summarized in table II. According to the literature survey, it is the first time to implement high frequency divider under the power supply of 0.5-V.

Along with frequency range of 4.1-to-6.4GHz (band II) from output of core-VCO, 0.05-to-3.2GHz (band I) continuous frequency tuning is obtained by the core VCO and frequency-extended circuits. For band I, the frequency tuning range is significantly as large as 194%. The total power consumption is 0.75-to-1mW depending on output frequency. Phase-noise characteristics for each divide ratio of stage 1 are illustrated in Fig.7. The performance of the VCO is listed in Table III.

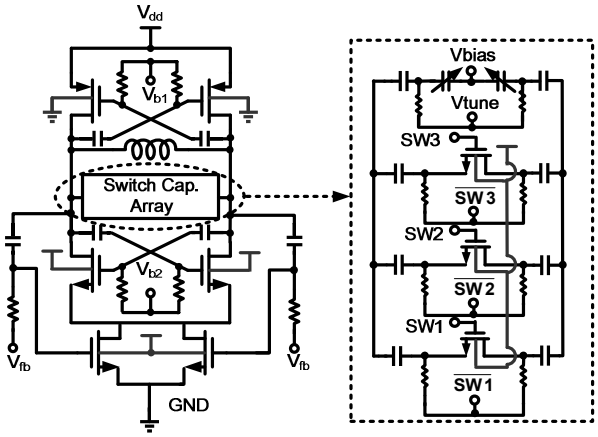

Fig.4 Schematic of 0.5-V core-VCO with FBB and gate-biasing

TABLE II FBB EFFECTS ON DIVIDER STAGE 1

Parameter	V_{dd}=0.5-V (w/o FBB)	V_{dd}=0.7-V (w/o FBB)	V_{dd}=0.5-V (w/ FBB)
Maximum operation freq.	not work (sim.)	4GHz (sim.)	7.2GHz (meas.)
Power consumption	not work (sim.)	0.21mW (sim.)	0.25mW (meas.)

TABLE III SUMMARY OF VCO PERFORMANCE

Technology	CMOS 90nm
Supply Voltage	0.5-V
P_{DC} of core VCO	0.45-to-0.65mW
P_{DC} of divider stage	0.3-to-0.35mW
Total P_{DC}	0.75 - 1.0mW
Peak-to-peak jitter	0.6-ps
FOM	-180 dBc/Hz
FOM_T	-204 dBc/Hz
Tuning range	Band I: 0.05GHz – 3.2GHz Band II: 4.1GHz – 6.4GHz
Core area	0.15mm^2

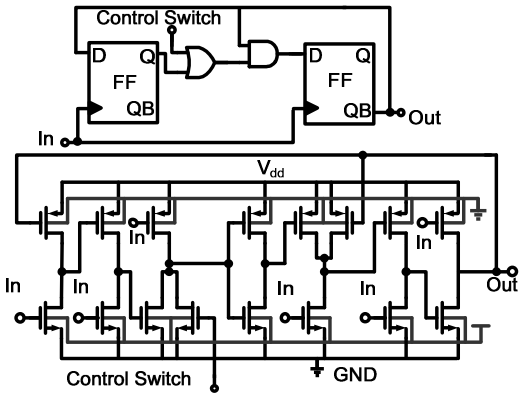

Fig.2 The proposed 0.5-V divide-by-2/3 divider using FBB technique

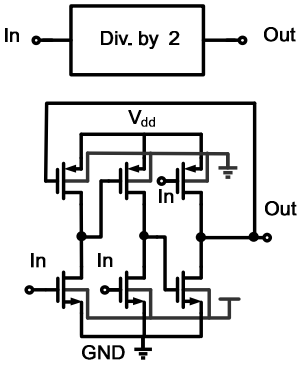

Fig.3 The proposed 0.5-V divide-by-2 divider using FBB technique

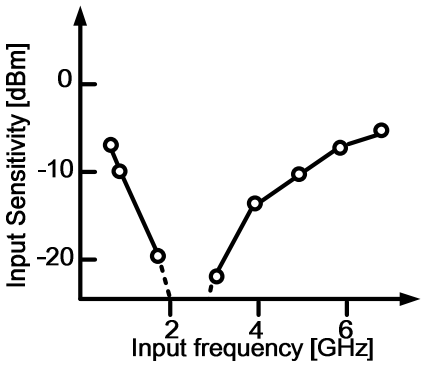

Fig.5 Measured input sensitivity of divider stage 1

FOM_T [9], which allows comparison of frequency tuning range as well as phase noise between other VCOs, is utilized. FOM_T is defined by the following equation.

$$FOM_T = L(f_{offset}) - 20\log\left(\frac{f_0}{f_{offset}} \cdot \frac{FTR}{10}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right) \quad (1)$$

where $L(f_{offset})$ is phase noise, f_{offset} is offset frequency, f_0 is center frequency and P_{DC} is power consumption. FTR is frequency tuning range, which is defined as $(f_{max} - f_{min})/((f_{max} + f_{min})/2)$ in percent figures. Table IV summarizes the comparison to other published ultra low voltage and ultra low power VCO with performances. Fig.8 compares FOM_T and frequency tuning range of ultra low voltage and ultra low power LC-VCO reported in literature [5][6][7][8]. To the best knowledge of authors', this study has demonstrated the first wide tuning range and the best FOM_T (-204 dBc/Hz), simultaneously, for sub-picosecond jitter clock generation.

IV. Conclusion

As addressed in this paper, the inevitable necessity of LC VCOs to replace ring VCOs for sub-picosecond jitter clock generation is investigated. Future clock generator with less jitter, lower power consumption, less chip area and wider tuning range are required in the realization of 0.5-V LSI and power aware LSI. Therefore investigations as present in this paper will become essential during the design of such clock generators.

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TABLE IV COMPARISON OF PUBLISHED ULTRA-LOW-VOLTAGE VCOs

-	Unit	[5]	[6]	[7]	[8]		This work	
Process	-	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS		90nm CMOS	
V_{DD}	V	0.6	0.5	0.9	0.5	0.43	0.5	
Frequency	GHz	5.3~6	3.65~3.76	2.17~2.73	2.15~2.62		**4.1 ~ 6.4**	**0.05 ~ 3.2**
DC power	mW	3.0	0.57	2.7	0.365	0.233	0.45~0.65	0.75~1.0
Chip area	mm^2	0.5	0.23	N.A	0.31		0.15	
Tuning range	MHz	700	90	560	470		**2300**	**3150**
FTR	%	8.1	3	22.8	20		44	194
FOM_T	dBc/Hz	-188	-183	-193	-196	-197	**-198**	**-204**

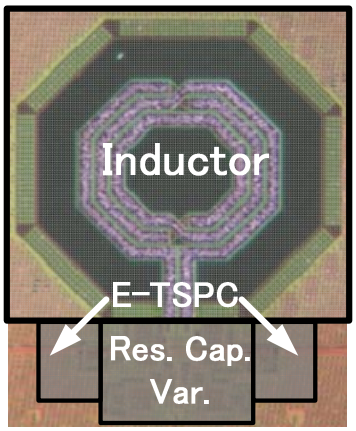

Fig.6 Chip microphotograph

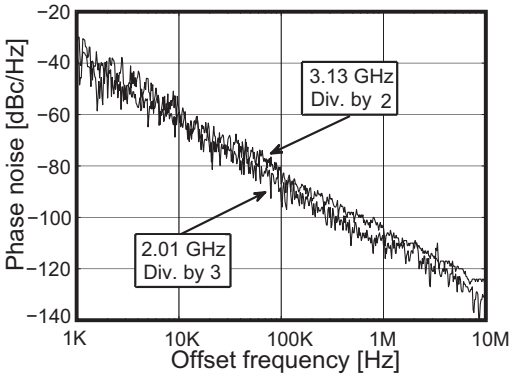

Fig.7 Measurement results of phase noise

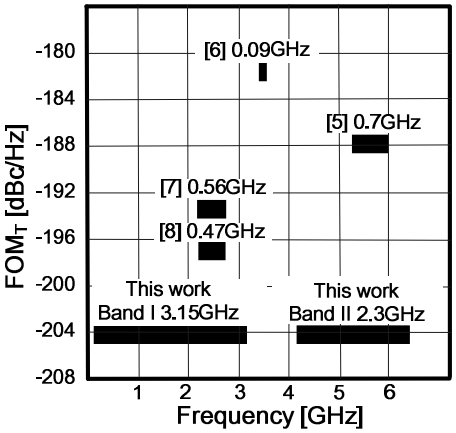

Fig.8 Comparison of FOM_T and tuning range between ultra-low-voltage VCOs