A 0.5 V, 1.2 mW, 160 fJ, 600 MS/s 5 bit Flash ADC

Masaya Miyahara, James Lin,
Kei Yoshihara and Akira Matsuzawa

Tokyo Institute of Technology, Japan

Matsuzawa & Okada Lab

Outline

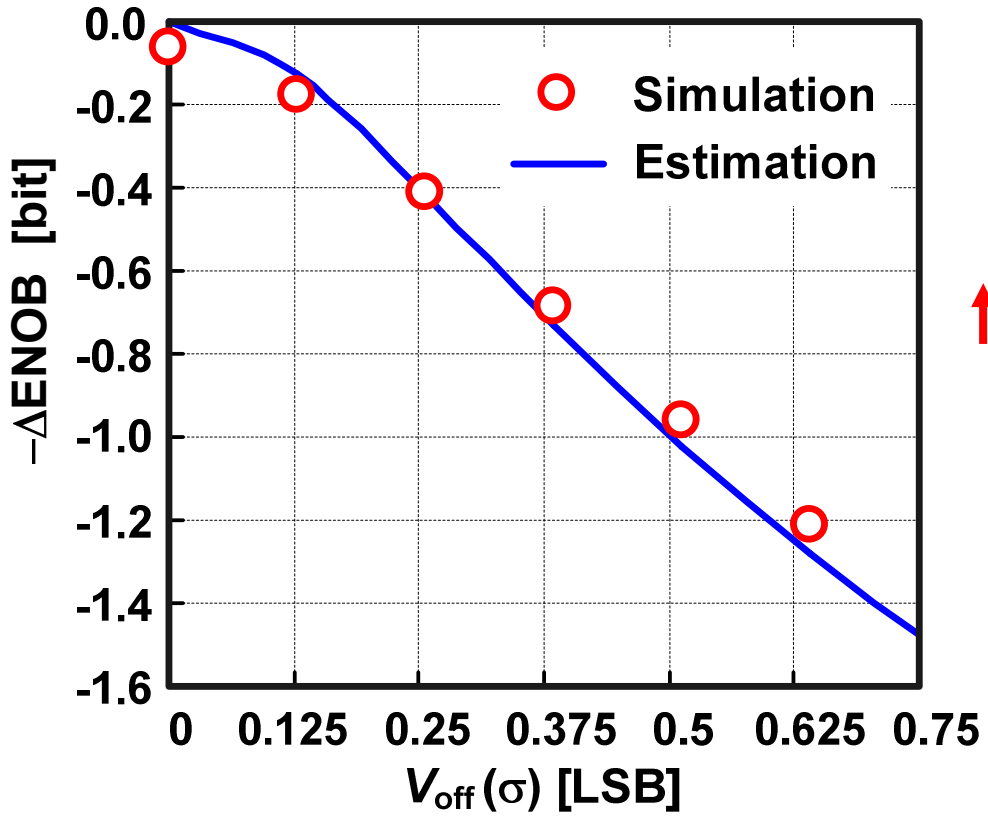
- **Motivation**
- **Design Concept**
- **Calibration Technique**
- **Measurement Results**
- **Conclusions**

Motivation

- **An ultra-low power ADC is strongly required.**
  - **Portable applications**
  - **Ubiquitous wireless sensor system**
  - **Green IT**
- **A low voltage operation is required for further technology scaling and low power operation.**
  - **Analog circuits design becomes more difficult.**
    - **Increasing V_T mismatch**
    - **Degradation of gain and distortion of an amplifier**
  - **The FoM of an ADC should be reduced like digital circuits.**
    - **Optimizing a speed, resolution and power.**
    - **Calibration technique for low voltage operation.**

Performance of flash ADCs

FoM is deteriorated by the offset voltage of the comparator.
Offset voltage should be low at low voltage operation.



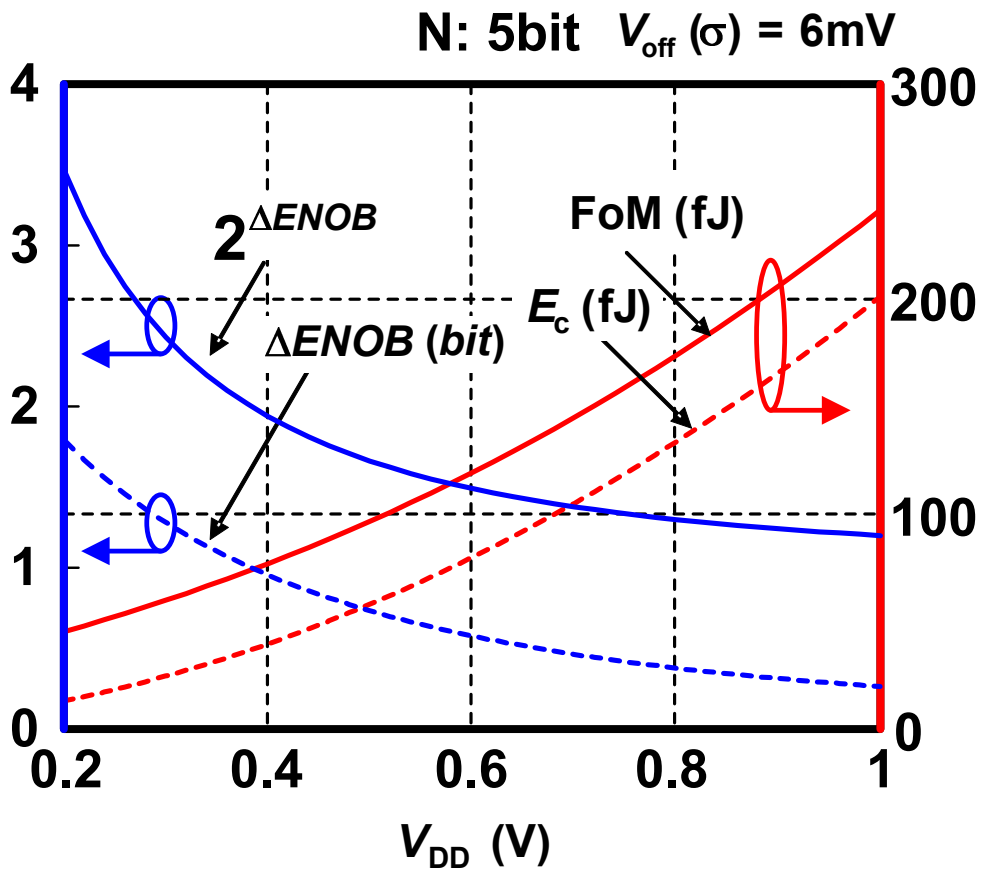
$$\mathrm{FoM} = \frac{P_d}{f_c \times 2^{N-\Delta ENOB}}$$

$$\uparrow \Delta ENOB = \frac{1}{2}\log_2\left(1 + 12\left(\frac{V_{off}(\sigma)}{V_q \downarrow}\right)^2\right)$$

$V_{off}(\sigma)$:Offset voltage
V_q : 1LSB voltage

FoM vs. VDD

FoM can be significantly reduced by reducing power supply voltage *V*DD.



$$\mathrm{FoM} = \frac{f_c \times E_c \times 2^N}{f_c \times 2^{N-\Delta ENOB}} = E_c 2^{\Delta ENOB}$$

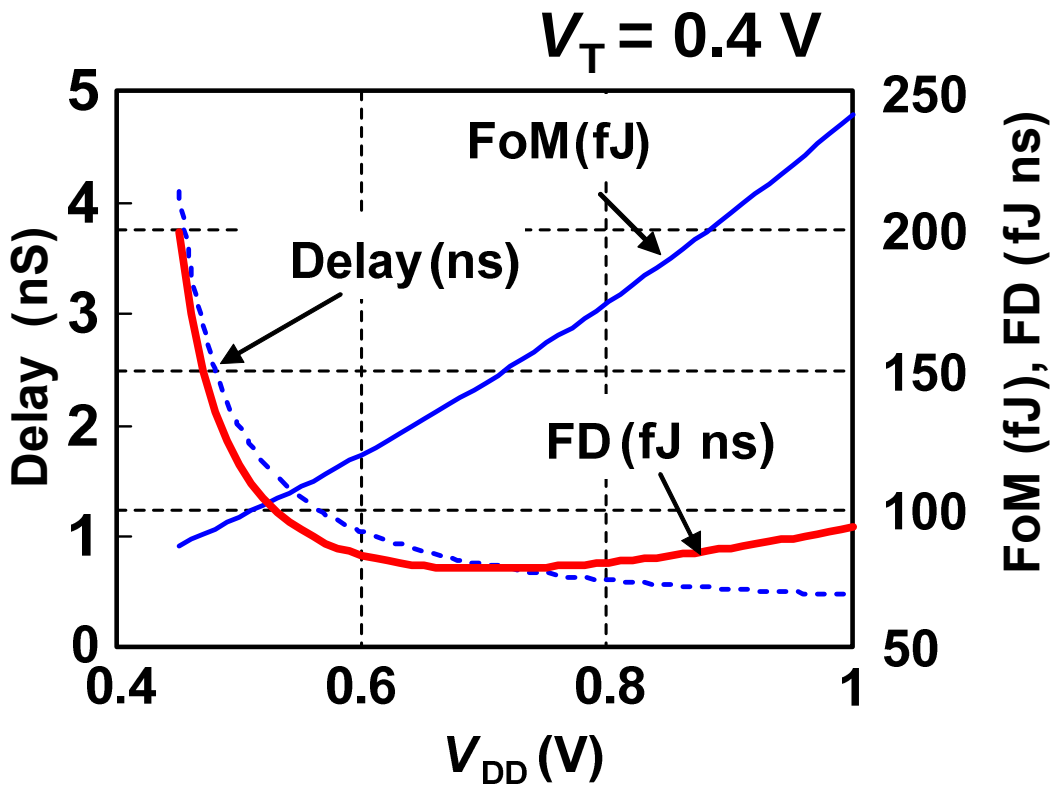
$$E_c = C_c V_{DD}^2 + \frac{V_{DD} \cdot I_c \exp\left(-\frac{V_T}{S}\right)}{f_c}$$

E_c:Energy consumption for each comparator and followed logic circuits.

FoM delay product

The FD product suggests the balance between the number of interleaving and decrease of energy consumption.

$$FD = FoM \times Delay$$



Excessive number of Interleaving ADC

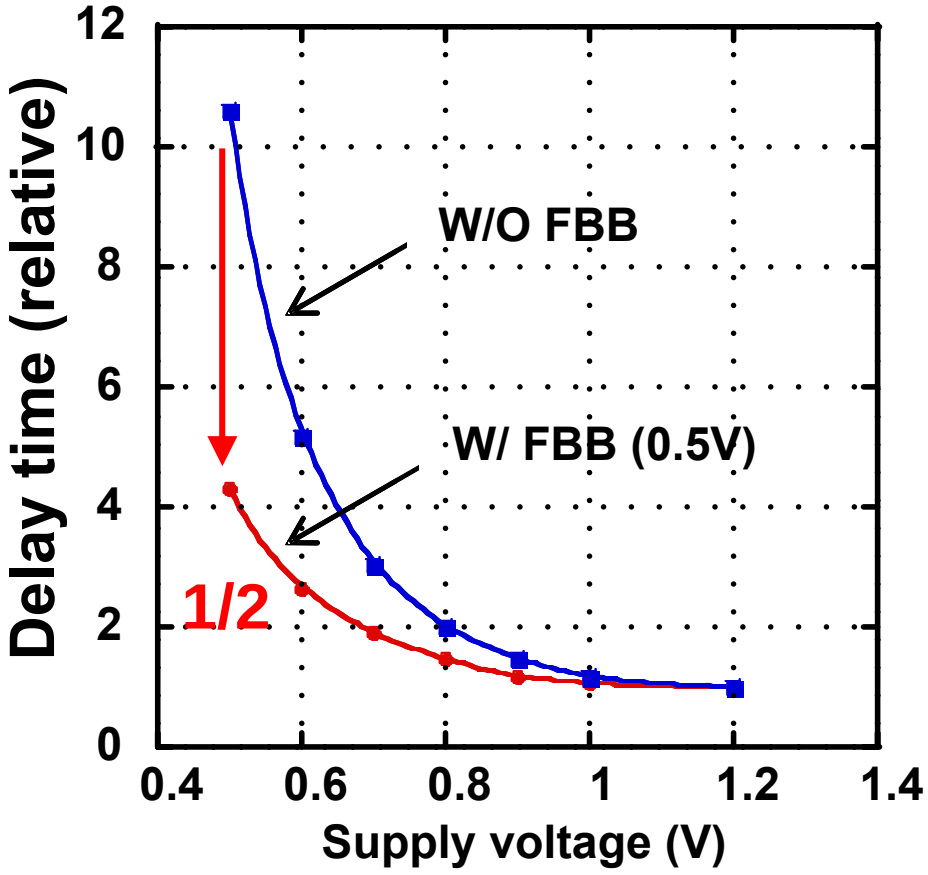
- **Large area**
- **Driving difficulty**
- **Reduction of ENOB**

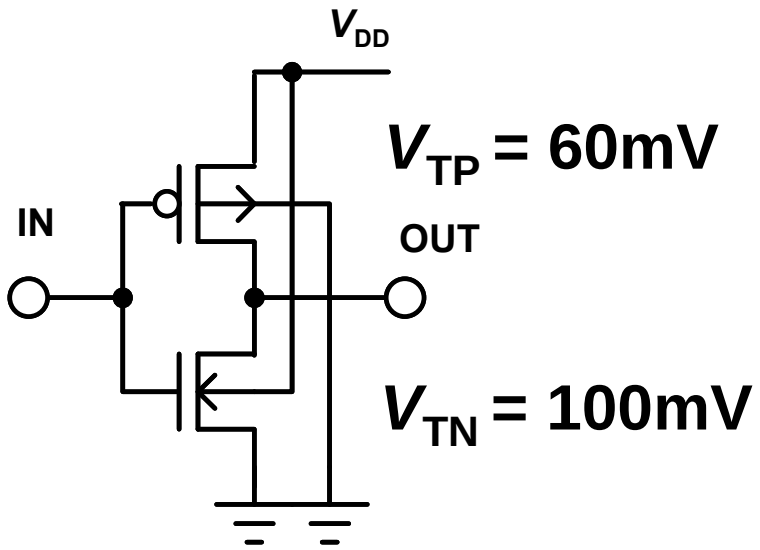
Delay time

$$T_d = k\frac{V_{DD}}{(V_{DD} - V_T)^{\alpha}}$$

Forward body biasing

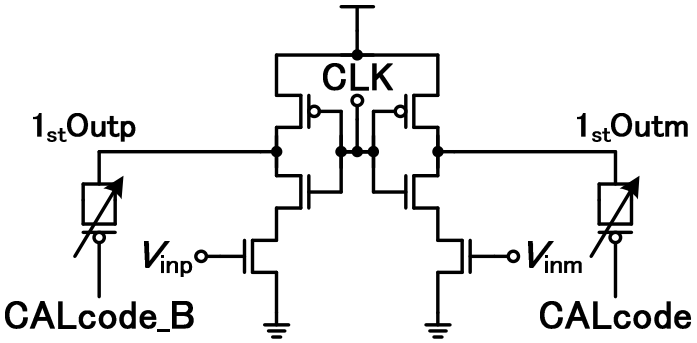
Forward body biasing can decrease the delay time (1/2) and can be used easily at 0.5 V operation.

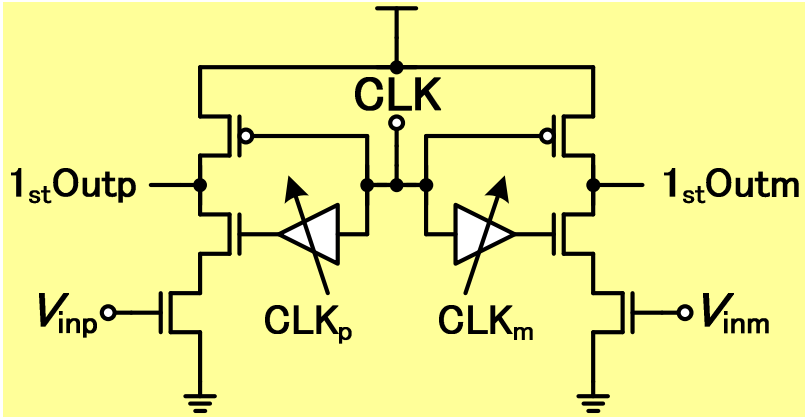


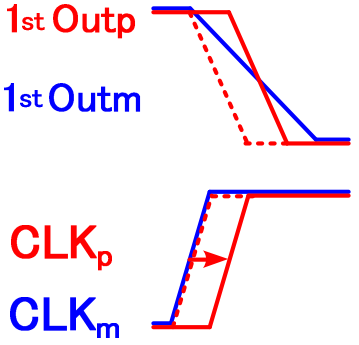


Increased leakage current in the proposed ADC is 0.32 mA by forward body biasing.

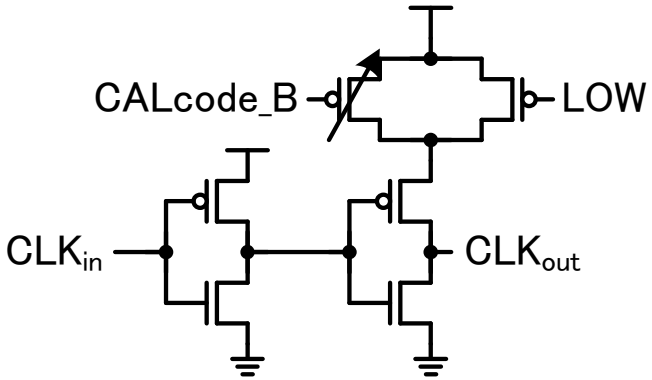
Proposed Calibration Technique







Conventional Calibration
(Capacitor DAC base[5])
- **MOS varactor sensitivity ↓**
- **Delay time and power ↑**



Timing controller

Proposed Calibration
(Timing control base)

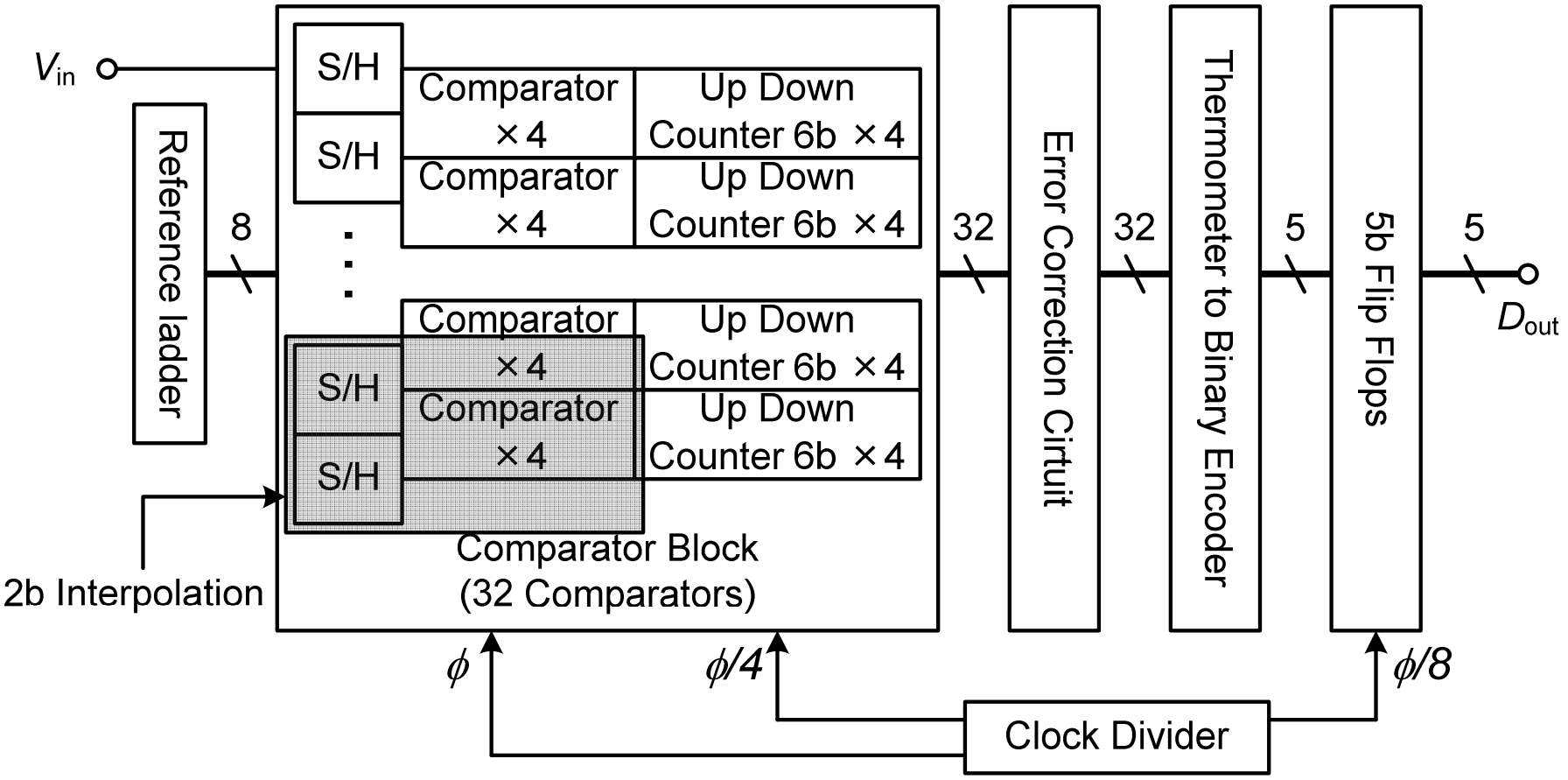
V_{DD}=0.5V, f_s=500MHz

	no CAL	Cap CAL [5]	Proposed
$V_{off}(\sigma)$ [mV]	10.1	5.79	1.49
P_d [μW]	14.5	21.4	24.5
Delay [ps]	365	756	511

[5] V. Giannini, ISSCC2008

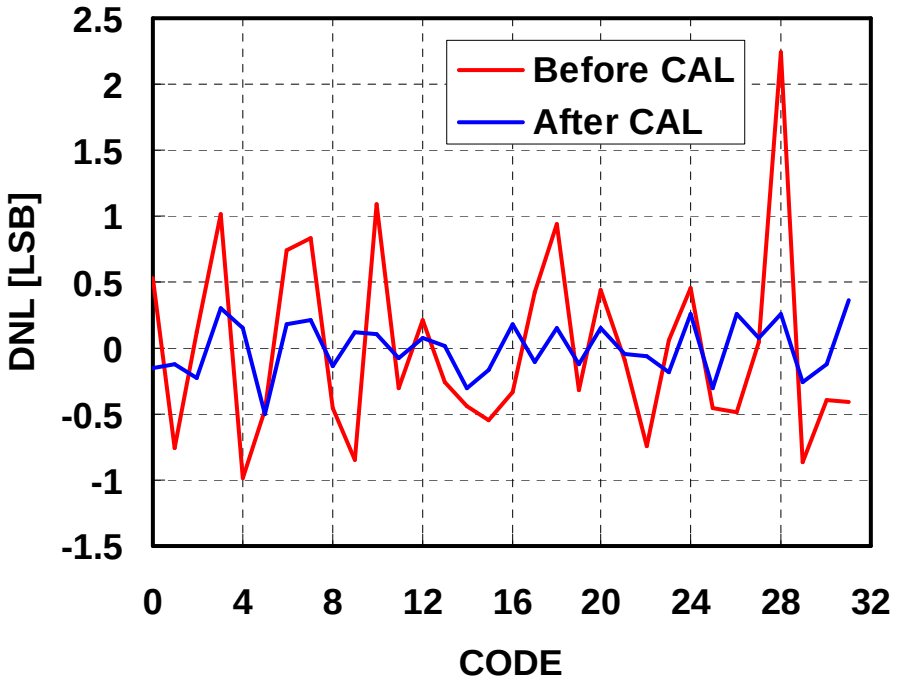
ADC Structure

90nm 1P9M CMOS process

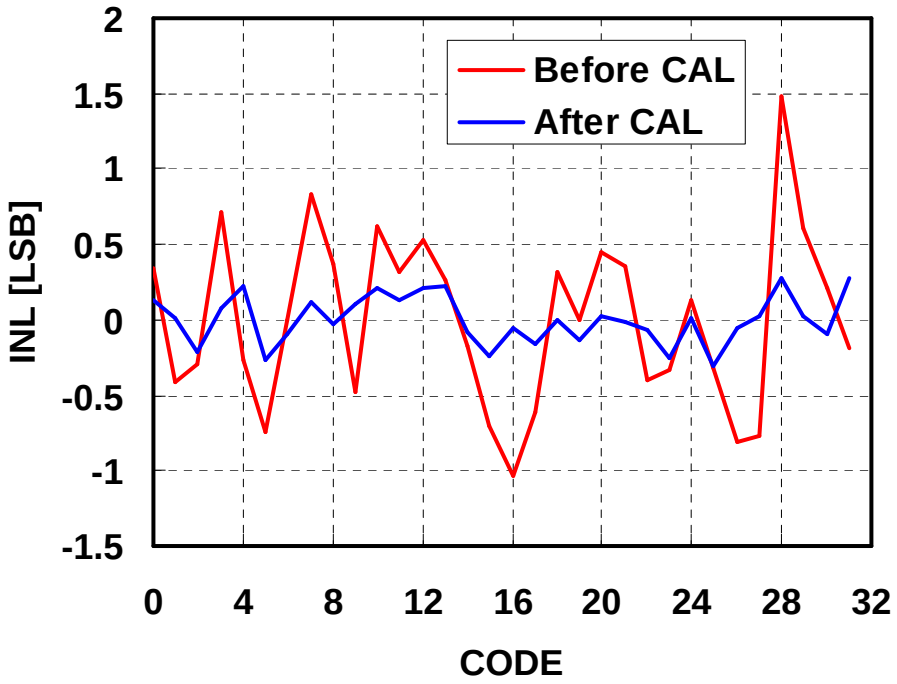


DNL and INL

DNL
+/-2.2 LSB => +/- 0.5 LSB.

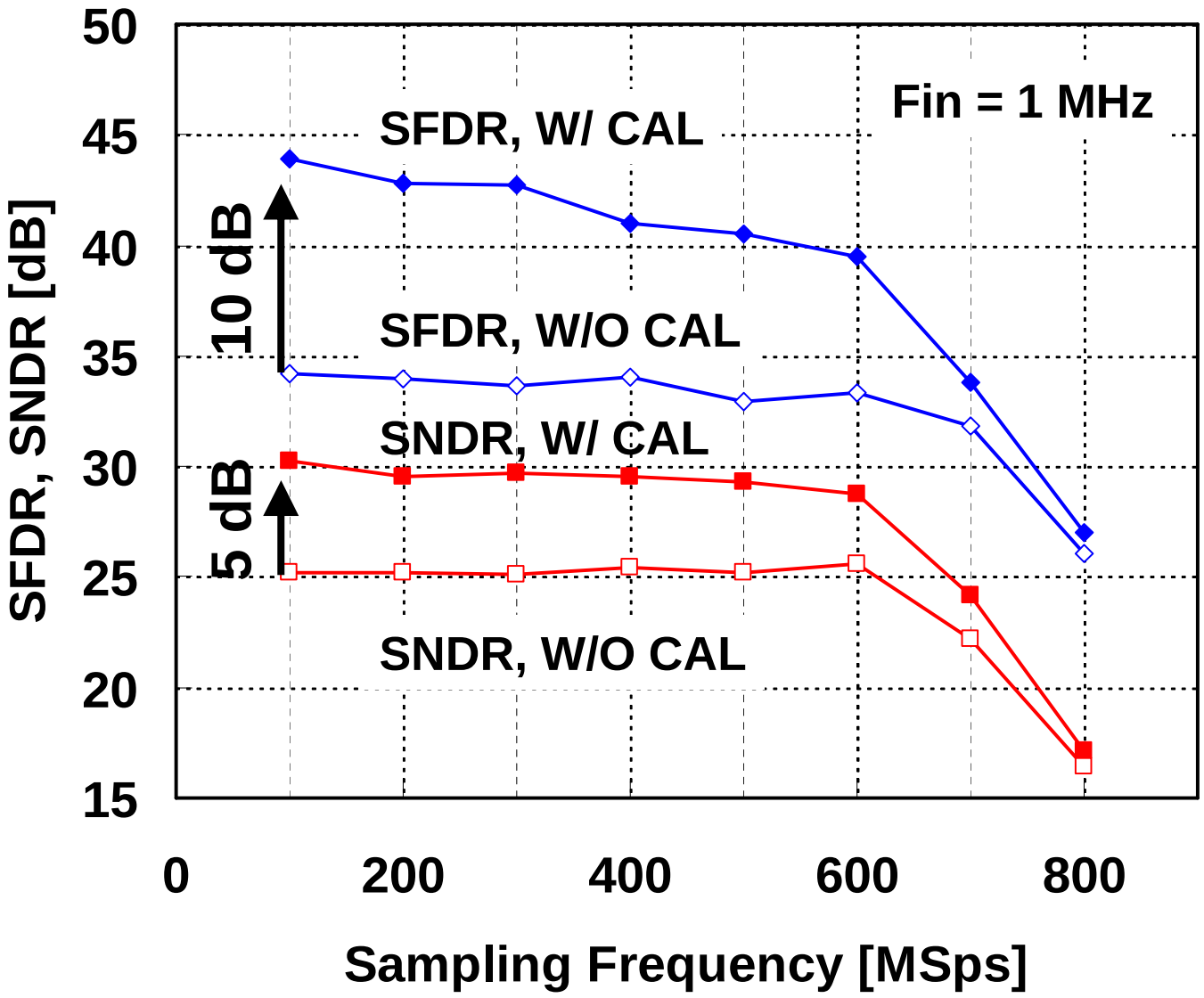


INL
+/-1.5 LSB => +/- 0.3 LSB.

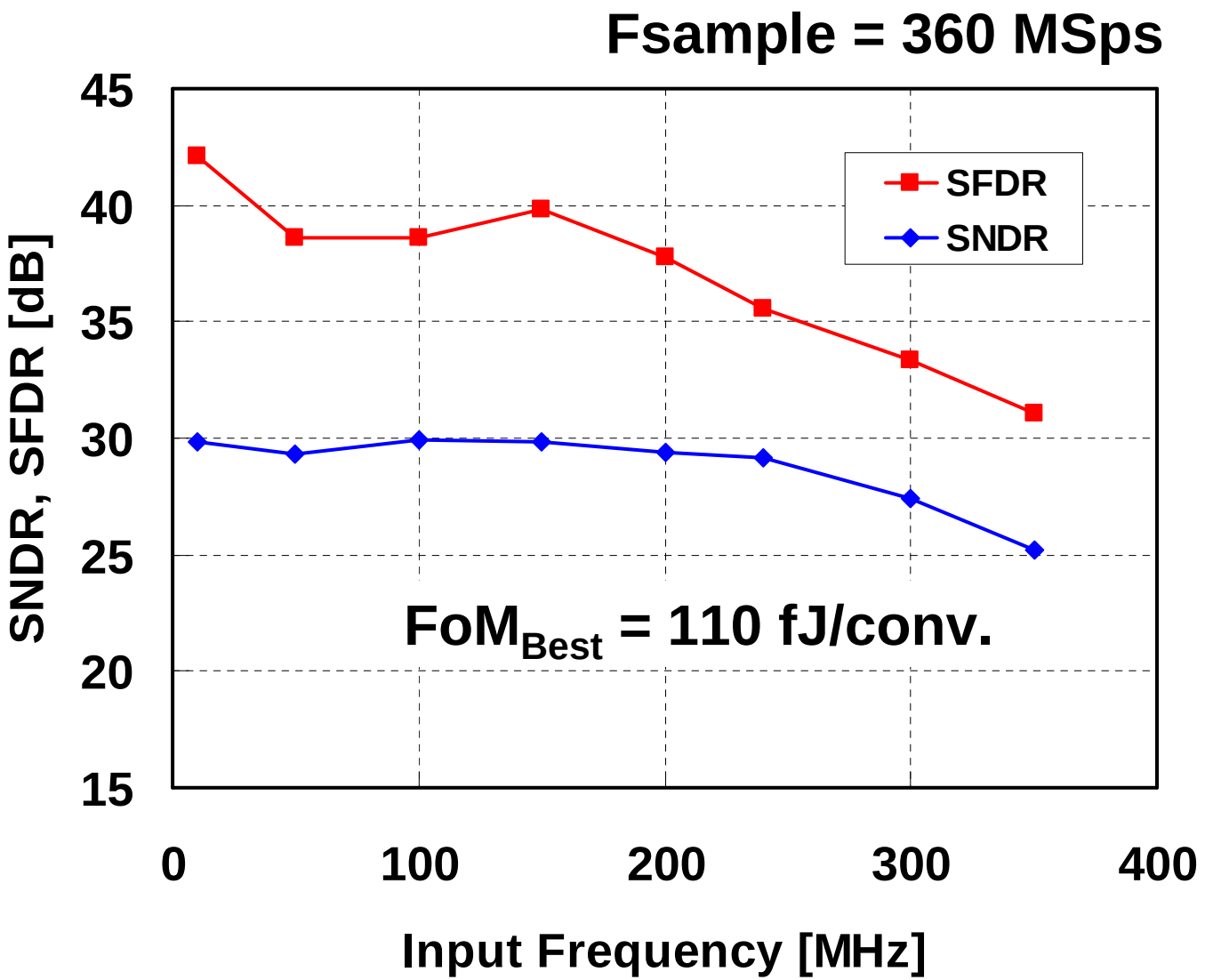


(Measurement results are updated because the measurement setup is improved.)

SFDR and SNDR vs. Fsample



SFDR and SNDR vs. Fin



Performance Summary

Reference #	[7]	[8]	[9]	[10]	**This work**
Resolution (bit)	5	5	5	5	**5**
fs (GS/s)	0.5	1.75	1.75	0.06	**0.6**
SNDR (dB)	26	30	30	26	**27**
Pd (mW)	5.9	2.2	7.6	1.3	**1.2**
Active area (mm^2)	0.87	0.017	0.03	-	**0.083**
Vdd (V)	1.2	1	1	0.6	**0.5**
FoM(fJ)	750	50	150	1060	**160**
CMOS Tech. (nm)	65	90	90	90	**90**
Architecture	SAR	Fold+Flash	Flash	Flash	**Flash**

FoM_{Fmax} = 160fJ @ 600MSps
FoM_{Best} = 110 fJ @ 360MSps

[7] B. P. Ginsburg, J. Solid-State Circuits 2007.
[8] B. Verbruggen, ISSCC 2008.
[9] B. Verbruggen, VLSI Circuits 2008.
[10] J. E. Proesel, CICC 2008.

Conclusions

- **The strategy for low voltage operation is proposed.**
  - **FoM delay product (FD) is considered for not only low FoM but also high speed operation.**
- **Low voltage design techniques are proposed.**
  - **Forward body bias can be used easily at 0.5 V operation. (T_d => 1/2)**
  - **The timing control based offset calibration technique is proposed. (DNL / INL 2 LSB => 0.5 LSB)**
- **Proposed ADC has good power efficiency and high speed operation.**
  - **600MSps, ERBW = 200 MHz, ENOB = 4.6 bit, FoM_{Best} =110 fJ/ conv. at 0.5 V supply.**

Thank you for your interest!

Masaya Miyahara,
masaya@ssc.pe.titech.ac.jp