[4D-12]

A 60GHz Direct-Conversion Transmitter in 65nm CMOS Technology

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Conclusion

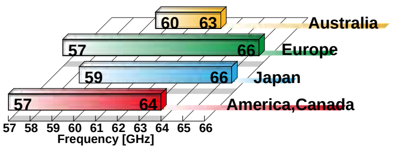
I designed a 60GHz Direct-Conversion Transmitter in 65nm CMOS process.
We built the device models by using a new de-embedding method.
The conversion gain is 10.6 dB and output power @1dB is 1.6 dBm.

1. Background

CMOS 60GHz RF Circuits

Available wide frequency range without licensees
High data rate wireless communication

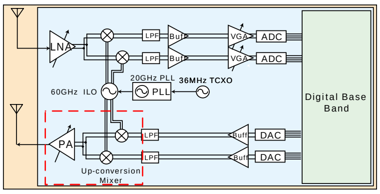
QPSK : 14Gbps, 16QAM : 28Gbps



Available frequency range

Direct conversion system

Power Amplifier
Up-conversion Mixer

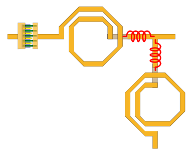


RF Front-end

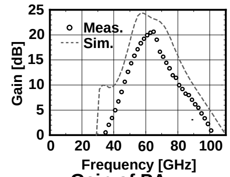
2. Challenge

Parasitic elements

The characteristic of PDK are not assured.
There are large error between simulation and measurement.
Modeling of components are needed.
Transistors, Capacitors, TLs, Decoupling Cap.



Parasitic elements



Gain of PA

3. De-embedding

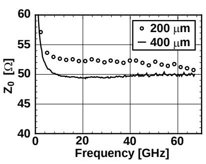
Conventional methods

Open-short method
Non-ideality of short cannot be neglected.
Thru only method
The length of the short-line has to be short because we use lumped component.

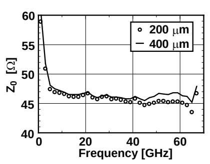
New de-embedding method

Multi-line de-embedding method [1]

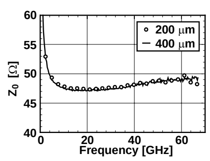
Compare Z_0 of 200 m-TL and Z_0 of 400 m-TL



Open-Short



Thru only



Multi-line

[1] N. Takayama, *et al.*, A Multi-Line De-Embedding Technique for mm-Wave CMOS Circuits , APMC 2010

4. De-coupling Capacitor Modeling

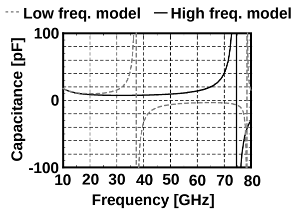
The characteristic of de-coupling capacitors has effect on circuit performance.

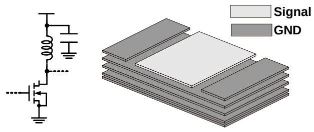
Low frequency

Planar structure
The self resonance frequency is low.

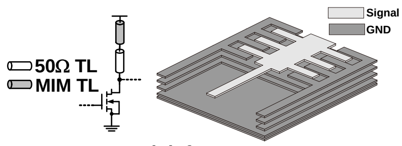
High frequency

Inter-digital structure
The self resonance frequency is high.
Low impedance transmission line





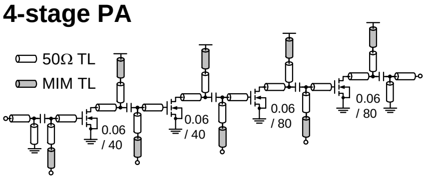
Low frequency



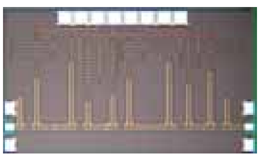
High frequency

5. Power Amplifier

CMOS 65nm process
4-stage PA



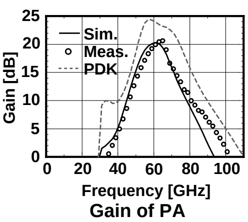
Circuit of PA



Chip photo

Measurement results

Simulation error reduced. 5[dB] ➡ 0.5[dB]
Power Gain : 20 [dB]
Output power @ 1dB : 9.9 [dBm]



Gain of PA

Comparison with other papers

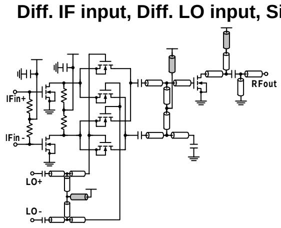
Reference	Technology	Freq. [GHz]	Gain [dB]	P_{1dB} [dBm]	PAE@P_{1dB} [%]	P_{DC} [mW]	V_{DD} [V]
[2] ISSCC 2008	90nm CMOS	60	5.5	9	6	80	1
[3] ISSCC 2009	65nm CMOS	60	15.8	2.5	3.95	43.5	1
[4] MWCL 2009	90nm CMOS	60	30	10.3	6	178	1.8
This work	65nm CMOS	61.5	20	9.9	6.7	144	1.2

[2] D. Chowdhury, *et al.*, ISSCC 2008 (UCB)
[3] W.L. Chan, *et al.*, ISSCC 2009 (Delft Univ.)
[4] J.-L.Kuo, *et al.*, MWCL 2009 (NTU)

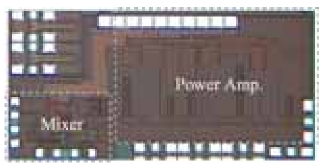
6. 60GHz Transmitter

Power Amplifier + Up-conversion Mixer

Passive Mixer
Diff. IF input, Diff. LO input, Single RF output



Circuit of Up-Conversion Mixer



Chip photo

Measurement results

Conversion Gain : 10.6 [dB]
Output Power @ 1dB : 1.6 [dBm]

Comparison with other papers

	Blocks	Freq. [GHz]	Gain [dB]	P1dB [dBm]	PDC [mW]	PLO [dBm]	VDD [V]
[5]	Mix	60	< -4	-	70	-	1.5
[6]	Mix	56-65	< 4	-5.6	24	0	1.6
This Work	Mix +PA	60	10.6	1.6	186	1	1.2

[5] S. Voinigescu,*et al.*, ISCAS 2007 [6] F. Zhang, *et al.*, EL 2008