

A 60GHz Direct-Conversion Transmitter in 65nm CMOS Technology

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Abstract— This paper presents a 60 GHz direct-conversion transmitter in 65 nm CMOS technology. The power amplifier consists of 4-stage transistors. The circuit model of de-coupling capacitor is built as a transmission line to consider the physical length. In the measurement results, the conversion gain is above 9.6dB at 58-65GHz band, and the 1 dB compression point is 1.6 dBm with 60 GHz LO frequency and 1 dB LO power.

I. INTRODUCTION

Recently, researches of wireless communications in mm-wave, 30-300 GHz, are actively conducted. 60 GHz wireless communication is especially expected because the frequency bands near 60GHz are available without licenses in many countries. 60 GHz circuits have been implemented by using compound semiconductor processes so far because of highly cutoff frequency and high-voltage operation [1]. However the cutoff frequency of CMOS transistor is increased in recent days, and CMOS circuits has obtained 60 GHz capability, which contributes to realize 60 GHz RFIC for reasonable consumer terminals. To achieve this, one of the challenges is design of 60 GHz power amplifier. It is difficult to obtain a large output power by CMOS transistors using a low supply voltage. Many researchers are studying this issue [2], [3].

In this work, the CMOS power amplifier at 60 GHz are implemented with the circuit component models extracted from measurements, and connecting it with the up-conversion mixer that converts signals from 0-1 GHz to 60 GHz, the direct-conversion transmitter is designed. The procedures of design and measurement result are described as follows.

II. CIRCUITS

The circuit schematic of power amplifier is shown in Fig. 1, which consists of four common source transistors. There are matching blocks composed of transmission lines and matching capacitor between transistors to increase the power gain and the output power, and in front of the first stage to convert the input impedance to 50 Ω . Designing circuits, the models of transistors, transmission lines, matching capacitors and de-coupling capacitors are used. The circuit model of de-coupling capacitor is characterized as a transmission line to consider the physical length.

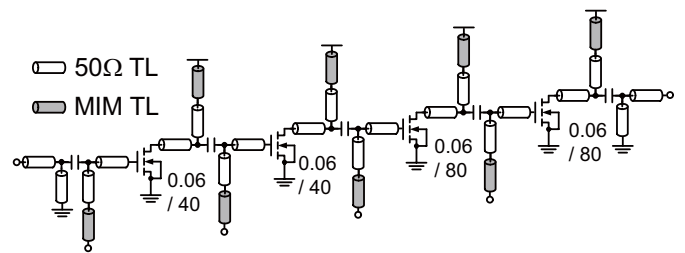


Fig. 1. Circuit schematic of power amplifier.

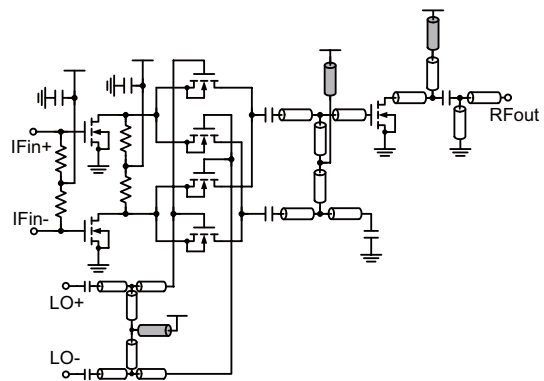


Fig. 2. Circuit schematic of up-conversion mixer.

The circuit of up-conversion mixer is shown in Fig. 2. A double-balanced mixer is employed as the core part of the mixer to reduce leakage of local signals. There are the IF-buffer with resistor loads in front of the input and the RF-buffer with transmission lines behind the output. In addition, to transmit LO signal power to the circuit, the impedance of the LO-port is converted to 50 Ω . One side of the mixer outputs is terminated with the capacitor to reduce the layout area.

III. MEASUREMENT RESULTS

For calibrating loss of the measurement system, loss of the signal generator, spectrum analyzer, cables and probes are measured by using the power meter. Loss of a 36-inch-long cable is more than about 5 dB and loss at 55 GHz is different to one at 65 GHz by about 0.5 dB, therefore this procedures is very important.

The microphotograph of the circuit of the PA connected

TABLE I
COMPARISON OF MM-WAVE POWER AMPLIFIERS AND UP-CONVERSION MIXERS IN SILICON

	Integrated Blocks	RF [GHz]	Gain [dB]	P_{1dB} [dBm]	P_{DC} [mW]	P_{LO} [dBm]	V_{DD} [V]	Technology
[2]	PA	51.2	19.5	3.1	150	-	1.2	90nm CMOS
[3]	PA	60	10	12.6	213	-	1	90nm CMOS
[4]	Up-conv. Mix.	60	≤ -4	-	70	-	1.5	90nm CMOS
[5]	Up-conv. Mix.	56-65	≤ 4	-5.6	24	0	1.6	130nm CMOS
This work	PA + Up-conv. Mix.	60	10.6	1.6	186	1	1.2	65nm CMOS

with up-conversion mixer is shown in Fig. 3. IF frequency is 500 MHz, and LO frequency is 60 GHz. In the measurement results, the conversion gain is above 10.6 dB and the 1dBm compression point is 1.6dBm with 1 dB LO power. The relation between the conversion gain and the input power is shown in Fig. 4 (a). The power consumption of the mixer is 49 mW and that of the PA is 137 mW, then the total is 186mW from a 1.2V supply. The comparison of the performance with other reported PAs and up-conversion mixer is shown in Tab. I. Among them with mixing function, the conversion gain of this circuit is the highest. Comparing with other PAs, the gain is very competitive.

For IEEE 802.15.3c unlicensed wireless communication systems, the transmitter has to operate from 58 GHz to 65 GHz. To confirm the performance, the measurements of the chip are done with changing the LO frequency. The results are shown in Fig. 4 (b). IF frequency is fixed to 100 MHz. From this figure, the conversion gains of this transmitter are more than 9.5 dB at the desired frequencies, 58-65 GHz.

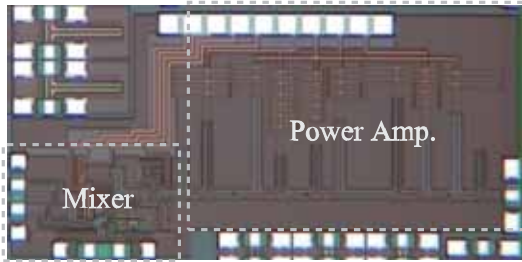


Fig. 3. Micrograph of PA connected with up-conversion mixer.

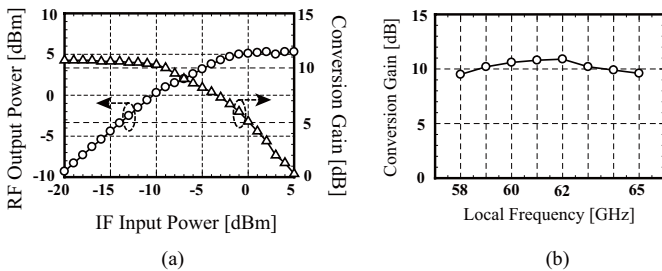


Fig. 4. Measurement results. (a) Power measurement. (b) LO frequency vs conversion gain.

IV. CONCLUSIONS

The 60GHz direct-conversion transmitter is implemented in 65nm CMOS technology. For designing the mm-wave circuits, it is important that models of transistors, transmission lines, matching capacitors and de-coupling capacitors are made from measurement data. Especially, modeling de-coupling capacitors as a transmission line contributes to improve accuracy in simulation. In the measurement results of power amplifier connected with up-conversion mixer, the conversion gain is above 9.6dB at 58-65GHz band and the 1dB compression point is 1.6dBm with 60GHz LO frequency and 1dBm LO power.

ACKNOWLEDGEMENTS

This work was partially supported by MIC, NEDO, STARC, and VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Cadence Design Systems, Inc and Agilent Technologies Japan, Ltd.

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