A 2-6 GHz Fully Integrated Tunable CMOS Power Amplifier for Multi-Standard Transmitters

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***Abstract*—A tunable power amplifier (PA) from 2.1 GHz to 6.0 GHz is presented for multi-standard radios. The proposed multi-band PA can tune the output impedance to 50 Ω over a wide frequency range, so external isolators following PAs can be eliminated. The PA is implemented by using a 0.18 μm CMOS process, and the supply voltage is 3.3 V. Over all of the frequency range, the PA realizes output return loss S_{22} of smaller than -8 dB, power gain of larger than 12 dB, output 1-dB compression point of larger than 15 dBm.**

I. Introduction

A single-chip multi-standard transceiver integrating all functional blocks for wireless communication is expected, especially for cellular applications. An integrated CMOS PA is a key challenge to realize such the single-chip transceivers. Wideband PAs utilizing distributed amplification are presented in [1-3]. However, the output powers are not sufficient for the multi-band use, and the distributed amplifiers usually need large layout area. A wideband PA utilizing multiple power mixers is reported [4], which realizes an output power of more than 30 dBm. However, wideband output matching is not considered, and external isolators for each band are still expected to be used. A tunable PA utilizing resistive feedback and parallel resonance is proposed in [5], which can tune output matching bands from 0.9GHz to 3.0GHz and deliver large output power with adequate linearity. In this paper, a 2-6GHz tunable PA is presented, and it can also realize an isolator-less transmitter at higher frequency bands.

II. Tunable Power Amplifier

A resistive feedback amplifier is commonly used as a broadband low noise amplifier because the input impedance is a function of the feedback resistance, which can be adjusted to 50 Ω over a wide frequency range. In this work, this technique is applied to the output impedance matching of tunable power amplifiers.

Fig. 1 shows the schematic of the proposed PA. A differential topology is employed to deliver larger output power, which also contributes to neglect parasitic impedance on common-mode nodes. To sustain voltage stress, a thick gate-oxide transistor is used for the common-gate stage. A supply voltage of 3.3V is used to increase voltage swing at the output nodes. The switches in the capacitor array are also implemented by thick gate-oxide transistors because of the same reason.

The feedback resistance is tuned depending on the switching state. There are some reasons for this. Firstly, the quality factor of the LC resonator depends on frequency and influence of the output impedance. Secondly, DC-cut capacitances cannot be very large because the parasitic capacitance of the output node determines the maximum resonance frequency. Thus, the feedback resistance has to be adjusted according to the frequency. The matching frequency can be switched from band 1 to band 4 in this case. By increasing the number of switches, finer frequency tuning can be realized. In addition to output matching tuning, the resistive feedback topology has an advantage in enhancing the stability of the circuit.

III. Mesurement Results

The proposed PA was designed and fabricated by using a 0.18 μm CMOS process. Fig. 2 shows the chip micrograph, and core size is 0.47 × 0.49 mm^2. The chip was measured by using RF probes with external DC blocks at input and output nodes. Figs. 3 and 4 show the measured S_{22} and S_{21} of each frequency band in differential-mode. The output matching frequency is shifted according to switching bands. From 2.1 GHz to 6.0 GHz, S_{22} keeps lower than -8 dB and S_{21} is larger than 12 dB. The output power and PAE at other bands with different signal frequency was measured.

Fig. 5 shows the saturated output power, the output 1-dB compression point, the PAE at 1-dB compression point, and the maximum PAE versus frequency. The output 1-dB compression point is larger than 15 dBm, and the saturated output power is larger than 18 dBm with >9 % of the maximum PAE.

Table I summarizes state-of-the-art results of multi-band PAs using CMOS technology. The proposed circuit demonstrates good output power with the tunable impedance matching.

IV. Conclusion

In this paper, a CMOS PA with the tunable output impedance matching over a wide frequency range is proposed for multi-band transmitters. A prototype was fabricated in a 0.18 μm CMOS process. Utilizing resistive feedback and parallel resonator with an inductor and a tunable capacitor array, the PA achieves wide-tunable output impedance matching from 2.1 GHz to 6.0 GHz. With a 3.3 V supply voltage, the PA realizes output 1-dB compression point of larger than 15 dBm. The proposed PA demonstrates the potential to realize multi-band transmitters without isolators.

Acknowledgment

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TABLE I. PERFORMANCE COMPARISON

	Technology	V_{DD} [V]	Frequency [GHz]	P_{1dB} [dBm]	P_{sat} [dBm]	Max PAE [%]	Area [mm^2]	S22 [dB]	Output matching	Topology
[1]	0.13μm CMOS	2.0	2.0 ~ 8.0	3.5	7 ~ 10	2 @1dB	—	< -5	Wideband	Distributed
[2]	0.13μm CMOS	1.5	0.5 ~ 5.0	10 ~ 17	14 ~ 21	3 ~ 16 (drain eff.)	3.6 (w/ pads)	< -6	Wideband	Distributed + Transformer
[3]	0.18μm CMOS	2.8	3.7 ~ 8.8	14 ~ 16	16 ~ 19	8 ~ 25	2.8 (w/ pads)	< -8	Wideband	Distributed
[4]	0.13μm CMOS	3.0	1.0 ~ 2.5	—	28 ~ 31	18 ~ 43	2.56 (w/ distributor)	—	Wideband	Power mixer + Transformer
[5]	0.18μm CMOS	3.3	0.9 ~ 3.0	17 ~ 21	20 ~ 21	11~ 23	0.31 (w/o pads)	< -10	Tunable	Feedback
This work	0.18μm CMOS	3.3	**2.1 ~ 6.0**	15 ~ 18	18 ~ 22	9~ 17	0.23 (w/o pads)	< -8	**Tunable**	Feedback

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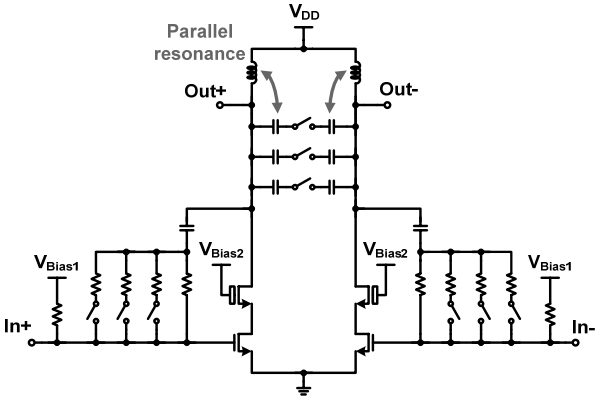

Fig. 1. Schematic of the tunable power amplifier.

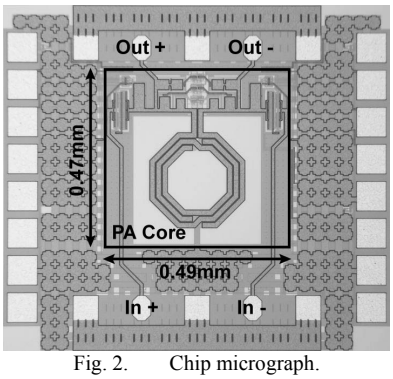

Fig. 2. Chip micrograph.

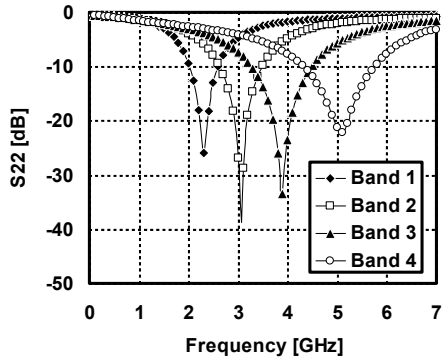

Fig. 3. Measured S_{22}.

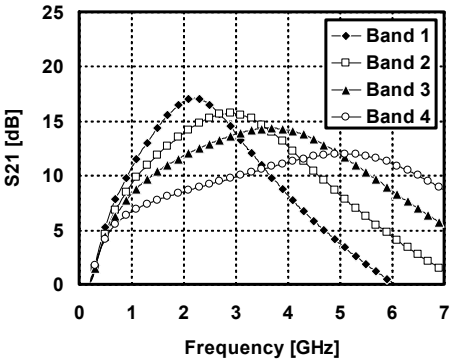

Fig. 4. Measured S_{21}.

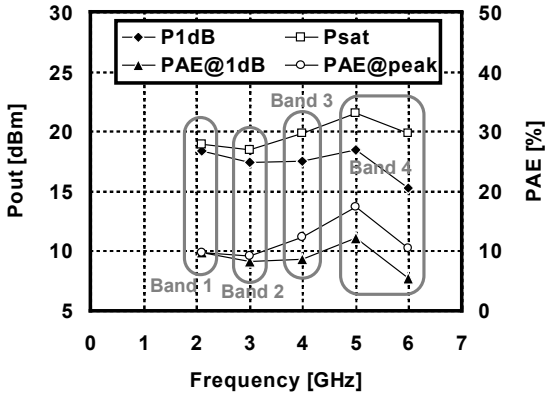

Fig. 5. Measured output 1-dB compression point, saturated output power, PAE at 1-dB compression point, and maximum PAE versus frequency.