Phase Noise Scaling of LC-VCO for Ultra Low Supply Voltage

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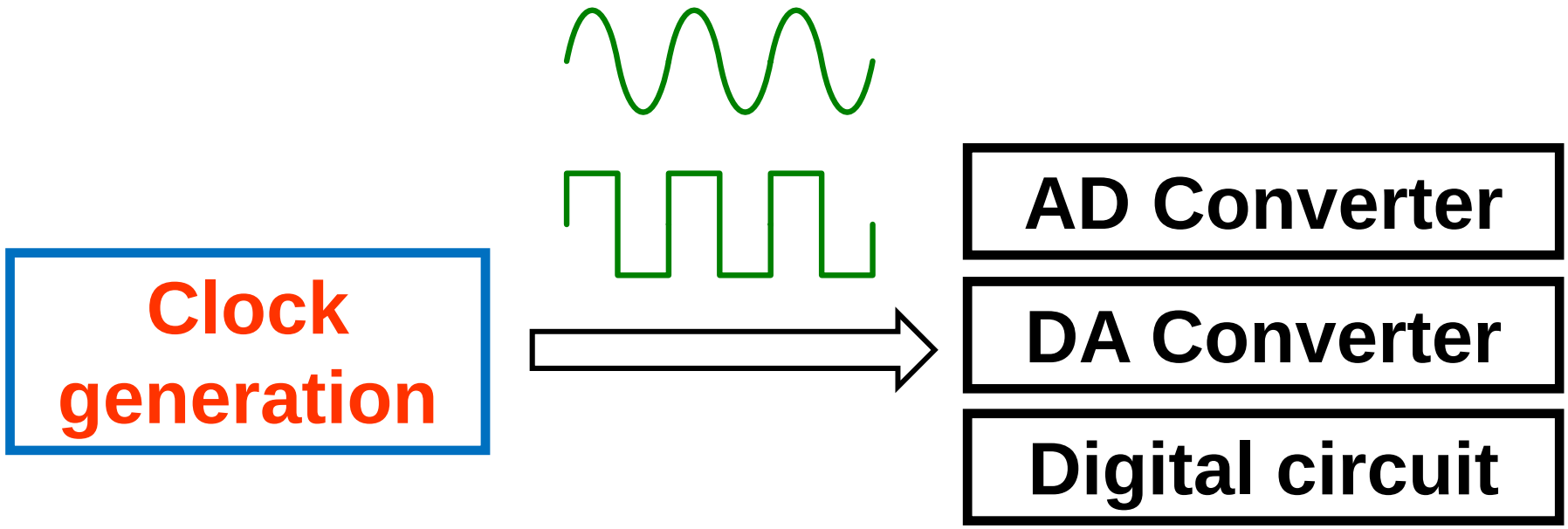
Outline

- **Background**
  - **Clock generation in System-on-Chip**
- **Challenging**
  - **Supply voltage scaling**
- **Low voltage clock generator's issues**
  - **Ring VCO becomes infeasible due to too large phase noise performance**
- **Possible solution**
- **Conclusion**

Research Background

Clock Generation in SOC



Clock generation circuits are widely used in a number of applications in which a reference tone is required

How to Evaluate Clock Generator?

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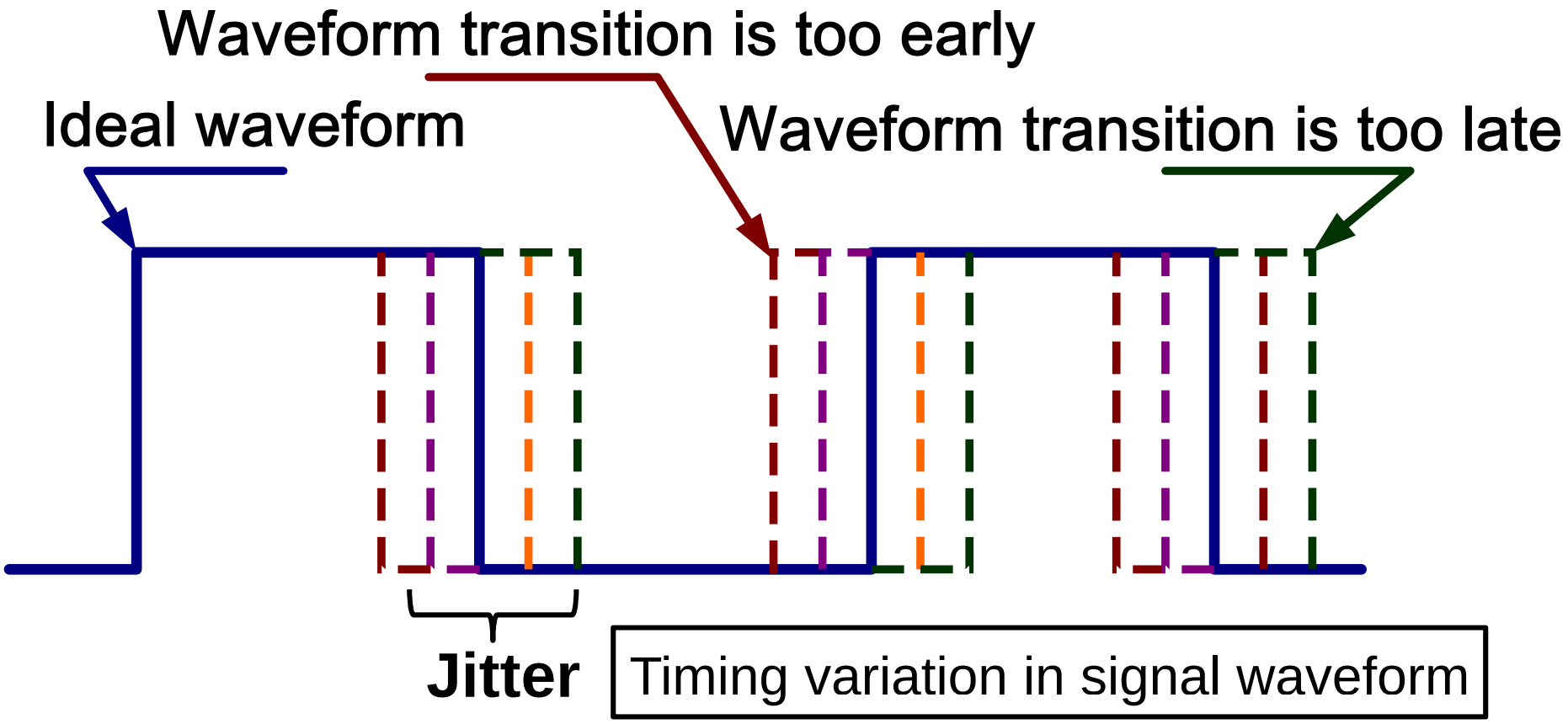
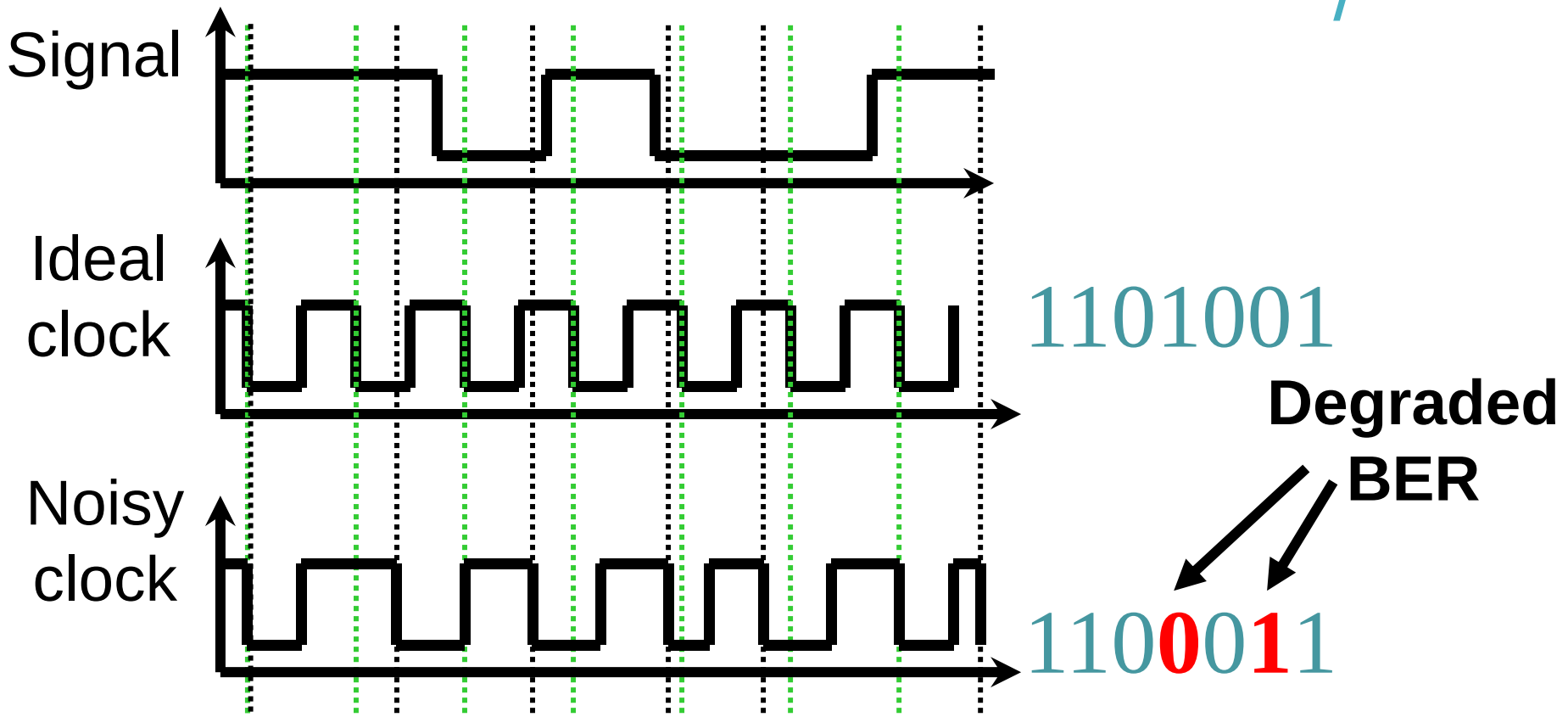
- **Phase noise**
  - **Measure of spectral density in frequency domain**
  - **Units: dBc/Hz (decibels below the carrier per Hz)**
- **Jitter (Better choice for clock)**
  - **Measurement of variations in time domain**
  - **Units: Seconds (usually pS)**

What is Jitter in Clock Generator?



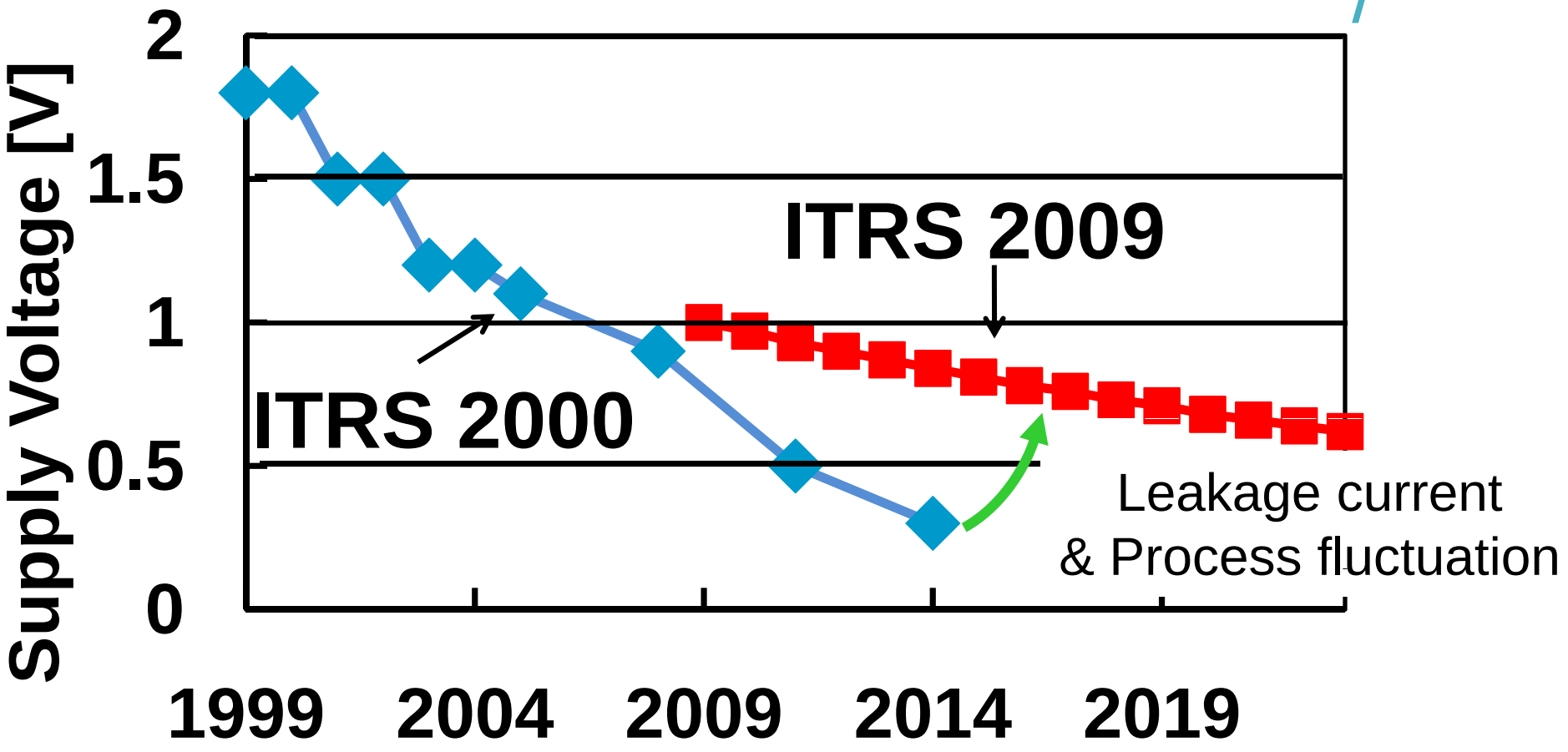
Cause of Jitter (phase noise): Thermal noise and shot noise

How Jitter Affect Performance?



Clock generator with small jitter (phase noise) is strongly desired

Scaling of Supply Voltage



How about phase noise performance along with supply voltage scaling?

Phase Noise Comparison

LC-VCO [A. Mazzanti, et al., JSSC 2008]

$$\frac{\omega_0^2}{\omega_{offset}^2}\cdot\frac{kT}{V_{\mathrm{DD}}I_{\mathrm{bias}}}\cdot\frac{1+\gamma_{\mathrm{n}}}{Q^2}$$

+30dB worse

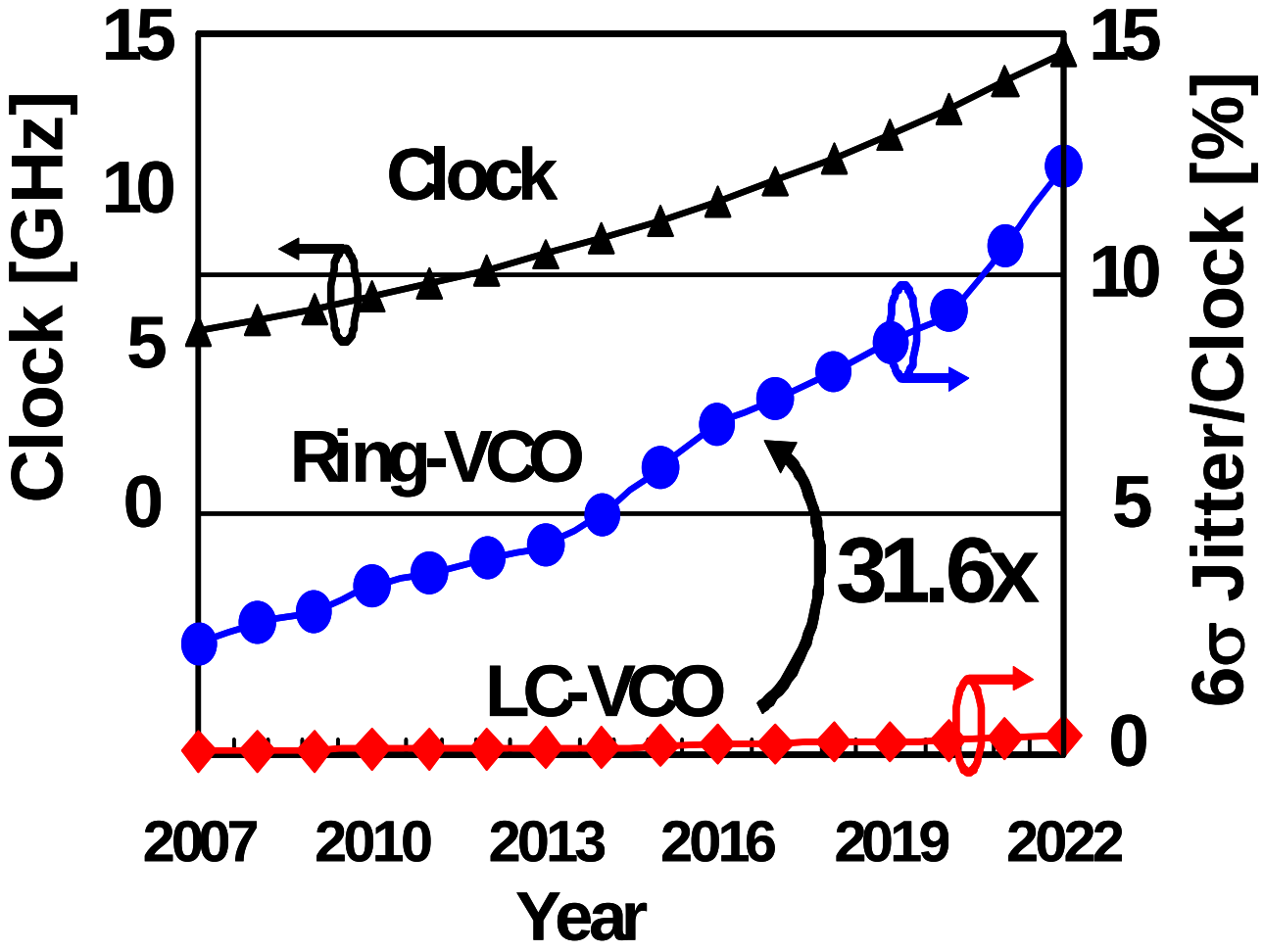
Ring-VCO [A. Abidi, JSSC 2006]

$$\frac{\omega_0^2}{\omega_{\mathbf{offset}}^2}\cdot\frac{\boldsymbol{kT}}{\boldsymbol{V_{\mathrm{DD}}I_{\mathrm{bias}}}}\cdot 2\boldsymbol{M}\left\{\frac{\boldsymbol{V_{\mathrm{DD}}}}{\boldsymbol{V_{\mathrm{DD}}-V_{\mathrm{TH}}}}\left(\gamma_n+\gamma_p\right)+1\right\}$$

M: #stages

$$V_{\mathrm{TH}}=\frac{V_{\mathrm{DD}}}{4},\ \gamma_{\mathrm{n}}=\gamma_{\mathrm{p}}=\frac{2}{3},\ M=3,\ Q=10$$

Scaling of Jitter



With same power consumption, LC-VCO has much smaller jitter performance

Scaling of Phase Noise

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V_{DD}	Type	P_{DC}	Phase Noise +10dB margin @1MHz	Jitter
1.2-V (Now)	LC	1mW	-121.6 dBc/Hz	0.16ps
	Ring	1mW	-91.6 dBc/Hz	5.0ps
0.5-V (Future)	LC	0.17mW	-114.0 dBc/Hz	0.38ps
	Ring	0.17mW	-84.0 dBc/Hz	12.0ps
		174mW	-114.0 dBc/Hz	0.38ps

For 0.5-V clock generators, ring-VCO becomes infeasible due to large power consumption and/or large jitter.

Comparison of Performance

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Parameter	Jitter	P_{DC}	Area	Tuning range
0.5-V Ring VCO	**Very Bad**	Good	Good	Good
0.5-V LC VCO	Very Good	**Fair, but can be improved**	Fair, and improved in [1]	**Fair, but can be improved**

LC-VCO with **P_{DC}, area and tuning range optimization** is necessary for 0.5-V clock generation circuits

[1]: R. Murakami, K. Okada, and A. Matsuzawa, "A 484-μm^2 21-GHz LC-VCO beneath a Stacked-Spiral Inductor, " to be presented at IEEE MTT-S European Microwave Conference (EuMC), Paris, France, Sep. 2010.

Research Status

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-	Unit	[2]	[3]	[4]	[5]	[6]
Topology	-	LC	LC	LC	LC	Ring
V_{DD}	V	0.6	0.5	0.9	0.5	0.5
Frequency	GHz	5.3 ~ 6	3.65 ~ 3.76	2.17 ~ 2.73	2.15~2.62	0.12-1.3
Tuning range	%	8.1	3	22.8	20	85
Jitter	ps	<1	<1	<1	<1	>15

[2] H.-H. Hsieh, *et al.,* MTT 2007 [3] K. Kwok, *et al.,* JSSC 2005 [4] S.Y. Lee, *et al.,* TCAS II 2008
[5] D. Park, *et al.,* MTT 2009 [6] T.W. Li, *et al.,* ASICON 2009

Ultra-low-voltage clock generator with **wide tuning range (merit of ring VCO)**and **sub-picosecond-jitter (merit of LC VCO)** are desired in future 0.5-V SoC and power aware SoC.

Possible Solution

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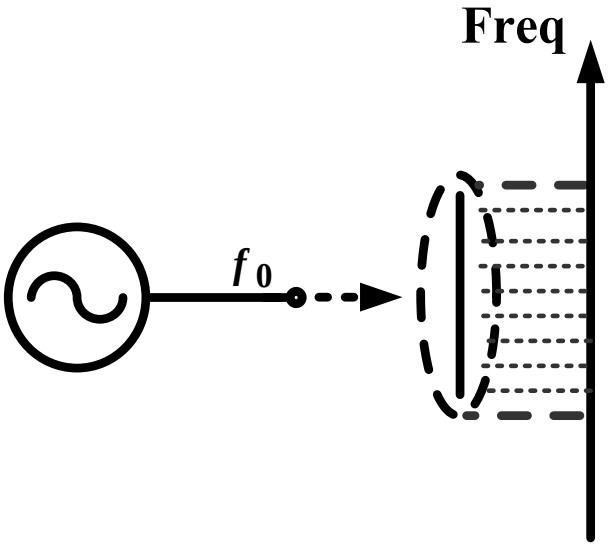
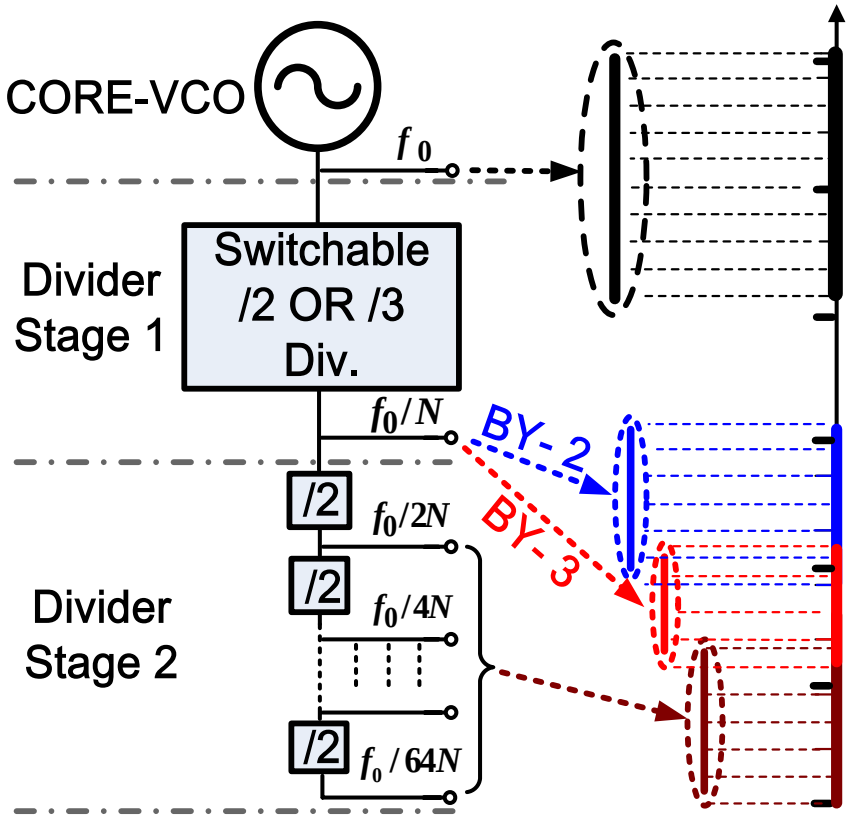


Conventional



Proposed

[REF]: Wei Deng, Kenichi Okada, and Akira Matsuzawa "A 0.5-V, 0.05-to-3.2 GHz, 4.1-to-6.4 GHz LC-VCO Using E-TSPC Frequency Divider with Forward Body Bias for Sub-Picosecond -Jitter Clock Generation" to be presented at Asian Solid-State Circuits Conference (A-SSCC), Nov. 2010

Summary

- Lowering of supply voltage is required to realize low-active-power circuits.
- Phase noise (Jitter) will become larger according to the voltage scaling.
- Ring-VCO become infeasible due to too large phase noise (jitter) and/or too large power consumption.
- To reduce the power consumption of the clock generator, adoption of LC-VCOs is an unavoidable way in such low-voltage condition.

Toward the Future

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- Ultra-low-voltage LC-VCO offers tremendous opportunities in phase noise (jitter) performance of clock generator in SoC design.

- The tuning range of ultra-low-voltage LC-VCO should be improved to fulfill the requirement for future 0.5-V sub-picosecond-jitter clock generation.

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Thanks for your attention!

Q & A

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